DUAL-CHANNEL IMAGE SENSOR ANALOG FRONT-END

FEATURES

- **Dual-Channel Image Signal Processing:**
  41.5-MHz Correlated Double Sampling (CDS)
  Provided Sample/Hold (S/H) Mode
- **Output Resolution: 16 Bits**
- **16-Bit Analog-to-Digital Conversion:**
  41.5-MHz Conversion Rate (per Channel)
  No Missing Codes Ensured
- **75-dB Input-Referred SNR (at 0-dB Gain)**
- **Programmable Black Level Clamping**
- **Programmable Gain Amplifier (PGA):**
  –3 dB to +18 dB (through Analog Front Gain)
- **Portable Operation:**
  Low Voltage: 2.7 V to 3.3 V
  Low Power: 290 mW at 3.0 V, 36 MHz

DESCRIPTION

The VSP2590 is a dual-channel analog front-end for processing imager output signals. The device includes a correlated double sampler (CDS), programmable gain amplifier (PGA), analog-to-digital converter (ADC), input clamp, optical black (OB) level clamp loop, serial interface, adjustable sampling timing control, and reference voltage generator. The VSP2590 also provides a sample/hold (S/H) input mode.

The VSP2590 is offered in a BGA-159 package and operates on a single +3 V supply.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VSP2590	BGA-159	ZWV	–25°C to +85°C	VSP2590	VSP2590ZWV	Tray, 348
					VSP2590ZWVR	Tape and Reel, 1000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	VSP2590	UNIT
Supply voltage (AVDD, DLLVDD, DVDD, DRVDD, DIVDD, DIVDD2, CVDD)	+4	V
Supply voltage differences (among VCC pins)	±0.1	V
Ground voltage differences (AVSS, DLLVSS, DVSS, DRVSS, DIVSS, DIVSS2, CVSS)	±0.1	V
Digital input voltage	–0.3 to (VDD + 0.3)	V
Analog input voltage	–0.3 to (VCC + 0.3)	V
Input current (all pins except supplies)	±10	mA
Ambient temperature under bias	–40 to +125	°C
Storage temperature	–55 to +150	°C
Junction temperature	+150	°C
Package temperature (IR reflow, peak)	+260	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, all power-supply voltages = +3.0 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP2560ZWV			UNIT
			MIN	TYP	MAX	
RESOLUTION						
Resolution				16		Bits
CHANNEL						
Channel				2		Channels
CONVERSION RATE						
Maximum conversion/clock rate		VCC = 3.0 V		36	41.5	MHz
ANALOG INPUT (Channels A, B)						
Maximum input signal level for full-scale out		Gain = –3 dB		1.5		V_{PP}
Maximum input signal for full-scale out		Gain = 0 dB		1.0		V_{PP}
Allowable input range					2.5	V_{PP}
Input capacitance		Without package, stray, or ESD capacitance		15		pF
Input limit			GND – 0.3		VCC + 3.3	V
TRANSFER CHARACTERISTICS (Channels A, B)						
(DNL)	Differential nonlinearity			±0.8		LSB
(INL)	Integral nonlinearity			±32		LSB
		Data range process = 0 mV to 100 mV		±10		LSB
No missing codes				Ensured		
Signal-to-noise ratio (1)		Gain = 0 dB		75		dB
CCD offset correction range			–200		200	mV
PROGRAMMABLE GAIN						
Analog gain programmable range			–3		+18	dB
Analog gain programmable step				3		dB
Analog gain accuracy				±0.3		dB
Analog gain channel mismatch				5		%
Digital gain programmable range			0		32	dB
Digital gain programmable step				0.032		dB
INPUT CLAMP (Channels A, B)						
Clamp on-resistance				400		Ω
Clamp level		Use internal reference		1.8		V
OPTICAL BLACK CLAMP (OBCLP) LOOP						
Control DAC resolution				12		Bits
Loop time constant				40.7		µs
Optical black clamp level		Programmable range of clamp level	1536		3072	LSB
		OBCLP level at code = 1000 0000 0000b (center)		2048		LSB
		OB level program step		1		LSB

(1) SNR = 20 log (full-scale voltage/rms noise).

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, all power-supply voltages = +3.0 V, and conversion rate = 36 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP2560ZWV			UNIT
			MIN	TYP	MAX	
GENERAL-PURPOSE 8-BIT DAC (Channels A, B)						
Minimum output voltage				0.1		V
Maximum output voltage				2.9		V
Differential nonlinearity				±0.25		LSB
Integral nonlinearity				±1		LSB
Offset error				±100		mV
Gain error				±5		%
Monotonicity				Ensured		
Minimum load resistance			10			kΩ
Maximum load capacitance					1000	pF
DIGITAL INPUTS						
Logic family				CMOS		
V_{T+}	Input voltage	Low-to-high threshold		1.7		V
V_{T-}		High-to-low threshold		1.0		V
I_{IH}	Input current	Logic high, V_{IN} = +3 V			±20	µA
I_{IL}		Logic low, V_{IN} = 0 V			±20	µA
MCLK clock duty cycle				50		%
Input capacitance				5		pF
DIGITAL OUTPUT (Channels A, B)						
Logic family				CMOS		
Logic coding				Straight binary		
V_{OH}	Output voltage	DRVDD = 3.0 V, logic high, I_{OH} = –2 mA		2.8		V
V_{OL}		DRVDD = 3.0 V, logic low, I_{OL} = 2 mA		0.2		V
VCC, VDD	Supply voltage		2.7	3.0	3.3	V
Power dissipation		Not using DLL, gain = 0 dB		290		mW
		Not using DLL, gain = +18 dB		310		mW
		Using DLL, gain = 0 dB		320		mW
		Using DLL, gain = +18 dB		340		mW
		Standby mode		4.5		mW
TEMPERATURE RANGE (TOPR)						
Operating temperature			–25		+85	°C
θ_{JA}	Thermal resistance			+40		°C/W

TIMING CHARACTERISTICS

POWER-ON/POWER-OFF SEQUENCE

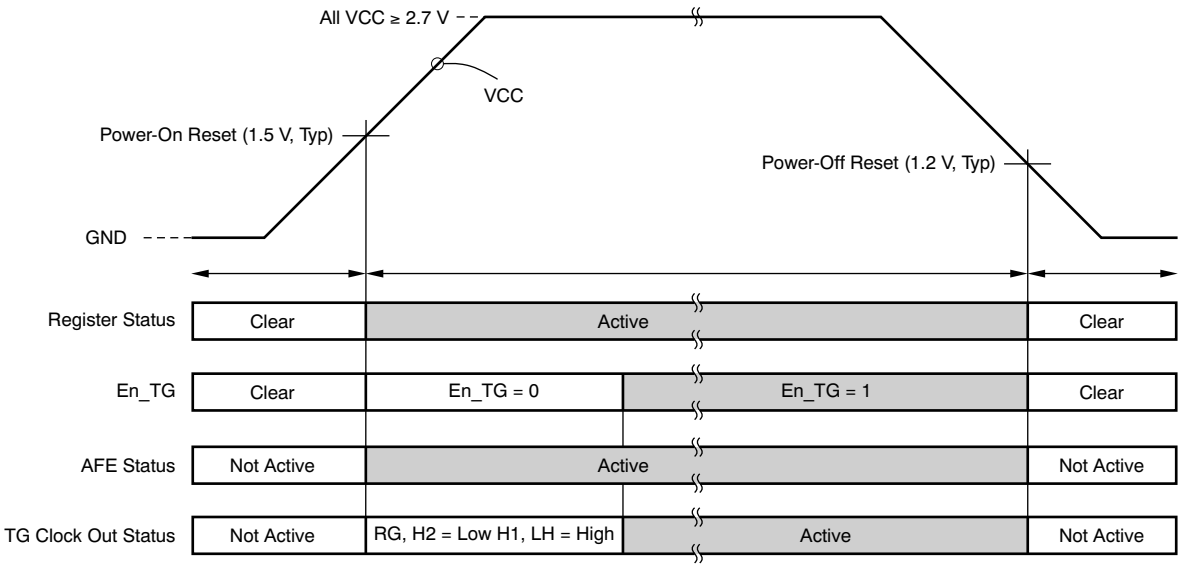


Figure 1. Power-On/Power-Off Reset Sequence

Reset Standby Function

MODE	REGISTER	CDS	ADC	RG CONTROL BUFFER	H1 CONTROL BUFFER	H2 CONTROL BUFFER	LH CONTROL BUFFER	DLL
Reset	Clear	Not active	Not active	Low	High	Low	High	Active(1)
Standby	Active	Not active	Not active	Low	High	Low	High	Active

(1) DLL is stopped by a DLL reset of a register.

DLL CLOCK (PER CHANNEL)

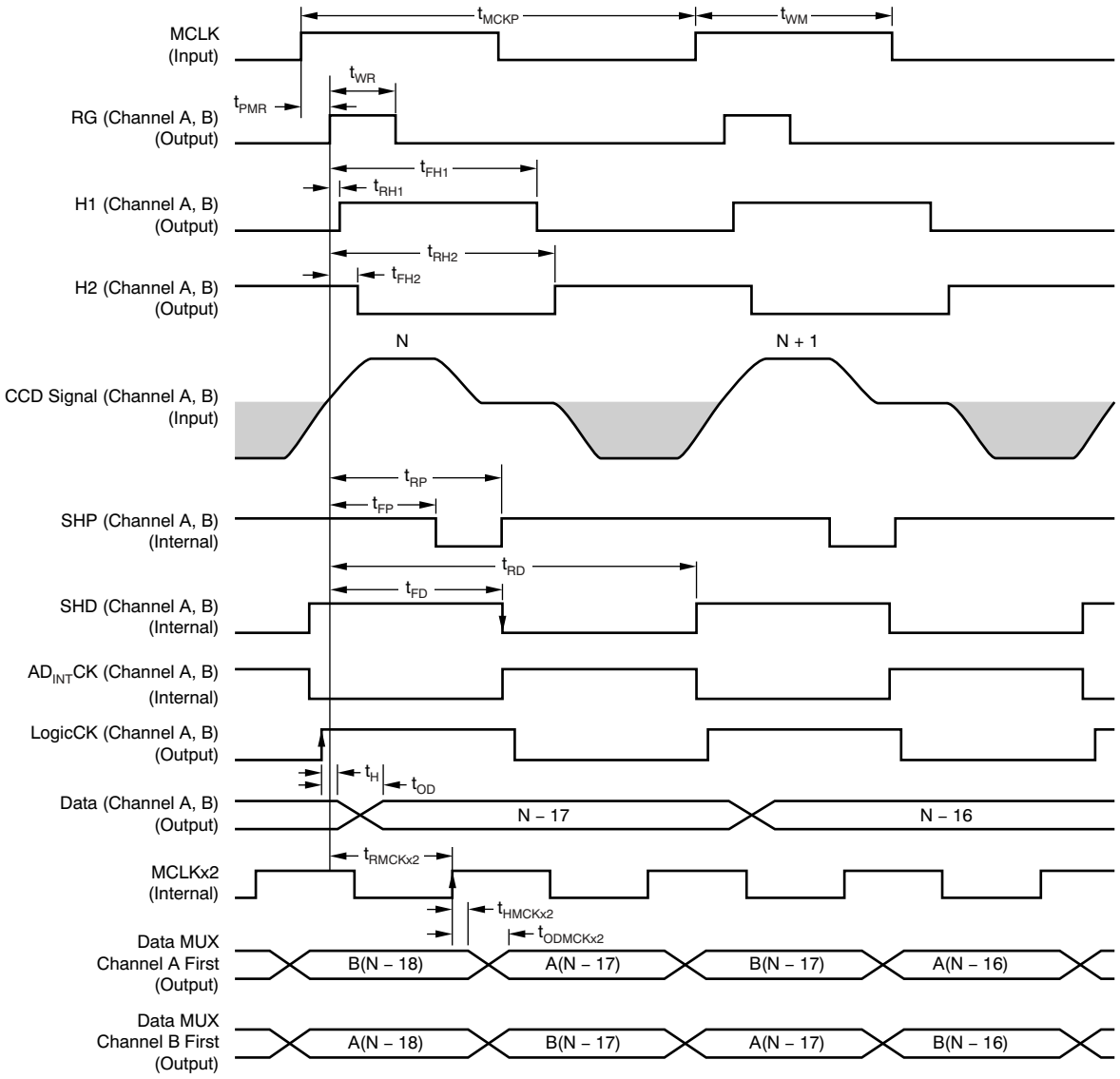


Figure 2. CDS Mode Timing Diagram for DLL Clock

CDS Mode Timing Characteristics for Figure 2(1)(2)

PARAMETER		MIN	TYP	MAX	UNIT
t_{MCKP}	Master clock period	—	27		ns
t_{WMCK}	Master clock width	—	13.5		ns
t_{PMR}	Delay master clock↑ to RG↑		2.0		ns
t_{WR}	RG pulse width	t_{MCKP}4/64	t_{MCKP}20/64	t_{MCKP}35/64	ns
t_{RH1}	Delay RG clock↑ to H1↑	–t_{MCKP}16/64	0	t_{MCKP}15/64	ns
t_{FH1}	Delay RG clock↑ to H1↓	t_{MCKP}16/64	t_{MCKP}32/64	t_{MCKP}47/64	ns
t_{RH2}	Delay RG clock↑ to H2↑	t_{MCKP}16/64	t_{MCKP}32/64	t_{MCKP}47/64	ns
t_{FH2}	Delay RG clock↑ to H2↓	–t_{MCKP}16/64	0	t_{MCKP}15/64	ns
t_{RLH}	Delay RG clock↑ to LH↑	–t_{MCKP}16/64	0	t_{MCKP}15/64	ns
t_{FLH}	Delay RG clock↑ to LH↓	t_{MCKP}16/64	t_{MCKP}32/64	t_{MCKP}47/64	ns
t_{RP}	Delay RG clock↑ to SHP↑	t_{MCKP}10/64	t_{MCKP}26/64	t_{MCKP}41/64	ns
t_{FP}	Delay RG clock↑ to SHP↓	–t_{MCKP}3/64	t_{MCKP}13/64	t_{MCKP}28/64	ns
t_{RD}	Delay RG clock↑ to SHD↑	t_{MCKP}42/64	t_{MCKP}58/64	t_{MCKP}73/64	ns
t_{FD}	Delay RG clock↑ to SHD↓	t_{MCKP}11/64	t_{MCKP}27/64	t_{MCKP}42/64	ns
t_{RMCKx2}	Delay RG clock↑ to 2MCLK↑	t_{MCKP}5/64	t_{MCKP}21/64	t_{MCKP}36/64	ns
SDLL	DLL step		t_{MCKP}/64		ns
t_H	Data hold time	1.3	1.7	2.5	ns
t_{OD}	Data output delay	2.6	3.7	6.1	ns
$t_{HMCLKx2}$	MUX data hold time	1.7	2.3	3.7	ns
$t_{ODMCLKx2}$	MUX data output delay	3.4	2.6	7.2	ns
CDL	Master clock latency	—	17	—	Clocks

(1) $T_{FP} < T_{RP}$.
(2) When a master clock stops, the DLL stops and returns to a standby condition.

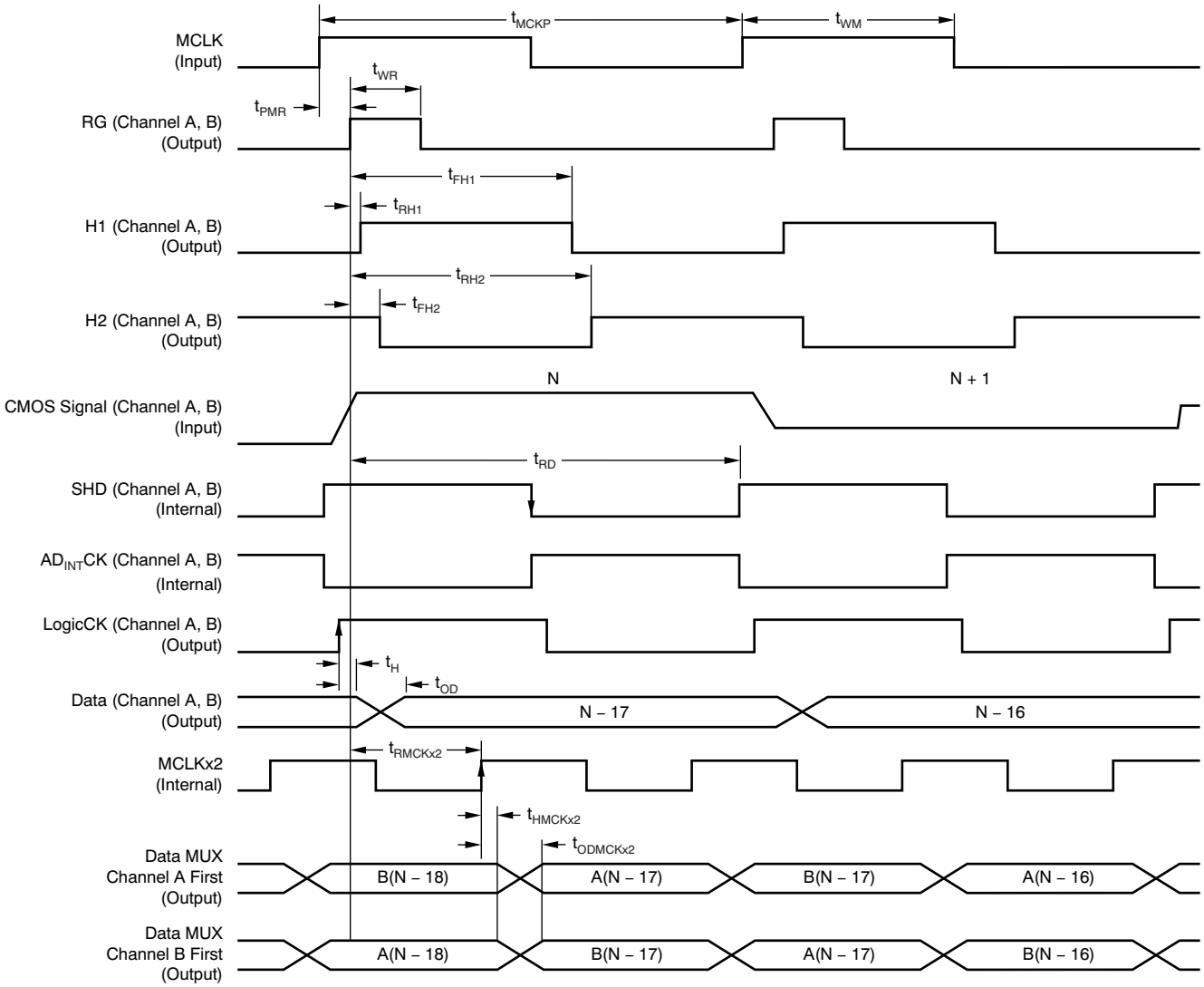


Figure 3. S/H Mode Timing Diagram for DLL Clock

S/H Mode Timing Characteristics for Figure 3(1)(2)

PARAMETER		MIN	TYP	MAX	UNIT
t_{MCKP}	Master clock period	—	27		ns
t_{WMCK}	Master clock width	—	13.5		ns
t_{PMR}	Delay master clock↑ to RG↑		2.0		ns
t_{WR}	RG pulse width	t_{MCKP}4/64	t_{MCKP}20/64	t_{MCKP}35/64	ns
t_{RH1}	Delay RG clock↑ to H1↑	–t_{MCKP}16/64	0	t_{MCKP}15/64	ns
t_{FH1}	Delay RG clock↑ to H1↓	t_{MCKP}16/64	t_{MCKP}32/64	t_{MCKP}47/64	ns
t_{RH2}	Delay RG clock↑ to H2↑	t_{MCKP}16/64	t_{MCKP}32/64	t_{MCKP}47/64	ns
t_{FH2}	Delay RG clock↑ to H2↓	–t_{MCKP}16/64	0	t_{MCKP}15/64	ns
t_{RLH}	Delay RG clock↑ to LH↑	–t_{MCKP}16/64	0	t_{MCKP}15/64	ns
t_{FLH}	Delay RG clock↑ to LH↓	t_{MCKP}16/64	t_{MCKP}32/64	t_{MCKP}47/64	ns
t_{RD}	Delay RG clock↑ to SHD↑	t_{MCKP}42/64	t_{MCKP}58/64	t_{MCKP}73/64	ns
t_{FD}	Delay RG clock↑ to SHD↓		t_{MCKP}27/64		ns
$t_{RMCLKx2}$	Delay RG clock↑ to 2MCLK↑	t_{MCKP}5/64	t_{MCKP}21/64	t_{MCKP}36/64	ns
SDLL	DLL step		t_{MCKP}/64		ns
t_H	Data hold time	1.3	1.7	2.5	ns
t_{OD}	Data output delay	2.6	3.7	6.1	ns
$t_{HMCLKx2}$	MUX data hold time	1.7	2.3	3.7	ns
$t_{ODMCLKx2}$	MUX data output delay	3.4	2.6	7.2	ns
CDL	Master clock latency	—	17	—	Clocks

(1) $T_{FP} < T_{RP}$.
(2) When a master clock stops, the DLL stops and returns to a standby condition.

EXTERNAL CLOCK (PER CHANNEL)

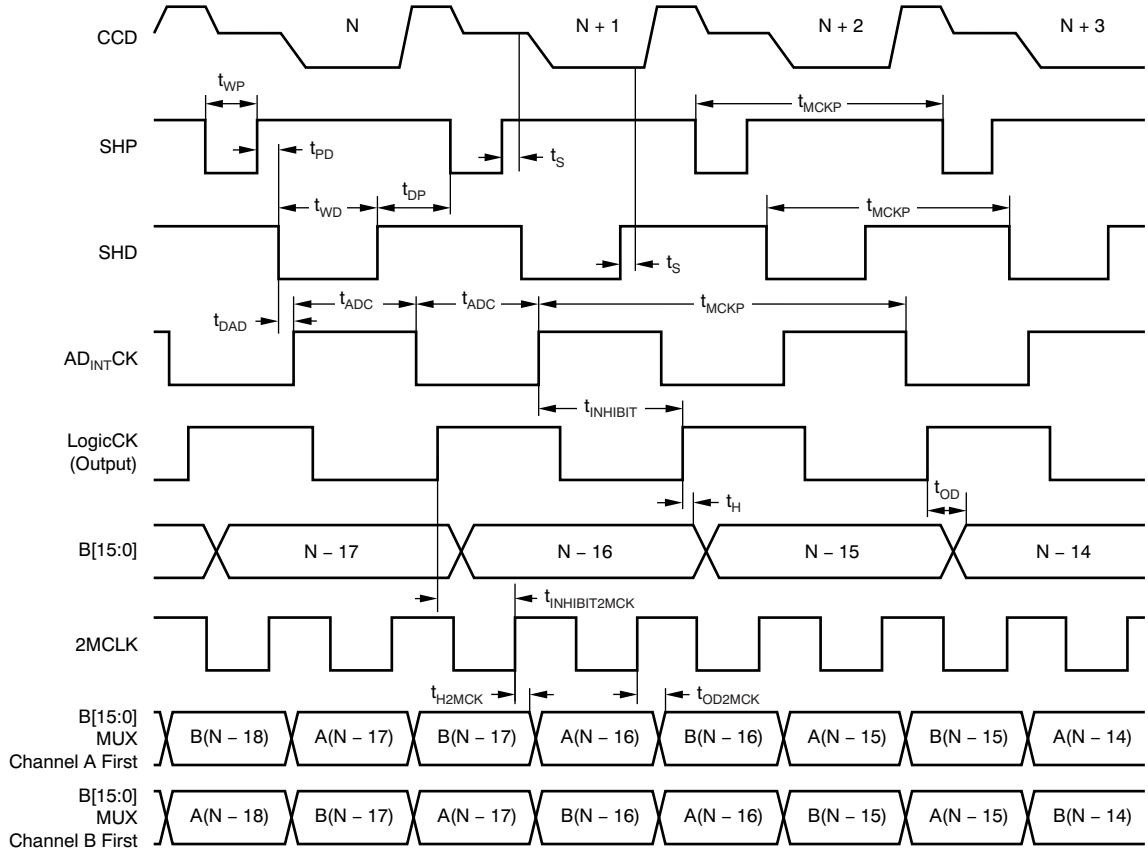


Figure 4. CDS Mode Timing Diagram for External Clock

CDS Mode Timing Characteristics for Figure 4(1)

PARAMETER		MIN	TYP	MAX	UNIT
t_{MCKP}	Clock period		27		ns
t_{ADC}	$AD_{INT}CK$ high or low level		13.5		ns
t_{WP}	SHP pulse width		6		ns
t_{WD}	SHD pulse width		13.5		ns
t_{PD}	SHP↑ to SHD↓		0		ns
t_{DP}	SHD↑ to SHP↓		9		ns
t_S	Sampling delay		3		ns
t_{DAD}	SHD↓ to $AD_{INT}CK$↑		0		ns
$t_{INHIBIT}$	Inhibit clock period from $AD_{INT}CK$↑ to LogicCK↑	4	7	10	ns
t_H	Data hold time	1.3	1.7	2.5	ns
t_{OD}	Data output delay	2.6	3.7	6.1	ns
$t_{HMCLKx2}$	MUX data hold time	1.7	2.3	3.7	ns
$t_{ODMCLKx2}$	MUX data output delay	3.4	2.6	7.2	ns
$t_{INHIBIT2MCK}$	Inhibit clock period from LogicCK↑ to 2MCLK↑	1.3	3.7	6.1	ns
DL	Data latency		17		Clocks

(1) $t_{WP} + t_{PD}$ should be nearly equal to $t_{WD} + t_{DP}$.

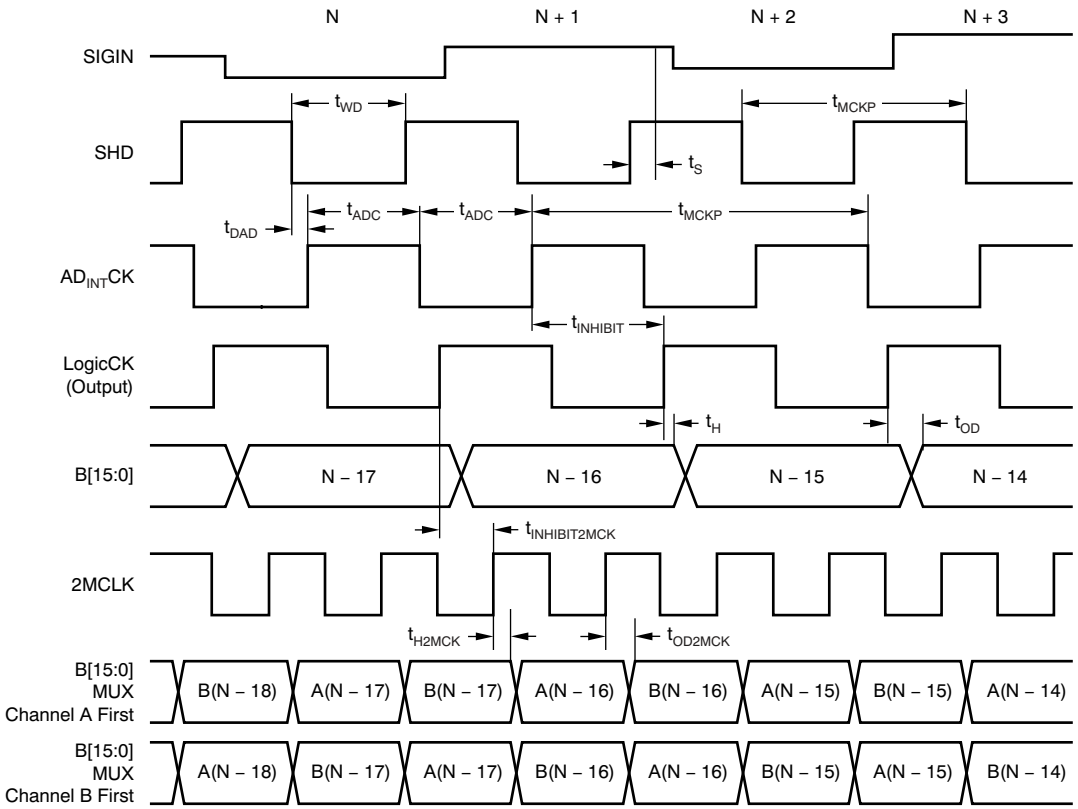


Figure 5. S/H Mode Timing Diagram for External Clock

S/H Mode Timing Characteristics for Figure 5(1)

PARAMETER		MIN	TYP	MAX	UNIT
t_{MCKP}	Clock period		27		ns
t_{ADC}	$AD_{INT}CK$ high or low level		13.5		ns
t_{WD}	SHD pulse width		6		ns
t_S	Sampling delay		3		ns
t_{DAD}	SHD↓ to $AD_{INT}CK$↑		0		ns
$t_{INHIBIT}$	Inhibit clock period from $AD_{INT}CK$↑ to LogicCK↑	4	7	10	ns
t_H	Data hold time	1.3	1.7	2.5	ns
t_{OD}	Data output delay	2.6	3.7	6.1	ns
$t_{HMCLKx2}$	MUX data hold time	1.7	2.3	3.7	ns
$t_{ODMCLKx2}$	MUX data output delay	3.4	2.6	7.2	ns
$t_{INHIBIT2MCK}$	Inhibit clock period from LogicCK↑ to 2MCLK↑	1.3	3.7	6.1	ns
DL	Data latency		17		Clocks

(1) $t_{WP} + t_{PD}$ should be nearly equal to $t_{WD} + t_{DP}$.

H1, H2, HSEL1, HSEL2, AND PBLK

H1 and H2 Timing While PBLK is Low (per channel)

When PBLK is low, H1 is fixed high and H2 is fixed low. For the duration that PBLK is low, H1 and H2 can be toggled only by the HSEL1 and HSEL2 input.

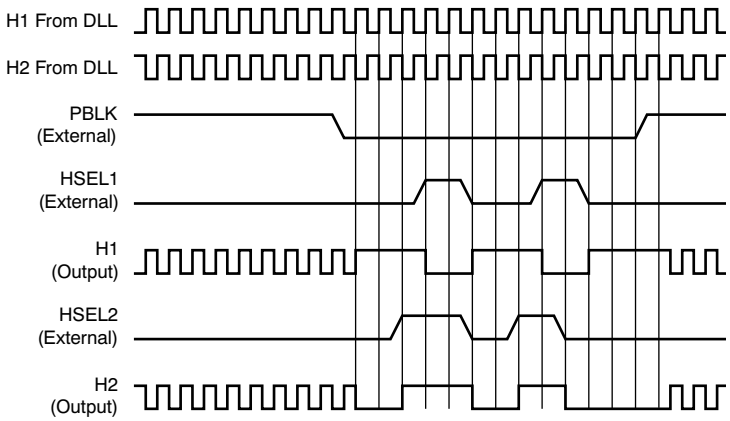


Figure 6. H1 and H2 Timing Diagram

HSEL1, HSEL2, and PBLK Timing

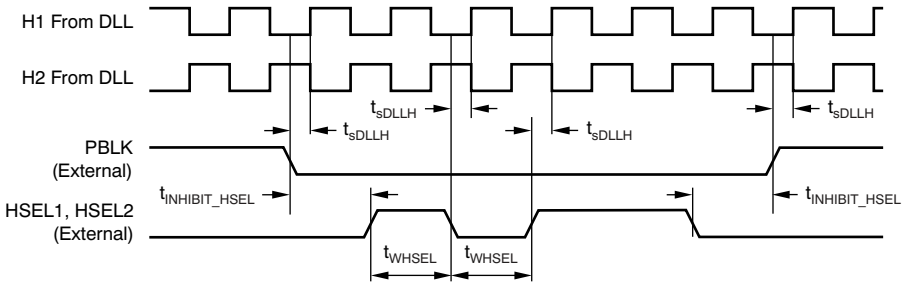


Figure 7. HSEL1, HSEL2, and PBLK Timing Diagram

Timing Characteristics for Figure 7

PARAMETER		MIN	TYP	MAX	UNIT
$t_{INHIBIT\_HSEL}$	HSEL high period inhibit timing (from PBLK)	$-t_{MCKP}$		$+t_{MCKP}$	ns
t_{WHSEL}	HSEL high/low period	t_{MCKP}			ns
t_{sDLLH}	Setup time H1/H2 (from DLL) to PBLK/HSEL1/HSEL2	800			ps

SERIAL INTERFACE

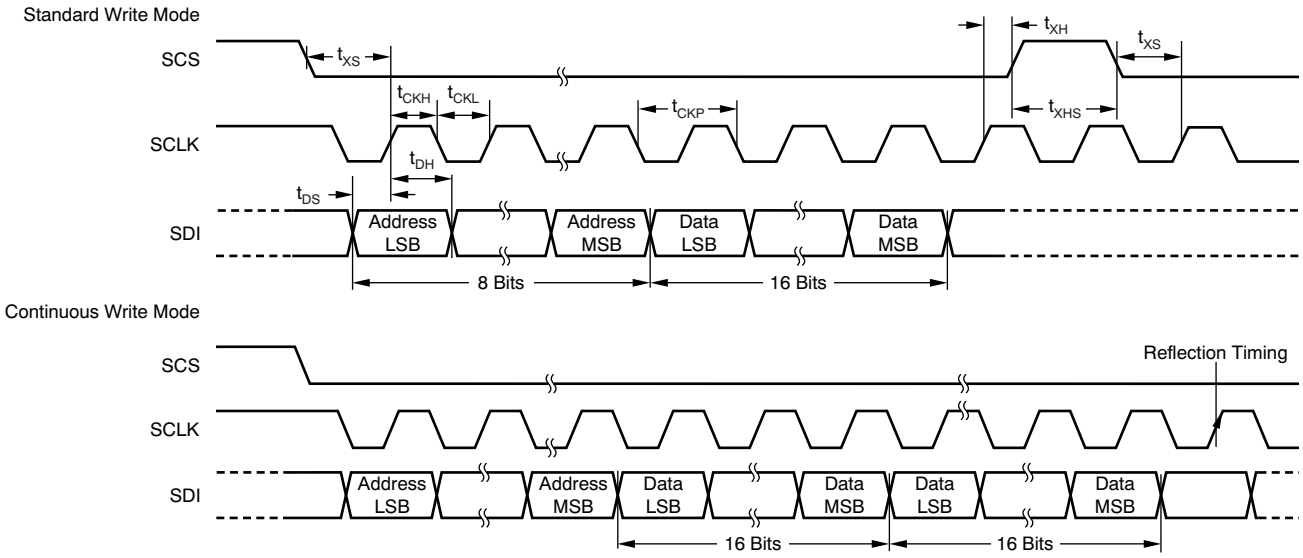


Figure 8. Serial Interface Timing Diagram

Update Timing

Immediate Update:

The data shift operation should decode at the rising edge of SCLK while S_{LOAD} is low. 16 bits of input data are loaded to the parallel latch in the VSP2590 at the rising edge of SCS.

External Sync Update:

Register update timing is synchronized with the falling edge of UPDATE_REG.

Continuous Writing

Continuous write mode is used when transmitting a large set of data. Receiving data initiates at the falling edge of S_{LOAD} and continues while S_{LOAD} is low. It is only necessary to transmit the starting address data; after that transmission, the address increments by one automatically. The data stream then consists of the starting address followed by the data for that register, then the data for the next register, and so on. The device accepts data for sequential registers as long as S_{LOAD} is low. When S_{LOAD} goes high, no more registers are written to.

Over or Shortage Data Input

16-bit data are counted by SCLK. Any over or shortage data are ignored.

Timing Characteristics for Figure 8

PARAMETER		MIN	TYP	MAX	UNIT
t_{CKP}	Clock period	50			ns
t_{CKH}	Clock high pulse width	25			ns
t_{CKL}	Clock low pulse width	25			ns
t_{DS}	Data setup time	15			ns
t_{DH}	Data hold time	15			ns
t_{XS}	S_{LOAD} to SCLK setup time	20			ns
t_{XH}	SCLK to $\overline{CS}$ hold time	50			ns
t_{XHS}	$\overline{CS}$ width	50			ns

REGISTER UPDATE

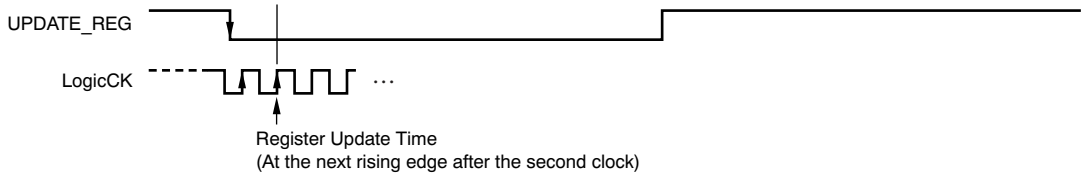


Figure 9. Register Update Timing Diagram

PIXEL COUNT-UP START TIMING

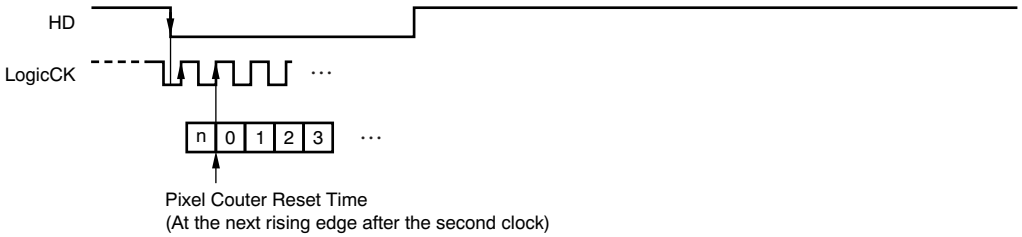


Figure 10. Pixel Count-Up Timing Diagram

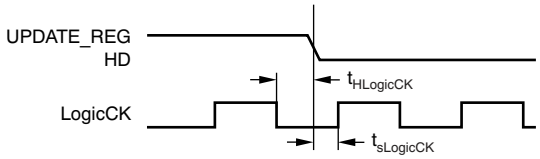


Figure 11. LogicCK Timing Diagram

Timing Characteristics for Figure 11

PARAMETER		MIN	TYP	MAX	UNIT
$t_{SLogicCK}$	Setup time LogicCK to UPDATE_REG/UPDATE_INL/HD	800			ps
$t_{HLogicCK}$	Hold time LogicCK to UPDATE_REG/UPDATE_INL/HD	2.0			ns

PIN CONFIGURATION

ZWV PACKAGE
BGA-159
(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AVSSA	COBA	TEST_ref	CMA	REFNA	REFPA	CVDDA	LogicCKAD	MnSHPA	MnLogicCKA	CVDDA	BYPDA	DLLVSSA	MCLKA
B	AVDDA	AVSSA	BYPCMA	REFVSSA	REFVDDA	GNDG	CVSSA	MCLKx2in	MnSHDA	PBLK	CVSSA	DLLVSSA	DLLVDDA	DLLVDDA
C	CCDINA	AVSSA		DOUT21	DOUT17	DOUT13	DVSS	DOUT9	DOUT5	DOUT1	DVSS	DVDD	DVSS	DVDD
D	CCDGNDA	AVSSA	DVDD	DOUT23	DOUT19	DOUT15	DVDD	DOUT11	DOUT7	DOUT3	RGA	H2A	H1A	LHA
E	AVDDA	AVDDA	UDACOUT1	DOUT25							DRVDD	DRVDD	DRVSS	DRVSS
F	CLPDMA	DIVSSA	DIVDDA	DOUT27							HSEL1	HSEL2	TEST_UPDATE	SCLK
G	CLPOBA	DIVSSA	DOUT31	DOUT29							TEST_IN	UPDATE_REG	S_{LOAD}	DIVSS2
H	CLPOBB	DIVSSB	DOUT30	DOUT28							TEST_OUT	SDI	RESET (XCLR)	DIVSS2
J	CLPDMB	DIVSSB	DIVDDB	DOUT26							TEST_IN	DIVDD2	DIVSS2	DIVSS2
K	AVDDB	AVDDB	UDACOUT2	DOUT24							DRVDD	DRVDD	DRVSS	DRVSS
K	CCGNDB	AVSSB	DVDD	DOUT22	DOUT18	DOUT14	DVDD	DOUT10	DOUT6	DOUT2	RGB	H2B	H1B	LHB
K	CCDINB	AVSSB	DVSS	DOUT20	DOUT16	DOUT12	DVSS	DOUT8	DOUT4	DOUT0	DVSS	DVDD	DVSS	DVDD
K	AVDDB	AVSSB	BYPCMB	REFVSSB	REFVDDB	GNDG	CVSSB	TEST_IN	MnSHDB	HD	CVSSB	DLLVSSB	DLLVDDB	DLLVDDB
K	AVSSB	COBB	TEST_ref	CMB	REFNB	REFPB	CVDDB	LogicCKBD	MnSHPB	MnLogicCKB	CVDDB	BYPDB	DLLVSSB	MCLKB

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A1	AVSSA	P	Analog GND (channel A)
A2	COBA	AO	OB loop output voltage connected to a 0.1-µF capacitor (channel A)
A3	Test_ref	AO	Test setting pin (Hi-Z)
A4	CMA	AO	Analog common dc reference connected to a 0.1-µF capacitor (channel A)
A5	REFNA	AO	ADC negative reference connected to a 0.1-µF capacitor (channel A)
A6	REFPA	AO	ADC positive reference connected to a 0.1-µF capacitor (channel A)
A7	CVDDA	P	Mask block power supply (channel A)
A8	LogicCKAD	DO	Logic clock output (channel A) for digital chip and total output
A9	MnSHPA	DIO	SHP monitor out/external SHP input (channel A)
A10	MnLogicCKA	DIO	MCLKx2 monitor out/external logicCK input (channel A)
A11	CVDDA	P	HTG block power supply (channel A)
A12	BYPDA	AO	DLL bypass connected to DLLVDD 1000-pF capacitor (channel A)
A13	DLLVSSA	P	DLL GND (channel A)
A14	MCLKA	DI	Masker clock (channel A) input
B1	AVDDA	P	Analog power supply (channel A)
B2	AVSSA	P	Analog GND (channel A)
B3	BYPCMA	AO	Analog positive reference connected to a 0.1-µF capacitor (channel A)
B4	REFVSSA	P	Reference block GND (channel A)
B5	REFVDDA	P	Reference block power supply (channel A)
B6	GNDG	P	SUB GND
B7	CVSSA	P	Mask block GND (channel A)
B8	MCLKx2in	DI	External CLKx2 input
B9	MnSHDA	DIO	SHD monitor out/external SHD input (channel A)
B10	PBLK	DI	Pre-blanking signal input; connect to DVDD when PBLK is not used
B11	CVSSA	P	HTG block GND (channel A)
B12	DLLVSSA	P	DLL GND (channel A)
B13	DLLVDDA	P	DLL power supply (channel A)
B14	DLLVDDA	P	DLL power supply (channel A)
C1	CCDINA	AI	CCD/CMOS sensor signal input (channel A)

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
C2	AVSSA	P	Analog GND (channel A)
C4	DOUT21	DO	Data output (channel A)
C5	DOUT17	DO	Data output (channel A)
C6	DOUT13	DO	Data output (channel B/MUX)
C7	DVSS	P	Digital GND
C8	DOUT9	DO	Data output (channel B/MUX)
C9	DOUT5	DO	Data output (channel B/MUX)
C10	DOUT1	DO	Data output (channel B/MUX)
C11	DVSS	P	Digital GND
C12	DVDD	P	Digital power supply
C13	DVSS	P	Digital GND
C14	DVDD	P	Digital power supply
D1	CCDGNDA	AI	CCD GND connection/CMOS sensor signal input (channel A)
D2	AVSSA	P	Analog GND (channel A)
D3	DVDD	P	Digital power supply
D4	DOUT23	DO	Data output (channel A)
D5	DOUT19	DO	Data output (channel A)
D6	DOUT15	DO	Data output, MSB (channel B/MUX)
D7	DVDD	P	Digital power supply
D8	DOUT11	DO	Data output (channel B/MUX)
D9	DOUT7	DO	Data output (channel B/MUX)
D10	DOUT3	DO	Data output (channel B/MUX)
D11	RGA	DO	RG pulse output (channel A)
D12	H2A	DO	H2 pulse output (channel A)
D13	H1A	DO	H1 pulse output (channel A)
D14	LHA	DO	LH pulse output (channel A)
E1	AVDDA	P	Analog power supply (channel A)
E2	AVDDA	P	Analog power supply (channel A)
E3	UDACOUT1	AO	Universal DAC1 output
E4	DOUT25	DO	Data output (channel A)
E11	DRVDD	P	Digital out power supply
E12	DRVDD	P	Digital out power supply
E13	DRVSS	P	Digital out GND
E14	DRVSS	P	Digital out GND
F1	CLPDMA	DI	CLPDM pulse input (channel A); connect to DVDD when CLPDM is not used
F2	DIVSSA	P	CLKGEN GND supply (channel A)
F3	DIVDDA	P	CLKGEN power supply (channel A)
F4	DOUT27	DO	Data output (channel A)
F11	HSEL1	DI	Horizontal mask timing 1; connect to GND when HSEL1 is not used
F12	HSEL2	DI	Horizontal mask timing 2; connect to GND when HSEL2 is not used
F13	TEST_Update	DI	Test setting pin; connect to DVDD
F14	SCLK	DI	Serial interface clock
G1	CLPOBA	DI	CLPOB pulse input (channel A); connect to DVDD when CLPOB is not used
G2	DIVSSA	P	CLKGEN GND supply (channel A)
G3	DOUT31	DO	Data output, MSB (channel A)
G4	DOUT29	DO	Data output (channel A)
G11	TEST_IN	DI	Test setting pin; connect to GND
G12	UPDATE_REG	DI	Serial interface signal
G13	SLOAD	DI	SPI signal
G14	DIVSS2	P	Serial interface GND

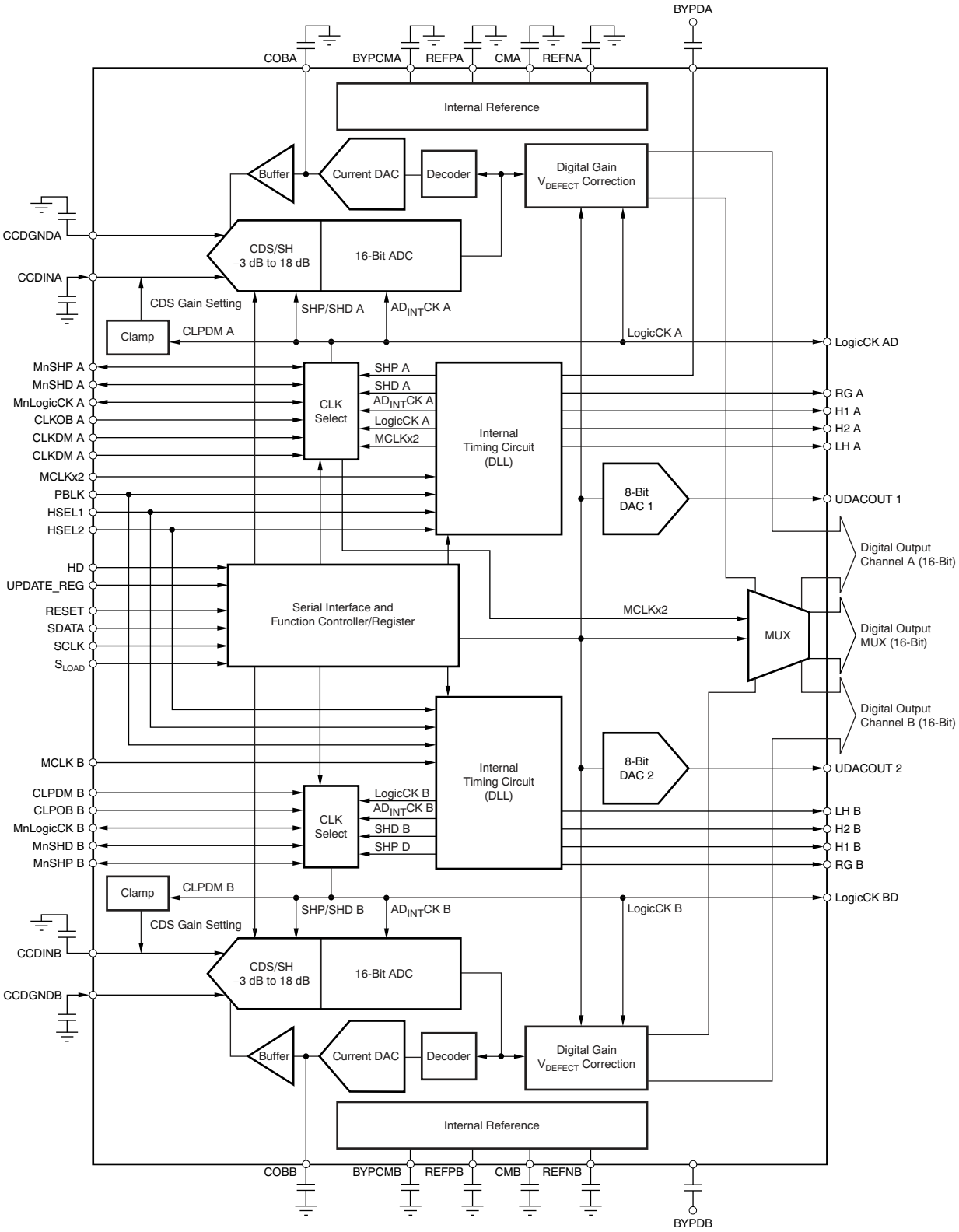
TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
H1	CLPOBB	DI	CLPOB pulse input (channel B); Connect to DVDD when CLPOB is not used
H2	DIVSSB	P	CLKGEN GND supply (channel B)
H3	DOUT30	DO	Data output (channel A)
H4	DOUT28	DO	Data output (channel A)
H11	TEST_OUT	DO	Test setting pin (normal operation = Hi-Z)
H12	SDI	DI	SRI signal
H13	RESET	DI	System reset; connect to DVDD when RESET is not used
H14	DIVSS2	P	Serial interface GND
J1	CLPDMB	DI	CLPDM pulse input (channel B); connect to DVDD when CLPDM is not used
J2	DIVSSB	P	CLKGEN GND supply (channel B)
J3	DIVDDB	P	CLKGEN power supply (channel B)
J4	DOUT26	DO	Data output (channel A)
J11	TEST_IN	DI	Test setting pin; connect to GND
J12	DIVDD2	P	Serial interface power supply
J13	DIVSS2	P	Serial interface GND
J14	DIVSS2	P	Serial interface GND
K1	AVDDB	P	Analog power supply (channel B)
K2	AVDDB	P	Analog power supply (channel B)
K3	UDACOUT2	AO	Universal DAC2 output
K4	DOUT24	DO	Data output (channel A)
K11	DRVDD	P	Digital out power supply
K12	DRVDD	P	Digital out power supply
K13	DRVSS	P	Digital out GND
K14	DRVSS	P	Digital out GND
L1	CCDGNDB	AI	CCD GND connection/CMOS sensor signal input (channel B)
L2	AVSSB	P	Analog GND (channel B)
L3	DVDD	P	Digital power supply
L4	DOUT22	DO	Data output (channel A)
L5	DOUT18	DO	Data output (channel A)
L6	DOUT14	DO	Data output (channel B/MUX)
L7	DVDD	P	Digital power supply
L8	DOUT10	DO	Data output (channel B/MUX)
L9	DOUT6	DO	Data output (channel B/MUX)
L10	DOUT2	DO	Data output (channel B/MUX)
L11	RGB	DO	RG pulse output (channel B)
L12	H2B	DO	H2 pulse output (channel B)
L13	H1B	DO	H1 pulse output (channel B)
L14	LHB	DO	LH pulse output (channel B)
M1	CCDINB	AI	CCD/CMOS sensor signal input (channel B)
M2	AVSSB	P	Analog GND (channel B)
M3	DVSS	P	Digital GND
M4	DOUT20	DO	Data output (channel A)
M5	DOUT16	DO	Data output, LSB (channel A)
M6	DOUT12	DO	Data output (channel B/MUX)
M7	DVSS	P	Digital GND
M8	DOUT8	DO	Data output (channel B/MUX)
M9	DOUT4	DO	Data output (channel B/MUX)
M10	DOUT0	DO	Data output, LSB (channel B/MUX)
M11	DVSS	P	Digital GND
M12	DVDD	P	Digital power supply

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
M13	DVSS	P	Digital GND
M14	DVDD	P	Digital power supply
N1	AVDDB	P	Analog power supply (channel B)
N2	AVSSB	P	Analog GND (channel B)
N3	BYPCMB	AO	Analog positive reference connected to a 0.1-μF capacitor (channel B)
N4	REFVSSB	P	Reference block GND (channel B)
N5	REFVDDB	P	Reference block power supply (channel B)
N6	GNDG	P	SUB GND
N7	CVSSB	P	Mask block GND (channel B)
N8	TEST_IN	DI	Test setting pin; connect to GND
N9	MnSHDB	DIO	SHD monitor out/external SHD input (channel B)
N10	HD	DI	HD timing pulse input; connect to DVDD when HD is not used
N11	CVSSB	P	HTG block GND (channel B)
N12	DLLVSSB	P	DLL GND (channel B)
N13	DLLVDDB	P	DLL power supply (channel B)
N14	DLLVDDB	P	DLL power supply (channel B)
P1	AVSSB	P	Analog GND (channel B)
P2	COBB	AO	OB loop output voltage connected to a 0.1 μF-capacitor (channel B)
P3	Test_ref	AO	Test setting pin (Hi-Z)
P4	CMB	AO	Analog common dc reference connected to a 0.1-μF capacitor (channel A)
P5	REFNB	AO	ADC negative reference connected to a 0.1-μF capacitor (channel B)
P6	REFPB	AO	ADC positive reference connected to a 0.1-μF capacitor (channel B)
P7	CVDDB	P	Mask block power supply
P8	LogicCKBD	DO	Logic clock output (channel B) for digital chip and total output
P9	MnSHPB	DIO	SHP monitor out/external SHP input (channel B)
P10	MnLogicCKB	DIO	External logicCK input (channel B)
P11	CVDDB	P	HTG block power supply (channel B)
P12	BYPDB	AO	DLL bypass connected to DLLVDD 1000-pF capacitor (channel B)
P13	DLLVSSB	P	DLL GND (channel B)
P14	MCLKB	DI	Masker clock input (channel B)

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

OVERVIEW

The VSP2590 is a dual-channel analog front-end device for processing imager output signals. A simplified block diagram is shown in Figure 12. The VSP2590 includes a sample/hold mode (S/H), programmable gain amplifier (PGA), analog-to-digital converter (ADC), input clamp, optical black (OB) level clamp loop, serial interface, timing control, and reference voltage generator. The device also provides a correlated double sampler (CDS) input mode. This CDS input mode consists of reconfiguration from the S/H circuit. The input mode is selected through the serial interface. Both the S/H and CDS modes provide analog gain for the input circuit.

All functions and parameters (such as PGA gain control, operation mode, and other settings) can be changed via the serial interface. All parameters are reset to default values when the serial interface activates a software reset.

The PGA of the VSP2590 provides both analog and digital gain. Digital PGA is a multi-gain function. This function can set different gain coefficients for each set of two pixels. The OB offset code can also set different offsets for every two pixels.

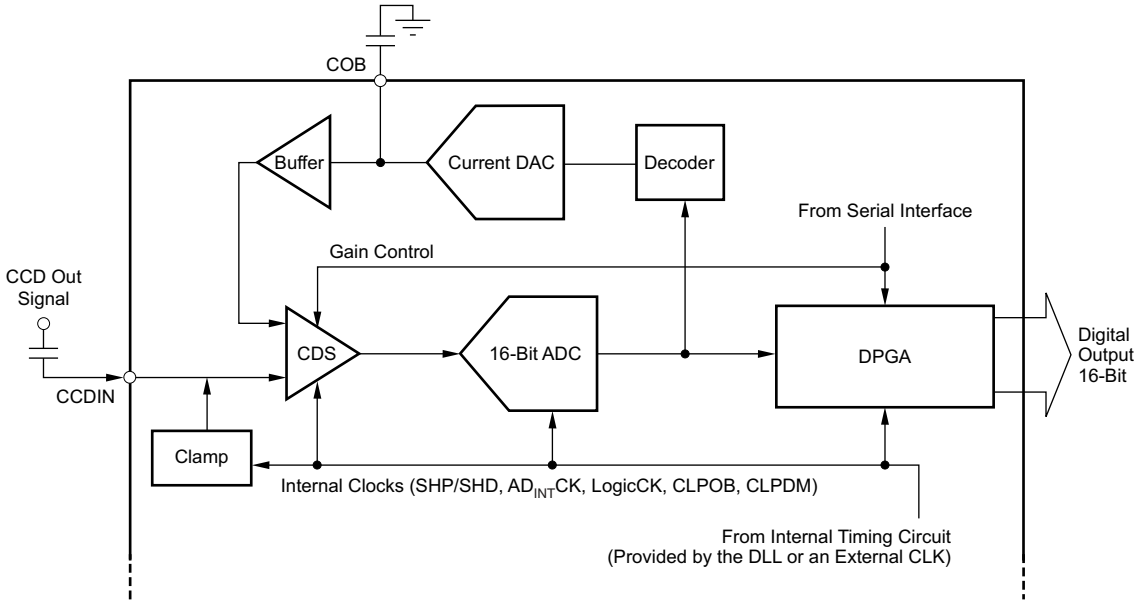


Figure 12. Simplified Block Diagram (Single Channel)

SAMPLE-AND-HOLD (S/H) MODE

In S/H mode, the input circuit of the VSP2590 is configured as a sample-and-hold mode by the serial interface setting. Figure 13 shows a simplified input circuit of the S/H mode. In this mode, the input signal is sampled by the SHD signal.

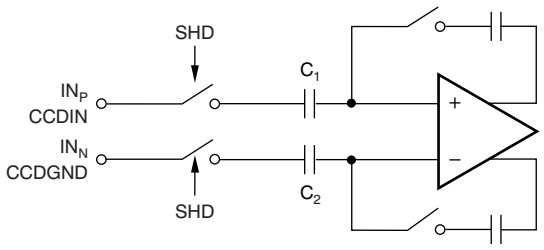


Figure 13. S/H Input Mode Block Diagram

CORRELATED DOUBLE SAMPLER (CDS) MODE

In CDS mode, the input circuit of the VSP2590 is reconfigured as correlated double sampler (CDS) by the serial interface setting. Figure 14 shows a simplified input circuit of the CDS mode.

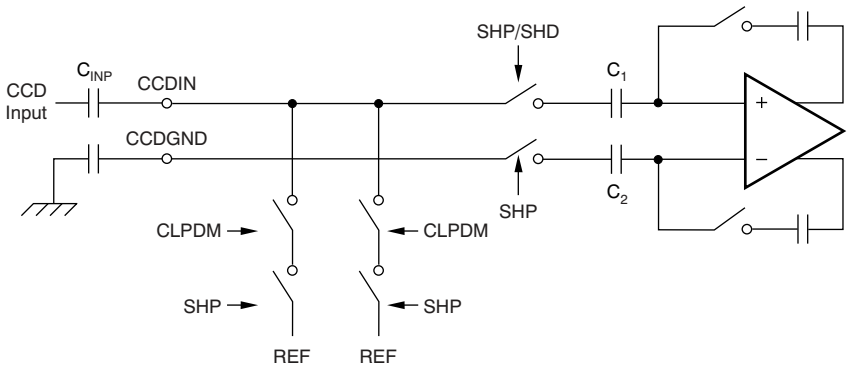


Figure 14. CDS Input Mode Block Diagram

INPUT CLAMP

In the CCD input mode, CCDIN of the VSP2590 is connected to the buffered CCD output through capacitive coupling; therefore, an input clamp is necessary. The purpose of the input clamp is to restore the dc component of the input signal that was lost during ac coupling and establish the desired dc bias point for CDS. The block diagram of Figure 14 also illustrates the input clamp. The input level is clamped to the internal reference voltage during the dummy pixel interval. More specifically, the clamping function becomes active when both CLPDM and SHP are active.

Immediately after device power on, the clamp voltage of the input capacitor is not charged. For a fast charge-up of the clamp voltage, the VSP2590 provides a boost-up circuit.

16-BIT ADC

The VSP2590 also provides a high-speed, 16-bit ADC. This ADC uses a fully differential, pipelined architecture with correction. This architecture is very advantageous for realizing better linearity at a lower signal level because large linearity errors tend to occur at specific points in the full-scale range, and the linearity improves for a level of signal below that specific point. The ADC ensures 16-bit resolution for the entire full-scale range.

OPTICAL BLACK (OB) LEVEL LOOP AND OB CLAMP LEVEL

The VSP2590 has a built-in optical black (OB) offset self-calibration circuit (OB loop) that compensates the OB level by using OB pixels that are output from the CCD image sensor. A block diagram of the OB loop and OB clamp circuit is shown in Figure 15. CCD offset is compensated by converging this calibration circuit while activating CLPOB during a period when OB pixels are output from the CCD.

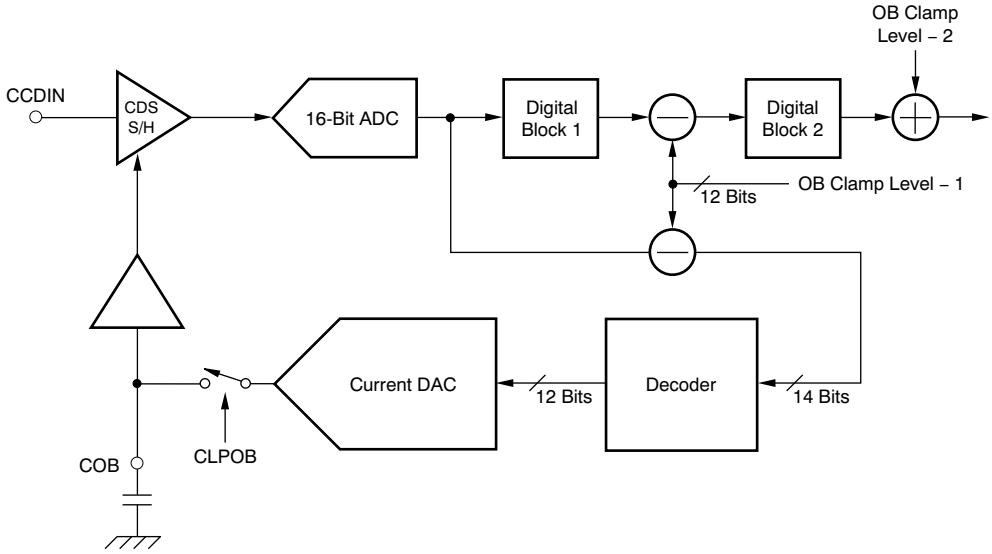


Figure 15. OB Loop and OB Level Clamp

Because the DPGA (which is a gain stage) is outside the OB loop, OB levels are not affected even when the gain changes.

The converging time of the OB loop is determined based on the capacitor value connected to the COB terminal and the output from the current output digital-to-analog converter (DAC) of the loop. The time constant, T_J, can be obtained from Equation 1:

$$T = \frac{C}{16384 \times I_{MIN}} \quad (1)$$

Where:

- C is the capacitor value connected to COB
- I_{MIN} is the minimum current (0.15 µA) of the current DAC, which is the current equivalent to 1 LSB of the DAC output.

When C = 0.1 µF, T is 40.7 µs.

Slew rate (SR) can be obtained from Equation 2:

$$SR = \frac{I_{MAX}}{C} \quad (2)$$

Where:

- C is the capacitor value connected to COB
- I_{MAX} is maximum current (153 µA) of the current DAC, which is the current equivalent to 1023 LSB of the DAC output.

DAC output current multiplication is provided. This function increases the DAC output current through serial interface as multiples of x2, x4, and x8. Increased DAC current shortens the time constant of the OB loop. In the case where the OB level drastically changes and must quickly settle the loop, this function is effective.

Immediately after power on, the COB capacitor voltage is not charged. For fast start-up, a COB voltage boost-up circuit is provided.

The OB clamp level can be set from 1536 to 3072 in 1-LSB steps, and provide a multi-OB level function that can be set to different offset values for each two-pixel pair. Table 1 lists the input code and OB clamp level.

Table 1. Input Code and OB Clamp Level

CODE	16-BIT CLAMP LEVEL (LSB)
0110 0000 0000b	1536
0110 0000 0001b	1537
—	—
0111 1111 1110b	2046
0111 1111 1111b	2047
1000 0000 0000b (default)	2048
—	—
1011 1111 1111b	3071
1100 0000 0000b	3072

PROGRAMMABLE GAIN

The VSP2590 gain ranges from –3 dB to 50 dB. The desired gain is set through a combination of analog gain and the digital programmable gain amplifier (DPGA). Both gain controls through the serial interface.

Analog gain can be programmed from –3 dB to 18 dB in 3-dB steps. The –3-dB gain is provided for large input signals (such as over 1.0 V). Digital gain can be programmed from 0 dB to 32 dB in 0.032-dB steps. The digital gain changes linearly in proportion to the setting code. The relationship between the input code and digital gain is shown in Figure 16.

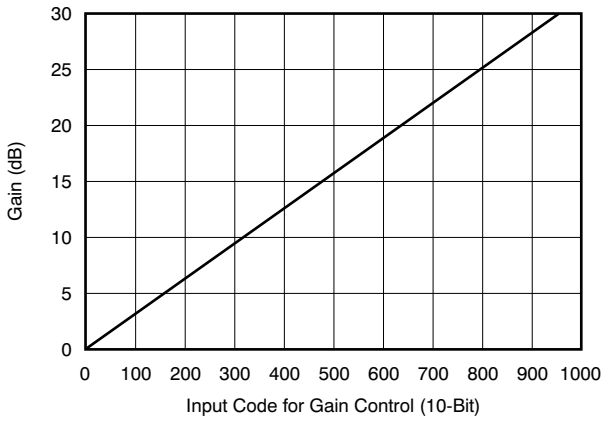


Figure 16. Setting Code versus Gain

CLOCKING AND DLL

The VSP2590 requires the following clocks for proper operation: MCLK is the system clock, SHP is the sampling pedestal level of the sensor signal, SHD is the sampling data level of the sensor signal, $AD_{INT}CK$ outputs the ADC data, CLPOB is the optical black level clamp, and CLPDM is the input clamp.

The VSP2590 has built-in DLL circuits that enable the required sampling clocks (SHP, SHD, and $AD_{INT}CK$) and the horizontal timing pulse of RG, H1, H2, and LH to be generated.

The PBLK timing signal (input from the pin) transmits the blanking period timing. In this period, high-speed horizontal timing pulses (RG, H1, H2, and LH) are masked and the trigger timing of H1 and H2 is transmitted as the external timing pulse of HSEL1 and HSEL2, respectively.

OUTPUT MULTIPLEXING

The VSP2590 allows selection of the output mode by the serial interface, dual channel mode, and multiplexing output mode. Output order in the multiplexing mode is selectable as channel A first or channel B first.

VOLTAGE REFERENCE

All reference voltages and bias currents used on the device are created from internal bandgap circuitry. The VSP2590 has a symmetrically independent voltage reference for each channel.

Both channels of the SH/CDS and the ADC use three primary reference voltages: REFP (1.5 V), REFN (1.0 V), and CM (1.275 V) of individual references. REFP and REFN are buffered on-chip. CM is derived as the midrange voltage of the resistor chain internally connecting REFP and REFN. The ADC full-scale range is determined by twice the difference voltage between REFP and REFN.

REFP, REFN, and CM should be heavily decoupled with appropriately-sized capacitors.

HOT PIXEL REJECTION

Sometimes, OB pixel output signals from the CCD include unusual level signals that are caused by pixel defection. If this level reaches a full-scale level, it may affect OB level stability. The VSP2590 has a function that rejects the unusually large pixel levels (hot pixels) in the OB pixel. This function may contribute to CCD yield improvement that is caused by OB pixel failure.

Rejection level for hot pixels is programmable through the serial interface. When hot pixels come from the CCD, the VSP2590 omits it and replaces the previous pixel level with the OB level calculation.

V_{CCD} DEFECT COMPENSATION

The VSP2590 provides a V_{CCD} defect compensation function. This function can compensate V_{CCD} defects by 32 points.

REGISTER DEFINITIONS

Table 2. Register Definitions

ADDRESS	REGISTER	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
0	Config	0	STB	STB mode	0 = Normal (circuit operates) 1 = STB mode Default = 0	Immediate
		1	REG_RST	Register reset	0 = Normal (circuit operates) 1 = clear all registers Default = 0	
		2	DLL_STB	DLL standby	0 = DLL operates 1 = DLL reset (CLK stop) Default = 0	
		3	DLL_RST	DLL reset	0 = DLL reset 1 = DLL operates Default = 1	
		5:4	PT	CLPOB loop current control	00b = 6.2 µA 10b = 24.8 µA 01b = 12.4 µA 11b = 49.6 µA Default = 00b	
		7:6	—	Reserved	Fixed at 0 Default = 00b	
		8	INPPOL	S/H mode data level polarity	0 = positive data level (S/H mode) 1 = Negative data level (S/H mode) Default = 0	
		9	INPMOD	Input mode select	0 = CDS mode 1 = S/H mode Default = 0	
		10	CLKPOL	Sampling clock polarity change for S/H mode	0 = SHP/SHD negative sampling 1 = SHP/SHD positive sampling Default = 0	
		11	—	Reserved	Fixed at 0 Default = 0	
		12	ExtEn	Clock selection (DLL or external)	0 = DLL CLK provided to system 1 = External CLK provided to system Default = 0	
		13	MonMode	Monitor out enable or disable	0 = No signal appears at the monitor pin 1 = Signal appears at the monitor pin Default = 0	
		15:14	—	Reserved	Fixed at 0 Default = 00b	
1	I/O config	2:0	HdrvAB	RG/H1/H2 pin drive ability select	000b = 3 mA 011b = 1 mA 001b = 2 mA 111b = Hi-Z Default = 001b	Immediate
		3	—	Reserved	Fixed at 0 Default = 0	
		6:4	OutEn_ana	Output buffer drive ability (analog output)	000b = 3 mA 011b = 1 mA 001b = 2 mA 111b = Hi-Z Default = 001b	
		7	—	—	Fixed at 0 Default = 0	
		10:8	OutEn_dig	Output buffer drive ability (digital output)	000b = 3 mA 011b = 1 mA 001b = 2 mA 111b = Hi-Z Default = 001b	
		15:11	—	Reserved	Fixed at 0 Default = 00000b	
2	OB_level0_A	11:0	OB level 0-A	—	OB level is limited as 1536 to 3072 (LSB) Default = 1000 0000 0000b	Immediate
		15:12	—	Reserved	Fixed at 0 Default = 0000b	
3	OB level0_B	11:0	OB level 0-B	—	OB level is limited as 1536 to 3072 (LSB) Default = 1000 0000 0000b	Immediate
		15:12	—	Reserved	Fixed at 0 Default = 0000b	

Table 2. Register Definitions (continued)

ADDRESS	REGISTER	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
4–7	—	—	—	Reserved	Fixed at 0	Immediate
8	DAC1	7:0	—	Universal DAC 1 level	Universal DAC 1 level = 256 steps Default = 0000 0000b	Immediate
		8	—	Universal DAC 1 on/off	0 = On 1 = Off Default = 0	
		15:9	—	Reserved	Fixed at 0 Default = 000 0000b	
9	DAC2	7:0	—	Universal DAC 2 level	Universal DAC 2 level = 256 steps Default = 0000 0000b	Immediate
		8	—	Universal DAC 2 on/off	0 = On 1 = Off Default = 0	
		15:9	—	Reserved	Fixed at 0 Default = 000 0000b	
10	—	—	—	Reserved	Fixed at 0	Register update
11	Analog Gain	2:0	Gain	Analog gain selection	000b = 0 dB 100b = 12 dB 001b = 3 dB 101b = 15 dB 010b = 6 dB 110b = 18 dB 011b = 9 dB 111b = –3 dB Default = 000b	Immediate
		15:3	—	Reserved	Fixed at 0 Default = 0 0000 0000 0000b	
12	OB_loop	1:0	OBFIL	—	00 = No filter 01 = 1st-order 10 = 2nd-order Default = 00b	Immediate
		2	—	Reserved	Fixed at 0 Default = 0	
		3	Shrink_OB	—	0 = Shrink OB period 1 = OB period not shrunk Default = 0	
		7:4	—	Reserved	Fixed at 0 Default = 0000b	
		12:8	HPIX level	—	Rejection level (LSB) = (hpix level + 1) × 128 Default = 11111b	
		13	HPIX enable	—	0 = Disabled 1 = Enable hot pixel rejection Default = 0	
		15:14	—	Reserved	Fixed at 0 Default = 00b	

Table 2. Register Definitions (continued)

ADDRESS	REGISTER	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
13	H-TG skip SHPD	1:0	SKIP_MODE	Skip SHP/SHD/RG	0 = No skips 1 = 2 skips 2 = 4 skips Default = 00b	Immediate
		3:2	—	Reserved	Fixed at 0 Default = 00b	
		5:4	SKIP_DELAY	—	00 = 1 clock delay 11 = 3 clock delay 01 = 2 clock delay 10 = 4 clock delay Default = 00b	
		7:6	—	Reserved	Fixed at 0 Default = 00b	
		8	SKIP_STOP [OB]	Inactive skip mode during CLPOB	0 = Skip during OB period 1 = Do not skip during OB period Default = 1	
		9	SKIP_STOP [DM]	Inactive skip mode during CLPDM	0 = Skip during DM period 1 = Do not skip during DM period Default = 1	
		11:10	—	Reserved	Fixed at 0 Default = 00b	
		12	En_TG	H-TG enable	0 = stop (mask) H1/H2/RG 1 = TG (mask circuit) active Default = 0	
		15:13	—	Reserved	Fixed at 0 Default = 000b	
14	SHP_A	4:0	SHPA fall	DLL tap select (1)	D4 = 0, TFP = t_{MCKP}13/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TFP = t_{MCKP}13/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		7:5	—	Reserved	Fixed at 0 Default = 000b	
		12:8	SHPA rise	DLL tap select	D12 = 0, TRP = t_{MCKP}26/64 + D[11:8] × t_{MCKP}/64 D12 = 1, TRP = t_{MCKP}26/64 + (16 – D[11:8]) × t_{MCKP}/64 Default = 00000b	
		15:13	—	Reserved	Fixed at 0 Default = 000b	
15	SHD_A	4:0	SHDA fall	DLL tap select	D4 = 0, TFD = t_{MCKP}27/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TFD = t_{MCKP}27/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		7:5	—	Reserved	Fixed at 0 Default = 000b	
		12:8	SHDA rise	DLL tap select	D12 = 0, TRD = t_{MCKP}58/64 + D[11:8] × t_{MCKP}/64 D12 = 1, TRD = t_{MCKP}58/64 + (16 – D[11:8]) × t_{MCKP}/64 Default = 00000b	
		15:13	—	Reserved	Fixed at 0 Default = 000b	
16	H1_A	4:0	H1A fall	DLL tap select	D4 = 0, TFH1 = t_{MCKP}32/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TFH1 = t_{MCKP}32/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		7:5	—	Reserved	Fixed at 0 Default = 000b	
		12:8	H1A rise	DLL tap select	D12 = 0, TRH1 = 0 + D[11:8] × t_{MCKP}/64 D12 = 1, TRH1 = 0 + (16 – D[11:8]) × t_{MCKP}/64 Default = 00000b	
		15:13	—	Reserved	Fixed at 0 Default = 000b	

(1) DLL tap selection uses a binary twos complement number. Typ = 00000b, min = 10000b, and max = 01111b.

Table 2. Register Definitions (continued)

ADDRESS	REGISTER	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
17	H2_A	4:0	H2A fall	DLL tap select	D4 = 0, TFH2 = 0 + D[3:0] × t_{MCKP}/64 D4 = 1, TFH2 = 0 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		7:5	—	Reserved	Fixed at 0 Default = 000b	
		12:8	H2A rise	DLL tap select	D12 = 0, TRH2 = t_{MCKP}32/64 + D[11:8] × t_{MCKP}/64 D12 = 1, TRH2 = t_{MCKP}32/64 + (16 – D[11:8]) × t_{MCKP}/64 Default = 00000b	
		15:13	—	Reserved	Fixed at 0 Default = 000b	
18	LH_A	4:0	LH A fall	DLL tap select	D4 = 0, TFLH = t_{MCKP}32/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TFLH = t_{MCKP}32/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		7:5	—	Reserved	Fixed at 0 Default = 000b	
		12:8	LH A rise	DLL tap select	D12 = 0, TRLH = 0 + D[11:8] × t_{MCKP}/64 D12 = 1, TRLH = 0 + (16 – D[11:8]) × t_{MCKP}/64 Default = 00000b	
		15:13	—	Reserved	Fixed at 0 Default = 000b	
19	RG_A	4:0	RGA fall	DLL tap select	D4 = 0, TWR = t_{MCKP}20/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TWR = t_{MCKP}20/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		15:5	—	Reserved	Fixed at 0 Default = 000 0000 0000b	
20	SHP_B	4:0	SHPB fall	DLL tap select	D4 = 0, TFP = t_{MCKP}13/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TFP = t_{MCKP}13/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		7:5	—	Reserved	Fixed at 0 Default = 000b	
		12:8	SHPB rise	DLL tap select	D12 = 0, TRP = t_{MCKP}26/64 + D[11:8] × t_{MCKP}/64 D12 = 1, TRP = t_{MCKP}26/64 + (16 – D[11:8]) × t_{MCKP}/64 Default = 00000b	
		15:13	—	Reserved	Fixed at 0 Default = 000b	
21	SHD_B	4:0	SHDB fall	DLL tap select	D4 = 0, TFD = t_{MCKP}27/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TFD = t_{MCKP}27/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		7:5	—	Reserved	Fixed at 0 Default = 000b	
		12:8	SHDB rise	DLL tap select	D12 = 0, TRD = t_{MCKP}58/64 + D[11:8] × t_{MCKP}/64 D12 = 1, TRD = t_{MCKP}58/64 + (16 – D[11:8]) × t_{MCKP}/64 Default = 00000b	
		15:13	—	Reserved	Fixed at 0 Default = 000b	
22	H1_B	4:0	H1B fall	DLL tap select	D4 = 0, TFH1 = t_{MCKP}32/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TFH1 = t_{MCKP}32/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		7:5	—	Reserved	Fixed at 0 Default = 000b	
		12:8	H1B rise	DLL tap select	D12 = 0, TRH1 = 0 + D[11:8] × t_{MCKP}/64 D12 = 1, TRH1 = 0 + (16 – D[11:8]) × t_{MCKP}/64 Default = 00000b	
		15:13	—	Reserved	Fixed at 0 Default = 000b	

Table 2. Register Definitions (continued)

ADDRESS	REGISTER	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
23	H2_B	4:0	H2B fall	DLL tap select	D4 = 0, TFH2 = 0 + D[3:0] × t_{MCKP}/64 D4 = 1, TFH2 = 0 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		7:5	—	Reserved	Fixed at 0 Default = 000b	
		12:8	H2B rise	DLL tap select	D12 = 0, TRH2 = t_{MCKP}32/64 + D[11:8] × t_{MCKP}/64 D12 = 1, TRH2 = t_{MCKP}32/64 + (16 – D[11:8]) × t_{MCKP}/64 Default = 00000b	
		15:13	—	Reserved	Fixed at 0 Default = 000b	
24	LH_B	4:0	LH B fall	DLL tap select	D4 = 0, TFLH = t_{MCKP}32/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TFLH = t_{MCKP}32/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		7:5	—	Reserved	Fixed at 0 Default = 000b	
		12:8	LH B rise	DLL tap select	D12 = 0, TRLH = 0 + D[11:8] × t_{MCKP}/64 D12 = 1, TRLH = 0 + (16 – D[11:8]) × t_{MCKP}/64 Default = 00000b	
		15:13	—	Reserved	Fixed at 0 Default = 000b	
25	RG_B	4:0	RGB fall	DLL tap select	D4 = 0, TWR = t_{MCKP}20/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TWR = t_{MCKP}20/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		15:5	—	Reserved	Fixed at 0 Default = 000 0000 0000b	
26	2MCLK	4:0	2MCLK rise	DLL tap select	D4 = 0, TRMCLKx2 = t_{MCKP}13/64 + D[3:0] × t_{MCKP}/64 D4 = 1, TRMCLKx2 = t_{MCKP}13/64 + (16 – D[3:0]) × t_{MCKP}/64 Default = 00000b	Register update
		15:5	—	Reserved	Fixed at 0 Default = 000 0000 0000b	
27	LogicCK_A	1:0	LogicCK A rise	LogicCK delay	Effective when sampling clocks are supplied from the DLL Default = 00b	Immediate
		7:2	—	Reserved	Fixed at 0 Default = 00 0000b	
		9:8	LogicCK B rise	LogicCK delay	Effective when sampling clocks are supplied from the DLL Default = 00b	
		15:10	—	Reserved	Fixed at 0 Default = 00 0000b	
28–47	—	—	—	Reserved	Fixed at 0	—

Table 2. Register Definitions (continued)

ADDRESS	REGISTER	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
48	Config	3:0	—	Reserved	Fixed at 0 Default = 0000b	Register update
		4	Muxctrl[0]	—	0 = MUX is disabled (32-bit parallel output) 1 = MUX is active (16-bit parallel output) Default = 0	
		5	—	Reserved	Fixed at 0 Default = 0	
		6	Muxctrl[2]	—	0 = Channel A first (only channel A) 1 = Channel B first (only channel B) Default = 0	
		7	—	Reserved	Fixed at 0 Default = 0	
		8	CTRL_ dgain[0]	Start pixel select to change digital gain	0 = Even pixel start 1 = Odd pixel start Default = 0	
		9	CTRL_ dgain[1]	—	0 = Use only OBlevel0 1 = Change OB level after every second pixel Default = 0	
		10	CTRL_ OBLEV[0]	Start pixel select to change OB level	0 = Even pixel start 1 = Odd pixel start Default = 0	
		11	CTRL_ OBLEV[1]	—	0 = Use only OBlevel0 1 = Change OB level after every second pixel Default = 0	
		15:12	—	Reserved	Fixed at 0 Default = 0000b	
49	OBlevel 1_0_A	11:0	OB level 1_0_A	—	OB level is limited as 1536 to 3072 (LSB) Default = 1000 0000 0000b	Immediate
		15:12	—	Reserved	Fixed at 0 Default = 0000b	
50	OBlevel 1_1_A	11:0	OB level 1_1_A	—	OB level is limited as 1536 to 3072 (LSB) Default = 1000 0000 0000b	Immediate
		15:12	—	Reserved	Fixed at 0 Default = 0000b	
51	OBlevel 1_0_B	11:0	OB level 1_0_B	—	OB level is limited as 1536 to 3072 (LSB) Default = 1000 0000 0000b	Immediate
		15:12	—	Reserved	Fixed at 0 Default = 0000b	
52	OBlevel 1_1_B	11:0	OB level 1_1_B	—	OB level is limited as 1536 to 3072 (LSB) Default = 1000 0000 0000b	Immediate
		15:12	—	Reserved	Fixed at 0 Default = 0000b	
53	dgain0_A	9:0	dgain0	—	Digital gain (dB) = dgain0/32 Default = 00 0000 0000b	Immediate
		15:10	—	Reserved	Fixed at 0 Default = 00 0000b	
54	dgain1_A	9:0	dgain1	—	Digital gain (dB) = dgain1/32 Default = 00 0000 0000b	Immediate
		15:10	—	Reserved	Fixed at 0 Default = 00 0000b	
55	dgain0_B	9:0	dgain0	—	Digital gain (dB) = dgain0/32 Default = 00 0000 0000b	Immediate
		15:10	—	Reserved	Fixed at 0 Default = 00 0000b	
56	dgain1_B	9:0	dgain1	—	Digital gain (dB) = dgain1/32 Default = 00 0000 0000b	Immediate
		15:10	—	Reserved	Fixed at 0 Default = 00 0000b	
57–63	—	—	—	Reserved	Fixed at 0	Immediate

Table 2. Register Definitions (continued)

ADDRESS	REGISTER	BIT	NAME	DESCRIPTION	CIRCUIT OPERATION CONDITION	UPDATE TIMING
64–95	V_{COMP}0-A to V_{COMP}31-A	12:0	V_{COMP}_POS_A	Replaced pixel address for V-compensation	Pixel address (LSB) Default = 0 0000 0000 0000b	Immediate
		14:13	V_{COMP}_rep_A	Replace address	— Default = 00b	
		15	—	Reserved	Fixed at 0 Default = 0	
96–127	V_{COMP}0-B to V_{COMP}31-B	12:0	V_{COMP}_POS_B	Replaced pixel address for V-compensation	Pixel address (LSB) Default = 0 0000 0000 0000b	Immediate
		14:13	V_{COMP}_rep_B	Replace address	— Default = 00b	
		15	—	Reserved	Fixed at 0 Default = 0	
128–255	—	—	—	Reserved	Fixed at 0	Immediate

PACKAGING INFORMATION

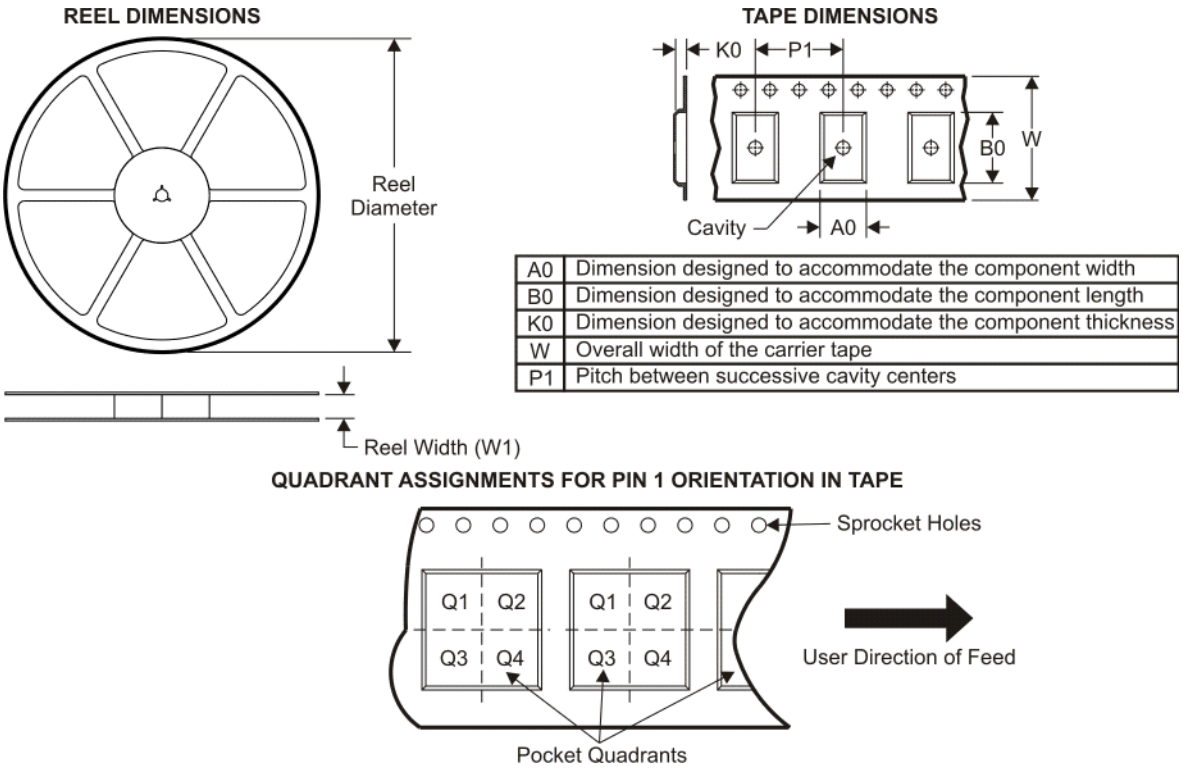
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
VSP2590ZWV	ACTIVE	NFBGA	ZWV	159	348	Pb-Free (RoHS)	SNAGCU	Level-2-260C-1 YEAR
VSP2590ZWVR	ACTIVE	NFBGA	ZWV	159	1000	Pb-Free (RoHS)	SNAGCU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

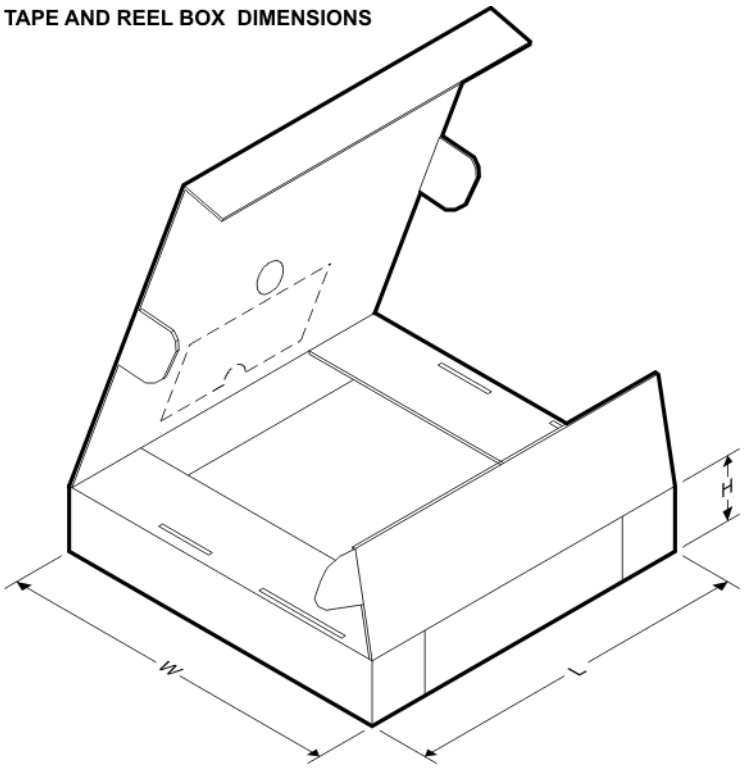


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP2590ZWVR	NFBGA	ZWV	159	1000	330.0	16.4	8.3	8.3	1.85	12.0	16.0	Q1

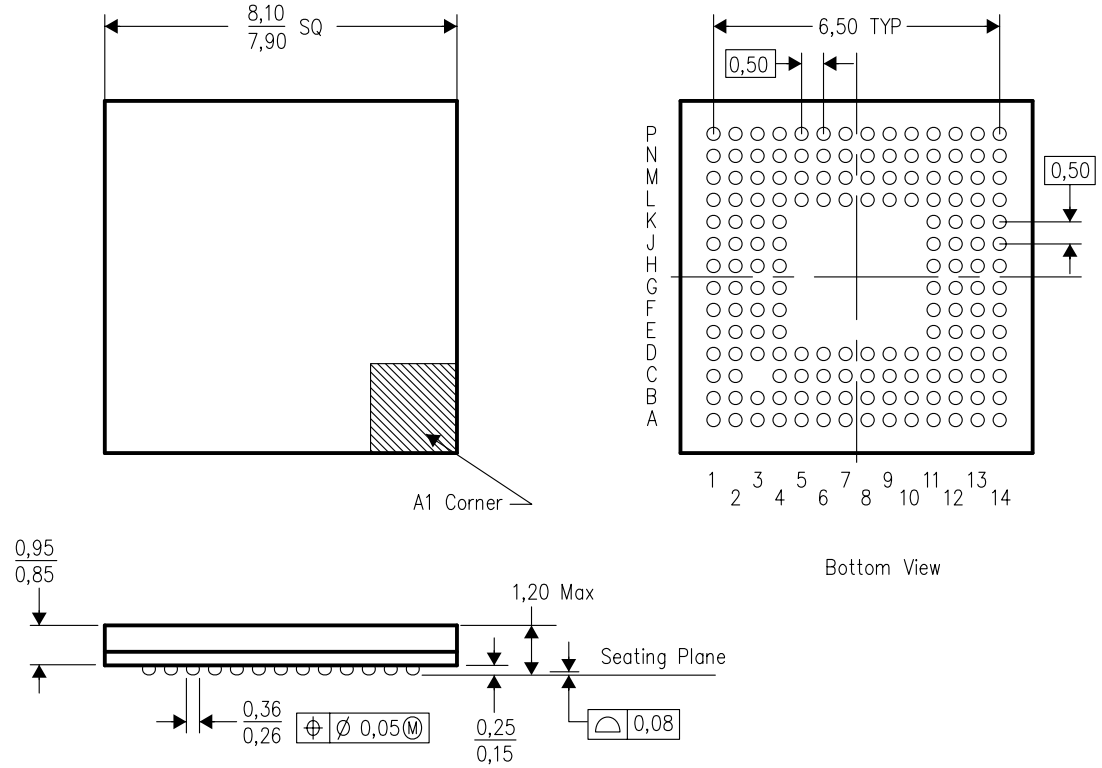
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP2590ZWVR	NFBGA	ZWV	159	1000	342.0	336.0	34.0

ZWV (S–PBGA–N159) PLASTIC BALL GRID ARRAY



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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