TRF1208 10 MHz to 11 GHz 3-dB BW, ADC Driver Amplifier

1 Features

- Superior single-ended to differential conversion performance as ADC driver
- Also works in differential to single-ended mode to work as DAC buffer
- 11 GHz, 3-dB bandwidth
- 8 GHz, 1-dB gain flatness
- Fixed SE to Diff power gain of 16 dB
- OIP3 performance:
  - 37 dBm at 2 GHz
  - 32 dBm at 6 GHz
- P1dB performance:
  - 15 dBm at 2 GHz
  - 12.5 dBm at 6 GHz
- Noise figure:
  - 7 dB at 2 GHz
  - 7 dB at 8 GHz
- Gain and phase imbalance: ±0.3 dB / ±3 degrees
- Power-down feature
- 3.3 V single-supply operation
- Active current: 138 mA

2 Applications

- Directly drives RF sampling or Gsps ADCs
- Suitable for aerospace and defense applications with up to X-band support
- High linearity to support next generation 5G systems
- Low noise figure for better signal integrity
- Reduced system size with small foot print and elimination of passive RF balun
- Low power, power-down mode with digital PD control for optimized system design
- Phased array radar
- Military radios
- High-speed digitizer
- 4G/5G wireless BTS
- RF active balun
- Test and measurement

3 Description

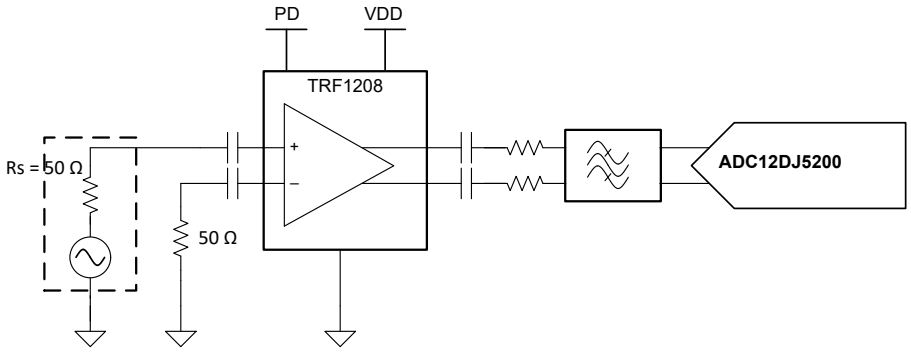
The TRF1208 is a very high performance, RF Amplifier optimized for radio frequency (RF) applications. This device is ideal for ac-coupled applications that require a single-ended to differential conversion when driving an analog-to-digital converter (ADC) such as the high performance ADC12DJ5200RF. The on-chip matching components simplify printed circuit board (PCB) implementation and provide the highest performance over the usable bandwidth. The device is fabricated in Texas Instruments' advanced complementary BiCMOS process and is available in a space-saving, WQFN-FCRLF package.

It operates on a single-rail supply and consumes about 138 mA of active current. A power-down feature is also available for power savings.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRF1208	WQFN-FCRLF (12)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TRF1208 Driving a High-Speed ADC

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2022) to Revision B (April 2022)	Page
• Changed *Pin 12* from: *OUTP* to: *OUTM* and *Pin 11* from: *OUTM* to *OUTP*	3
• Updated the *Interfacing with AFE7950 RX* and *Interfacing with AFE7950 TX* figures	16
• Updated the *TRF1208 in Receive Chain with AFE7950* figure	18
• Updated the *TRF1208 in Transmit Chain with AFE7950* figure	20

Changes from Revision * (October 2021) to Revision A (March 2022)	Page
• Changed the status of the document from: *Advanced Information* to: *Production Data*	1

5 Pin Configuration and Functions

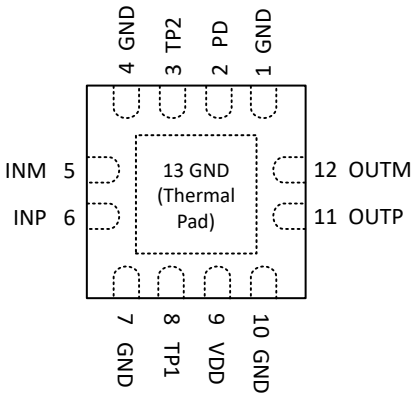


**Figure 5-1. RPV Package,
12-Pin WQFN-FCRLF
(Top View)**

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
GND	1, 4, 7, 10	GND	Ground
INP / INM	6, 5	I	Differential signal input
OUTP / OUTM	11, 12	O	Differential signal output
PD	2	I	Power down signal. Supports 1.8 V and 3.3 V Logic. 0 = Chip Enabled. 1 = Power Down.
TP1	8	—	Test pin. Short to ground.
TP2	3	—	Test pin. Short to ground.
VDD	9	P	3.3 V supply (there is an alternate part, TRF1208A5, that works off 5 V supply).
Thermal pad	13	—	Thermal pad. Connect to ground on board.

(1) I = input, O = output, P = power, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, VDD		–0.3	3.7	V
Input level	INP, INM		20	dBm
	PD	–0.3	3.7	V
Temperature	Junction temperature, T_J	–40	150	ºC
	Storage temperature, Tstg	–40	150	ºC
Continuous power dissipation		See thermal information		

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	3.2	3.3	3.45	V
T_A	Ambient air temperature	–40	25	105	°C
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE	UNIT
		PKG DES (PKG FAM)	
		PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Test conditions are at T_A = 25 °C , V_{DD} = 3.3 V, Single-ended input with R_S = 50 Ω, output with Z_L = 100 Ω differential, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal 3-dB bandwidth	V_o = 0.1 V_{PP}		11		GHz
LSBW	Large-signal 3-dB bandwidth	V_o = 1 V_{PP}		11		GHz
1-dB BW	Bandwidth for 1-dB flatness			8		GHz
S21	Power Gain	f = 2 GHz		16		dB
S11	Input return loss	f = 10 MHz to 8 GHz		–10		dB
S12	Reverse isolation	f = 2 GHz		-35		dB
Imb_{GAIN}	Gain Imbalance	f = 10 MHz to 8 GHz		± 0.3		dB
Imb_{PHASE}	Phase Imbalance	f = 10 MHz to 8 GHz		± 3		degrees
CMRR	CMRR using the formula (S21-S31) / (S21+S31). Port-1: INP, Port-2: OUTP, Port-3: OUTM	f = 2 GHz		-45		dB
HD2	Second-order harmonic distortion	f = 0.5 GHz, P_o = +3 dBm		-70		dBc
		f = 2 GHz, P_o = +3 dBm		-65		dBc
		f = 6 GHz, P_o = +3 dBm		-52		dBc
		f = 8 GHz, P_o = +3 dBm		-45		dBc
HD3	Third-order harmonic distortion	f = 0.5 GHz, P_o = +3 dBm		-68		dBc
		f = 2 GHz, P_o = +3 dBm		-63		dBc
		f = 6 GHz, P_o = +3 dBm		-56		dBc
		f = 8 GHz, P_o = +3 dBm		-63		dBc
IMD2	Second-order intermodulation distortion	f = 0.5 GHz, P_o = -4 dBm per tone (10 MHz spacing)		-73		dBc
		f = 2 GHz, P_o = -4 dBm per tone (10 MHz spacing)		-69		dBc
		f = 6 GHz, P_o = -4 dBm per tone (10 MHz spacing)		-56		dBc
		f = 8 GHz, P_o = -4 dBm per tone (10 MHz spacing)		-45		dBc
IMD3	Third-order intermodulation distortion	f = 0.5 GHz, P_o = -4 dBm per tone (10 MHz spacing)		-75		dBc
		f = 2 GHz, P_o = -4 dBm per tone (10 MHz spacing)		-84		dBc
		f = 6 GHz, P_o = -4 dBm per tone (10 MHz spacing)		-72		dBc
		f = 8 GHz, P_o = -4 dBm per tone (10 MHz spacing)		-51		dBc
OP1dB	Output 1-dB compression point	f = 0.5 GHz		11		dBm
		f = 2 GHz		15		dBm
		f = 6 GHz		12.5		dBm
		f = 8 GHz		7.5		dBm
OIP2	Output second-order intercept point	f = 0.5 GHz, P_o = -4 dBm per tone (10 MHz spacing)		68		dBm
		f = 2 GHz, P_o = -4 dBm per tone (10 MHz spacing)		63		dBm
		f = 6 GHz, P_o = -4 dBm per tone (10 MHz spacing)		55		dBm
		f = 8 GHz, P_o = -4 dBm per tone (10 MHz spacing)		42		dBm

6.5 Electrical Characteristics (continued)

Test conditions are at T_A = 25 °C , V_{DD} = 3.3 V, Single-ended input with R_S = 50 Ω, output with Z_L = 100 Ω differential, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OIP3	Output third-order intercept point	f = 0.5 GHz, P_o = -4 dBm per tone (10 MHz spacing)		34		dBm
		f = 2 GHz, P_o = -4 dBm per tone (10 MHz spacing)		37		dBm
		f = 4 GHz, P_o = -4 dBm per tone (10 MHz spacing)		34		dBm
		f = 6 GHz, P_o = -4 dBm per tone (10 MHz spacing)		30		dBm
		f = 8 GHz, P_o = -4 dBm per tone (10 MHz spacing)		21		dBm
NF	Noise Figure	f = 0.5 GHz		6.5		dB
		f = 2 GHz		6.8		dB
		f = 6 GHz		7.2		dB
		f = 8 GHz		7		dB
IMPEDANCE						
Z_{O-DIFF}	Differential output impedance	f = DC (internal to the device)		3		Ω
Z_{IN}	Single ended input impedance	With INM terminated with 50 Ω		50		Ω
TRANSIENT						
V_{OMAX}	Output max operating range (differential)			2		V_{PP}
V_{OSAT}	Output saturated voltage level (differential)	f = 2 GHz		3.9		V_{PP}
T_{REC}	Over-drive recovery time	Using a -0.5 Vp input pulse of width 2 ns		0.2		ns
POWER SUPPLY						
I_{QA}	Active current	Current on VDD pin, PD = 0		138		mA
I_{QPD}	Power-down quiescent current	Current on VDD pin, PD = 1		7		mA
ENABLE						
V_{PDHIGH}	PD pin logic HIGH		1.45			V
V_{PDLOW}	PD pin logic LOW				0.8	V
I_{PDBIAS}	PD bias current (current on PD pin)	PD = HIGH (1.8 V logic)		50	100	µA
		PD = HIGH (3.3 V logic)		200	250	µA
C_{PD}	PD pin capacitance			2		pF
T_{ON}	Turn_on time	50% V_{PD} to 90% RF		200		ns
T_{OFF}	Turn_off time	50% V_{PD} to 10% RF		50		ns

6.6 Typical Characteristics

Temperature = 25 °C, VDD = 3.3 V, input is 50 Ω single-ended, output is 100 Ω differential unless otherwise specified.

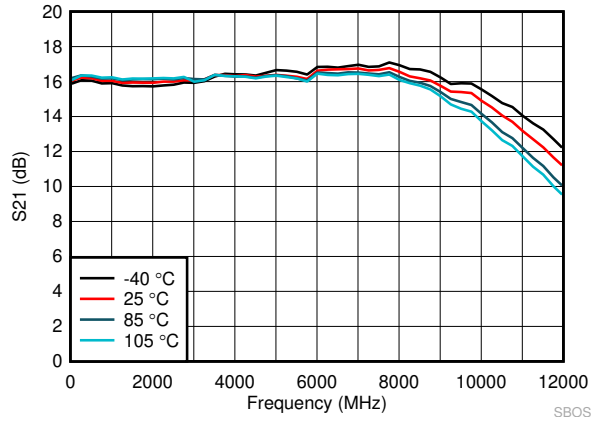


Figure 6-1. Power Gain Across Temperature

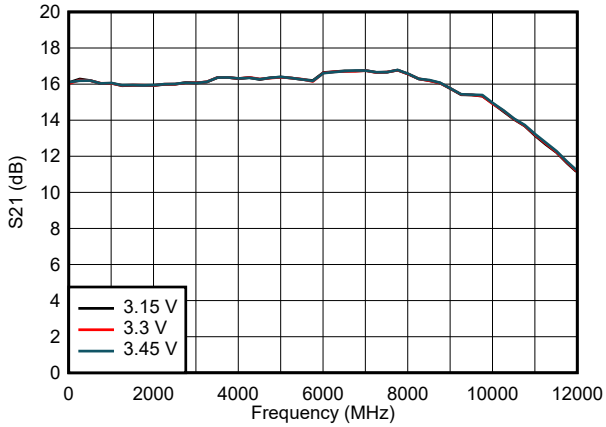


Figure 6-2. Power Gain Across VDD

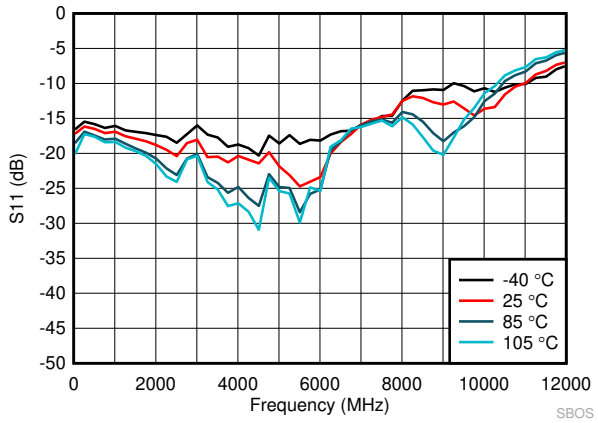


Figure 6-3. Return Loss Across Temperature

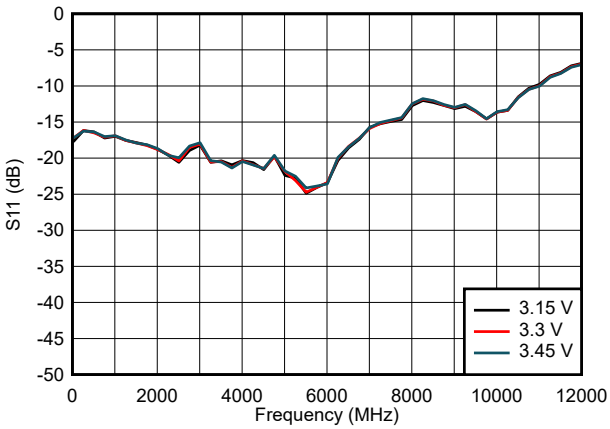


Figure 6-4. Return Loss Across VDD

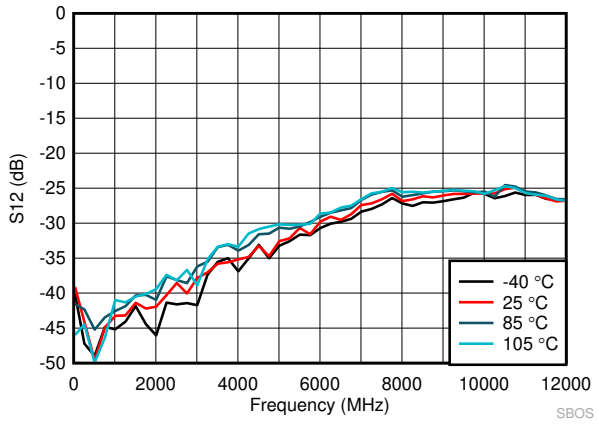


Figure 6-5. Reverse Isolation Across Temperature

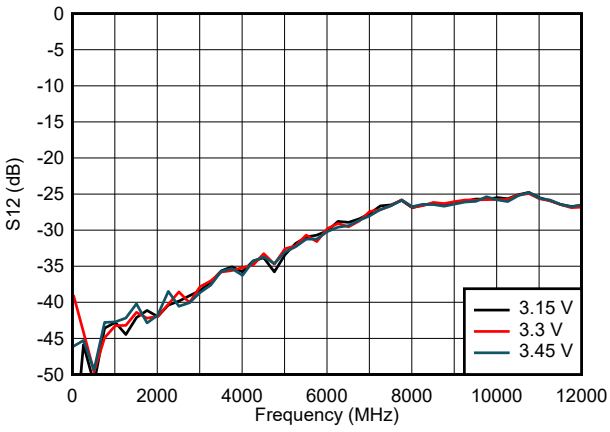
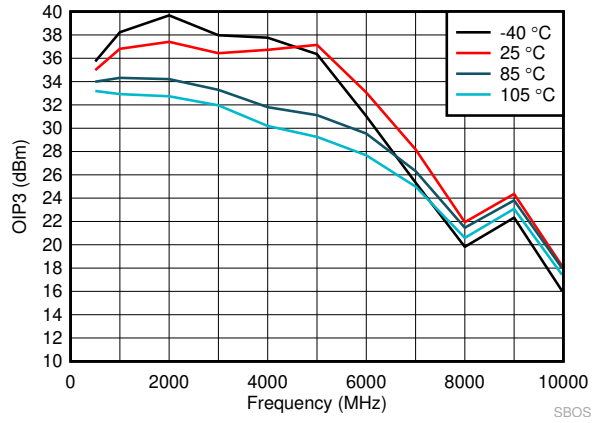


Figure 6-6. Reverse Isolation Across VDD

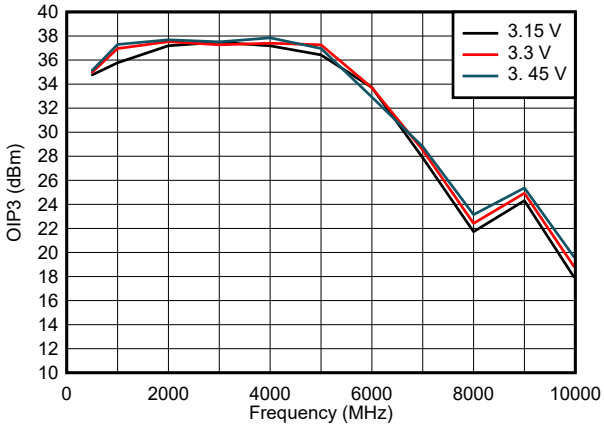
6.6 Typical Characteristics (continued)

Temperature = 25 °C, VDD = 3.3 V, input is 50 Ω single-ended, output is 100 Ω differential unless otherwise specified.



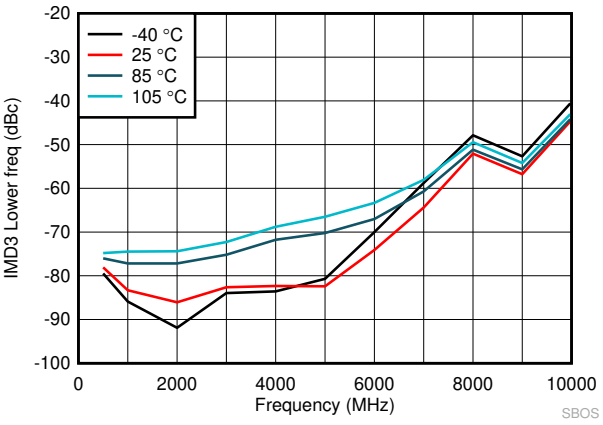
P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-7. OIP3 Across Temperature



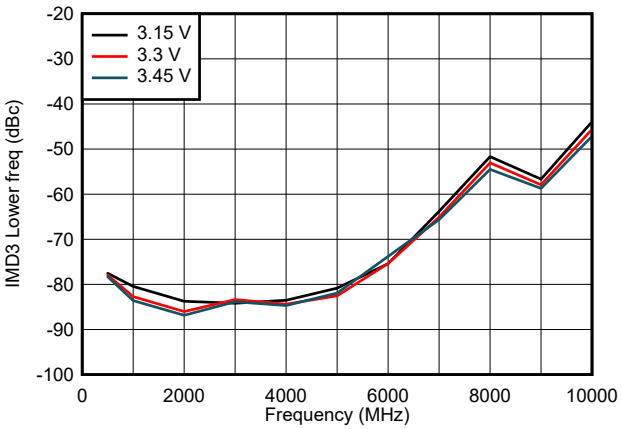
P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-8. OIP3 Across VDD



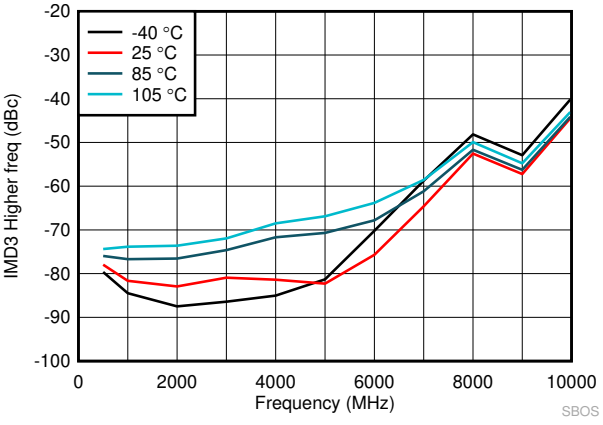
At ($2f_1$-f_2) frequency, $f_1 < f_2$; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-9. IMD3 Lower Across Temperature



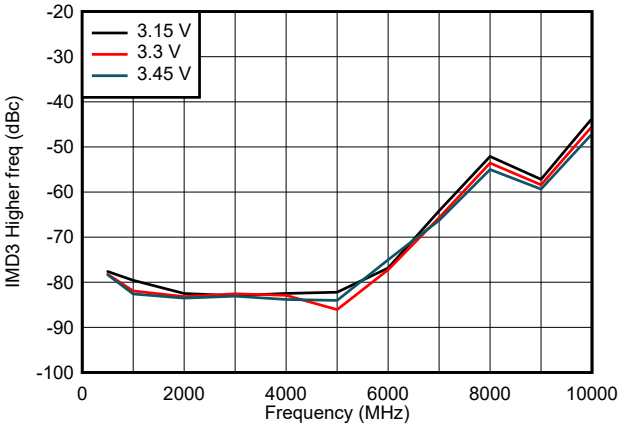
At ($2f_1$-f_2) frequency, $f_1 < f_2$; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-10. IMD3 Lower Across VDD



At ($2f_2$-f_1) frequency, $f_1 < f_2$; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-11. IMD3 Higher Across Temperature

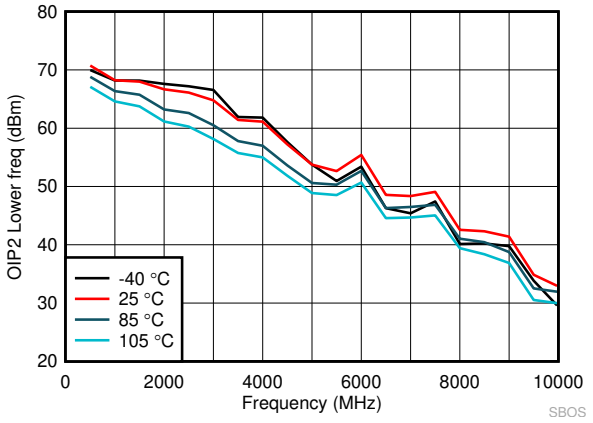


At ($2f_2$-f_1) frequency, $f_1 < f_2$; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-12. IMD3 Higher Across VDD

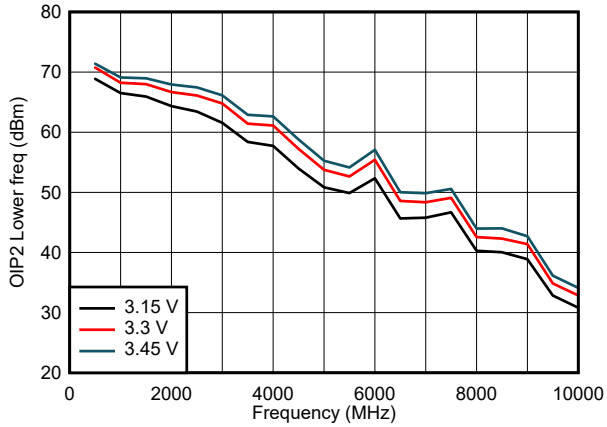
6.6 Typical Characteristics (continued)

Temperature = 25 °C, VDD = 3.3 V, input is 50 Ω single-ended, output is 100 Ω differential unless otherwise specified.



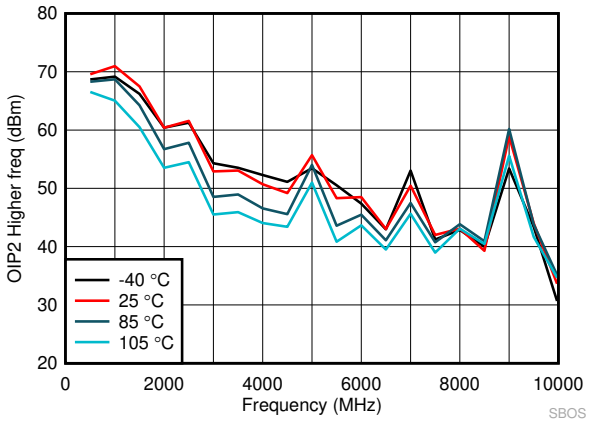
At (f_2-f_1) frequency, $f_2 > f_1$; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-13. OIP2 Lower Across Temperature



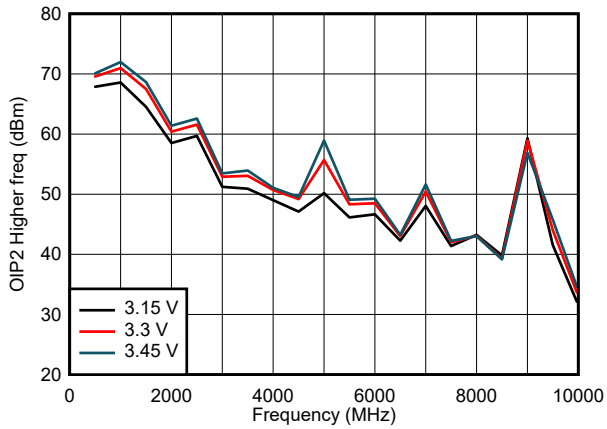
At (f_2-f_1) frequency, $f_2 > f_1$; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-14. OIP2 Lower Across VDD



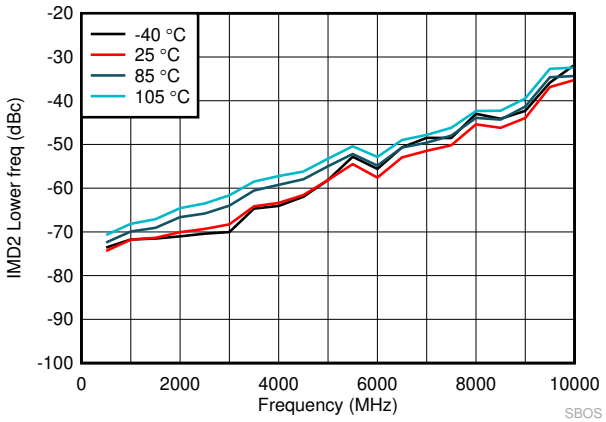
At (f_2+f_1) frequency, $f_2 > f_1$; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-15. OIP2 Higher Across Temperature



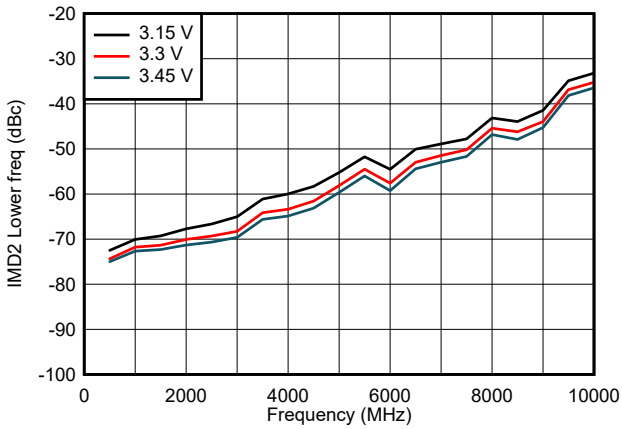
At (f_2+f_1) frequency, $f_2 > f_1$; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-16. OIP2 Higher Across VDD



At (f_2-f_1) frequency, $f_2 > f_1$; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-17. IMD2 Lower Across Temperature

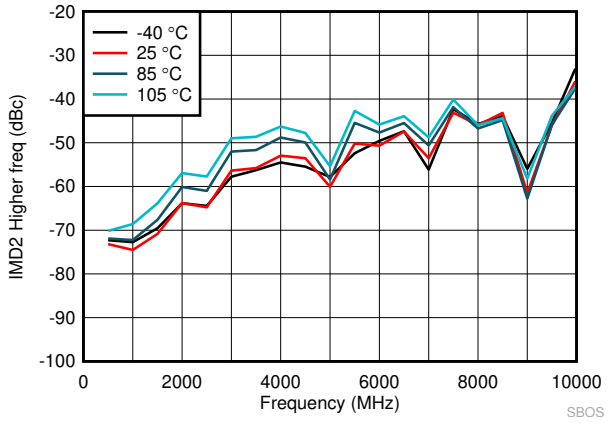


At (f_2-f_1) frequency, $f_2 > f_1$; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-18. IMD2 Lower Across VDD

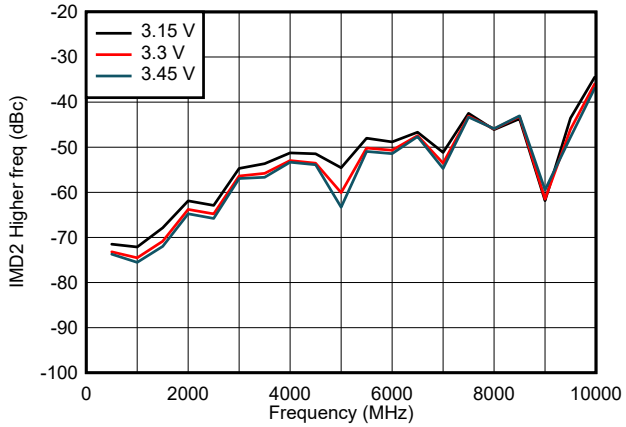
6.6 Typical Characteristics (continued)

Temperature = 25 °C, VDD = 3.3 V, input is 50 Ω single-ended, output is 100 Ω differential unless otherwise specified.



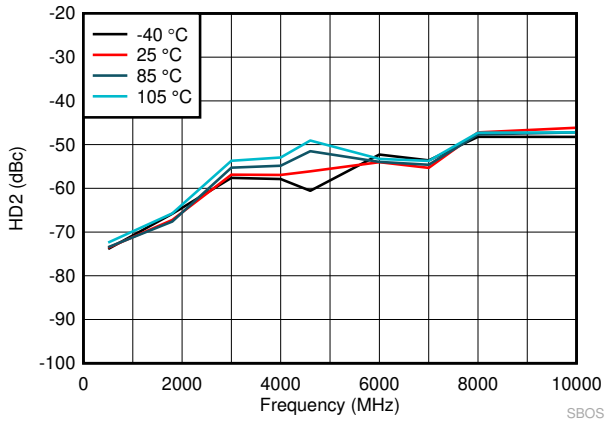
At (f_2+f_1) frequency, f_2 > f_1; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-19. IMD2 Higher Across Temperature



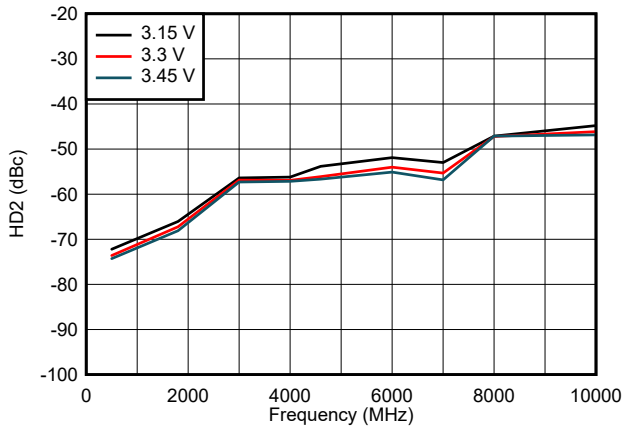
At (f_2+f_1) frequency, f_2 > f_1; P_{out} /tone = -4 dBm, 10 MHz tone spacing

Figure 6-20. IMD2 Higher Across VDD



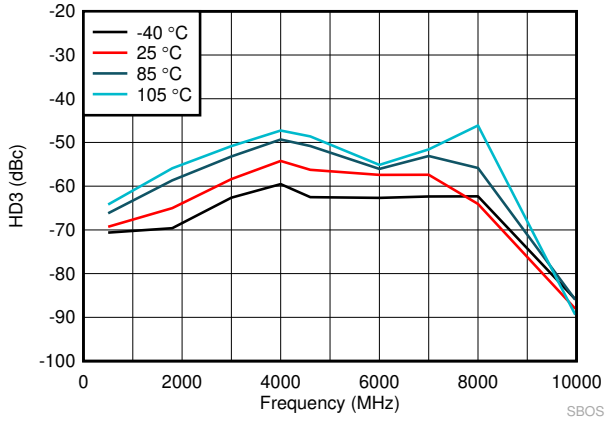
P_{out} = +3 dBm

Figure 6-21. HD2 Across Temperature



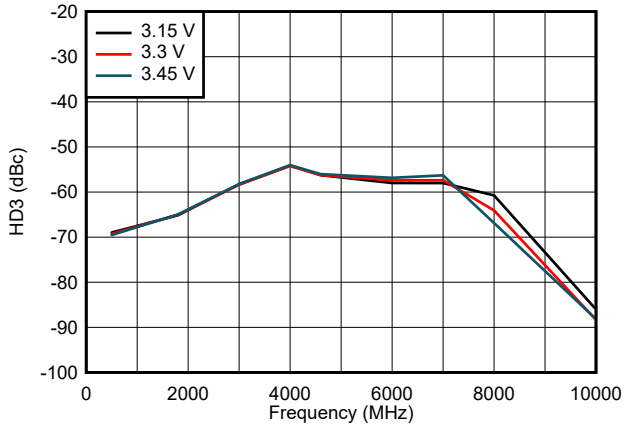
P_{out} = +3 dBm

Figure 6-22. HD2 Across VDD



P_{out} = +3 dBm

Figure 6-23. HD3 Across Temperature



P_{out} = +3 dBm

Figure 6-24. HD3 Across VDD

6.6 Typical Characteristics (continued)

Temperature = 25 °C, VDD = 3.3 V, input is 50 Ω single-ended, output is 100 Ω differential unless otherwise specified.

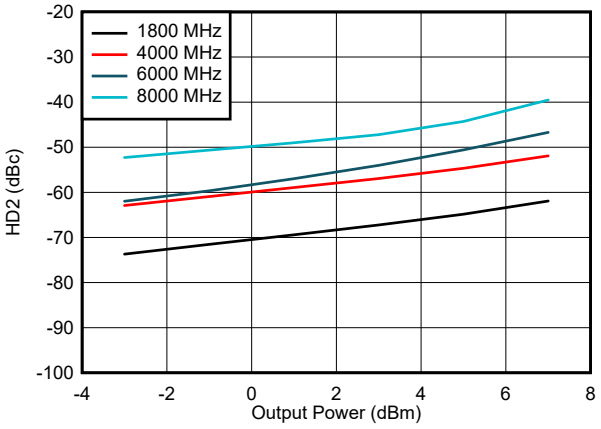


Figure 6-25. HD2 vs Output Power

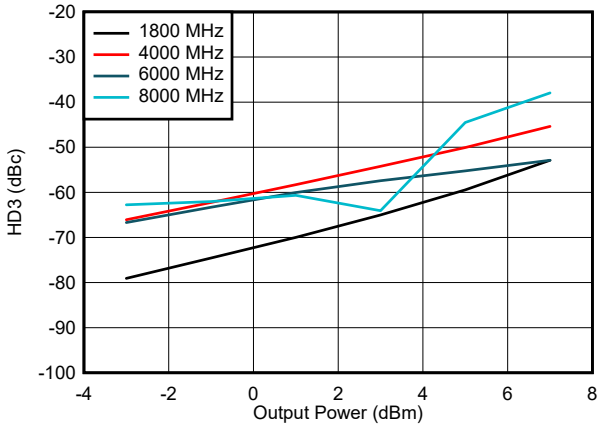


Figure 6-26. HD3 vs Output Power

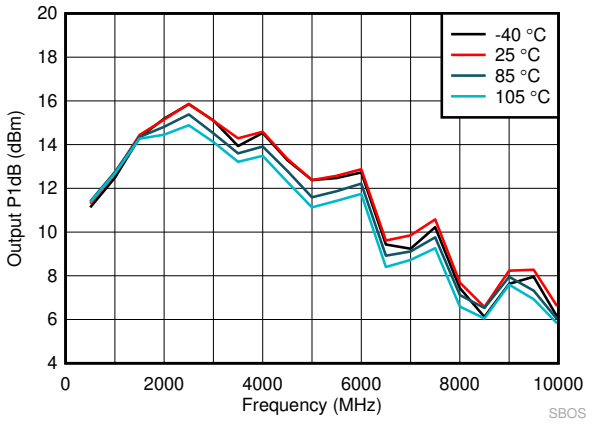


Figure 6-27. Output P1dB Across Temperature

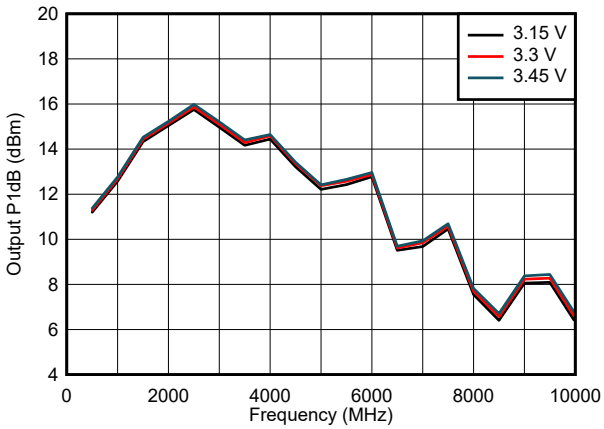


Figure 6-28. Output P1dB Across VDD

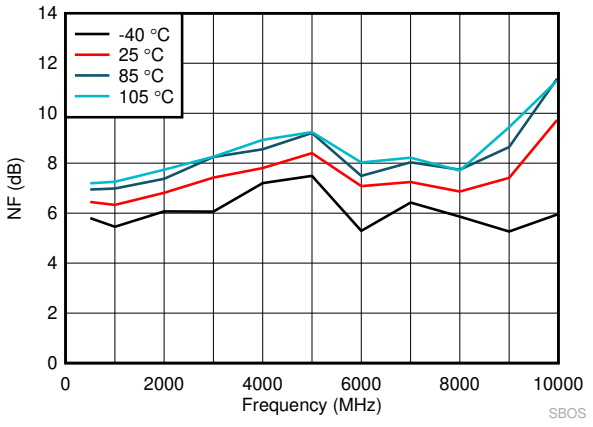


Figure 6-29. NF Across Temperature

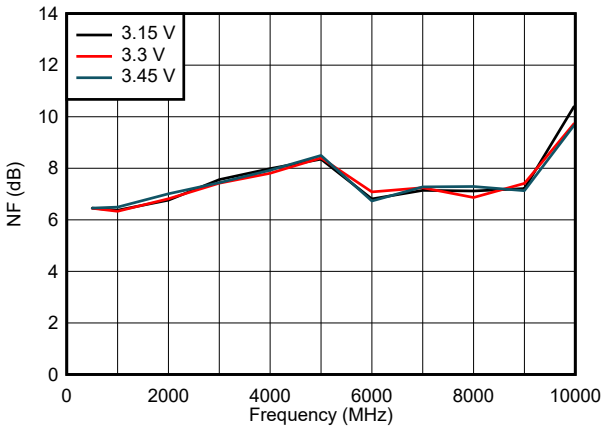


Figure 6-30. NF Across VDD

6.6 Typical Characteristics (continued)

Temperature = 25 °C, VDD = 3.3 V, input is 50 Ω single-ended, output is 100 Ω differential unless otherwise specified.

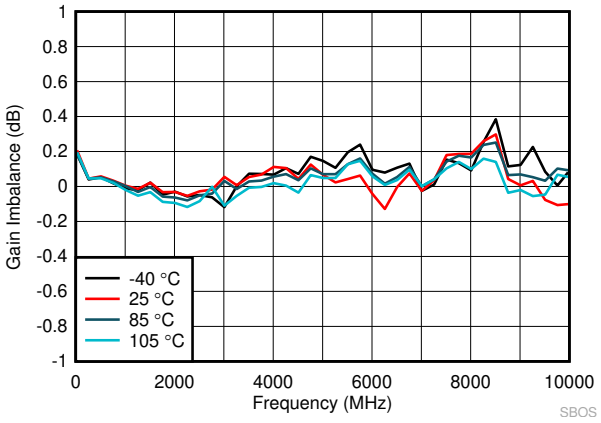


Figure 6-31. Gain Imbalance

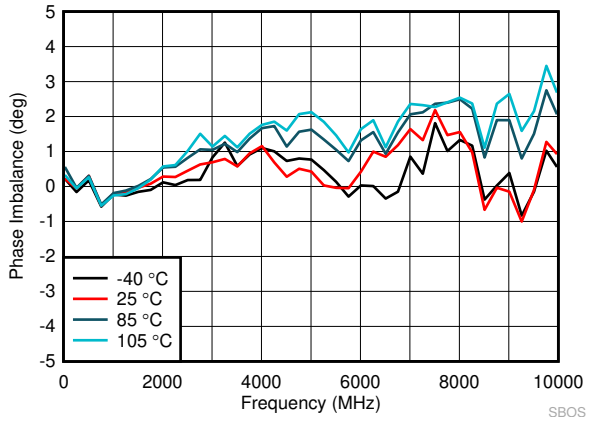


Figure 6-32. Phase Imbalance

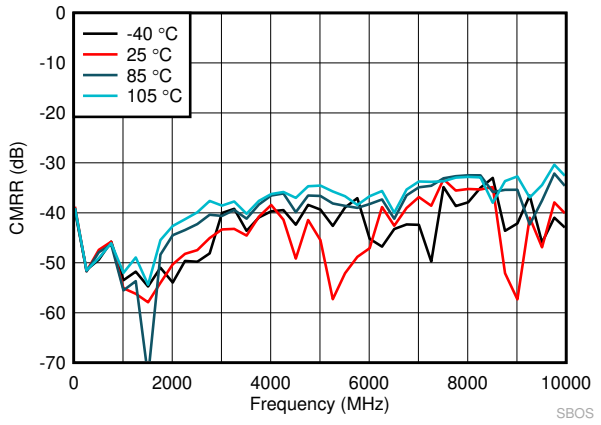


Figure 6-33. CMRR Across Temperature

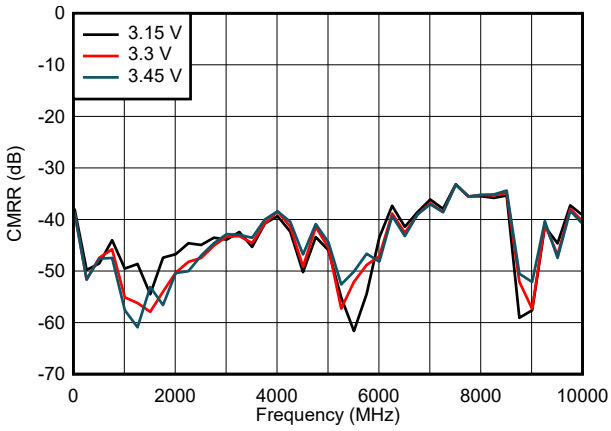
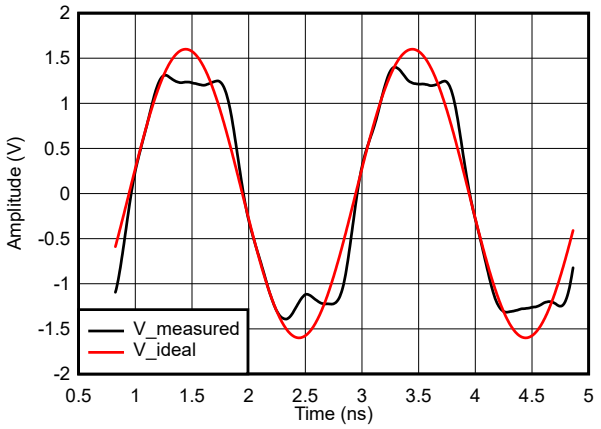
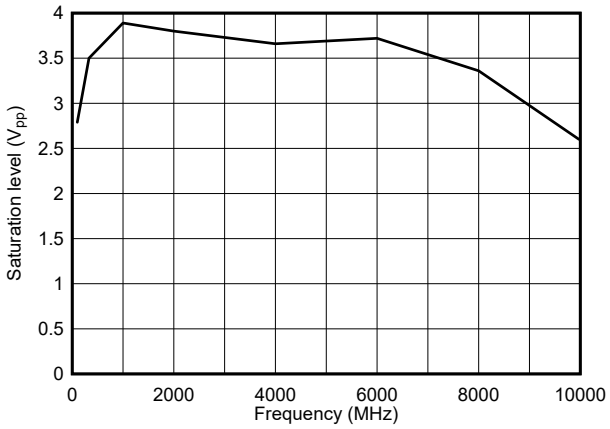


Figure 6-34. CMRR Across VDD



Input = -2 dBm, f = 500 MHz

Figure 6-35. Overdrive Recovery



Input = +6 dBm

Figure 6-36. Saturation Voltage

6.6 Typical Characteristics (continued)

Temperature = 25 °C, VDD = 3.3 V, input is 50 Ω single-ended, output is 100 Ω differential unless otherwise specified.

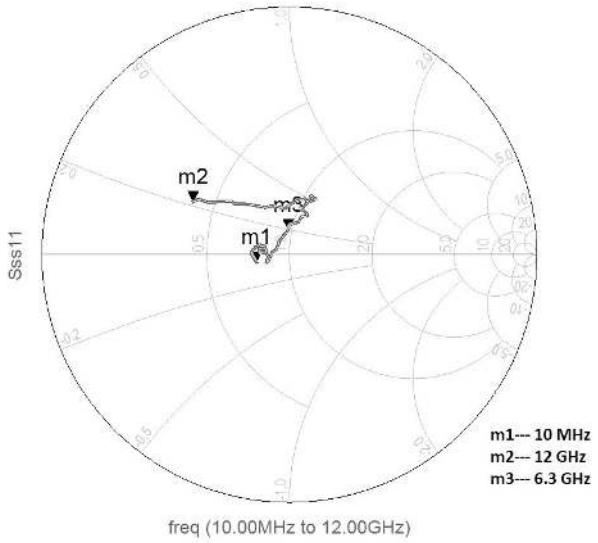


Figure 6-37. Single-Ended S11

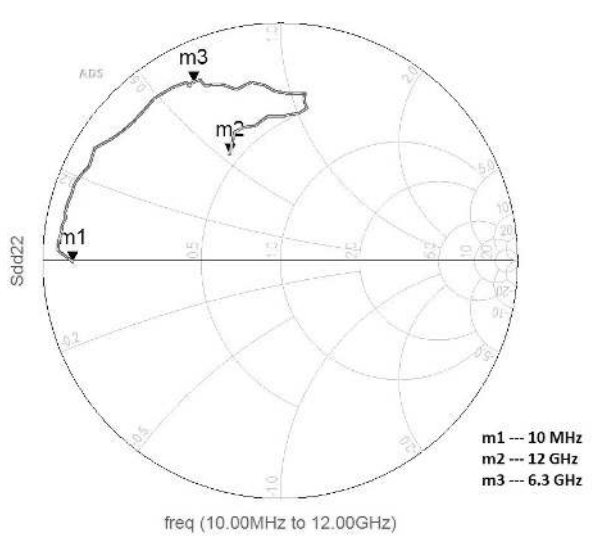


Figure 6-38. Differential S22

7 Detailed Description

7.1 Overview

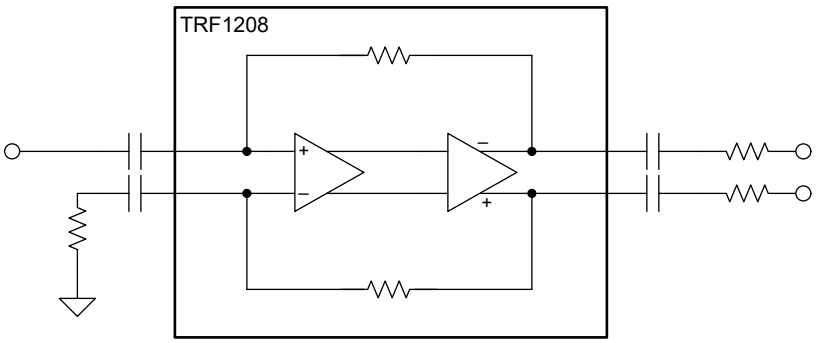
The TRF1208 is a very high-performance amplifier optimized for radio frequency (RF) and intermediate frequency (IF) with signal bandwidths up to 11 GHz. The device is ideal for ac-coupled applications that may require a single-ended to differential conversion when driving an analog-to-digital converter (ADC). The chip has a 2-stage architecture and provides about 16 dB of gain when configured for single-ended inputs driven from a 50-Ω source. This chip can also work as as a Diff-to-SE amplifier to act as a DAC buffer.

This chip does not require any pull up or pull down components on PCB and thereby it simplifies the layout and ensures the highest performance over the whole bandwidth.

The input and output are ac coupled. The chip is powered with 3.3 V supply (TRF1208A5 is an alternate part that works off 5 V supply). A power-down feature is also available for this chip.

7.2 Functional Block Diagram

The following figure shows the functional block diagram of TRF1208. It essentialy has 2-stages with voltage feedback configuration.



7.3 Feature Description

The TRF1208 includes the following features:

- Fully differential amplifier
- Single supply operation
- Power-down option

7.3.1 Fully-Differential Amplifier

The TRF1208 is a voltage feedback fully-differential amplifier (FDA) with fixed gain by architecture. TRF1208 is most suited to be operated as a single-ended to differential amplifier by terminating the INM pin by a 50 Ω resistor and driving the INP pin directly with no external components.

This amplifier has non-linearity cancellation circuits due to which it has excellent linearity performance over a wide range of frequencies.

The output of the amplifier has a low DC impedance. It can be matched to a load if required by adding appropriate series resistors or attenuator pad.

7.3.2 Single Supply Operation

TRF1208 operates on a single 3.3 V supply. The input and output bias voltages are set internally. Therefore, the signal path has to be ac-coupled on the board at all the 4 RF input and output pins. Single supply operation simplifies the board design.

There is also another variant of this chip (TRF1208A5) that operates with 5 V supply instead of 3.3 V.

7.3.3 Power Down Option

There is power-down functionality for this device. The PD pin can be used to power-down the amplifier. This pin supports both 1.8 V and 3.3 V digital logics and is referenced to the GND. A logic 1 turns the device off placing the device into a low quiescent current state.

Note that, when disabled, the signal path is still present through the internal circuits. Input signals applied to a disabled device still appear at the outputs at some lower level through this path as they would for any disabled feedback amplifier.

7.4 Device Functional Modes

TRF1208 has 2 functional modes, namely, Active mode and Power-down mode. The functional modes are controlled by the PD pin as described in the previous section.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Driving a High-Speed ADC

A common application of TRF1208 is to drive a high-speed ADC such as ADC12DJ5200RF or AFE7950 which have differential input. Conventionally passive baluns are used to drive Gsps ADCs due to non-availability of high-BW, linear amplifiers. TRF1208 is an active balun that has excellent bandwidth flatness, gain, and phase imbalance comparable to or exceeding costly passive baluns.

Figure 8-1 shows a typical interface circuit for ADC12DJ5200RF. Depending on the ADC and system requirement, this circuit can be simplified or can be more complex.

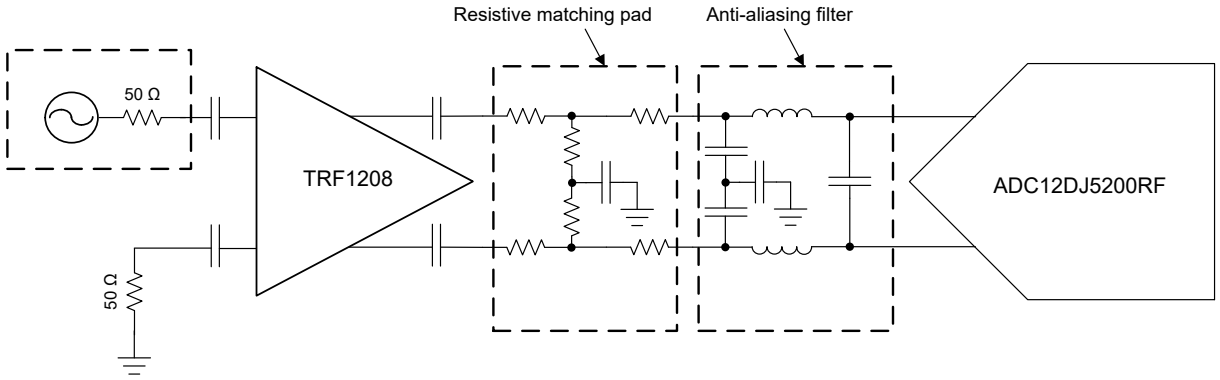
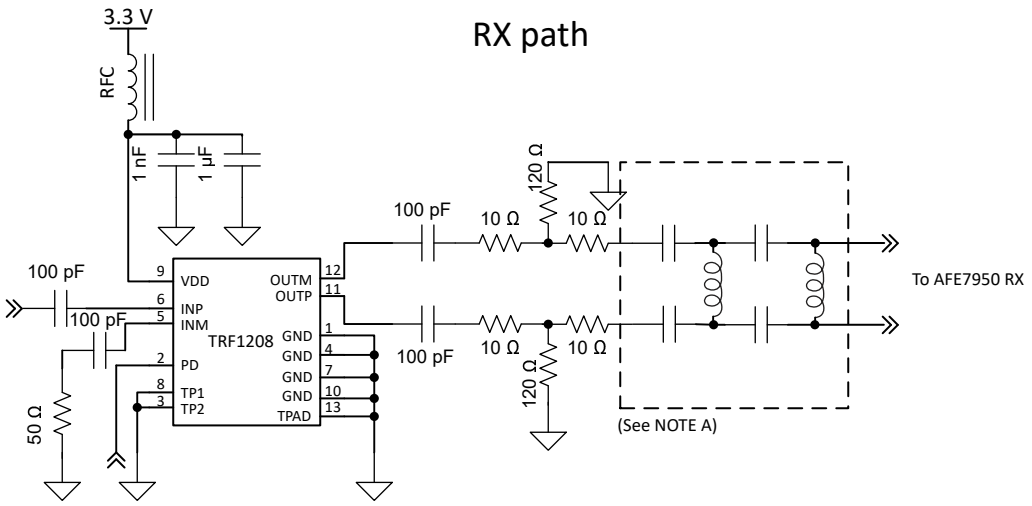


Figure 8-1. Interfacing with ADC12DJ5200RF

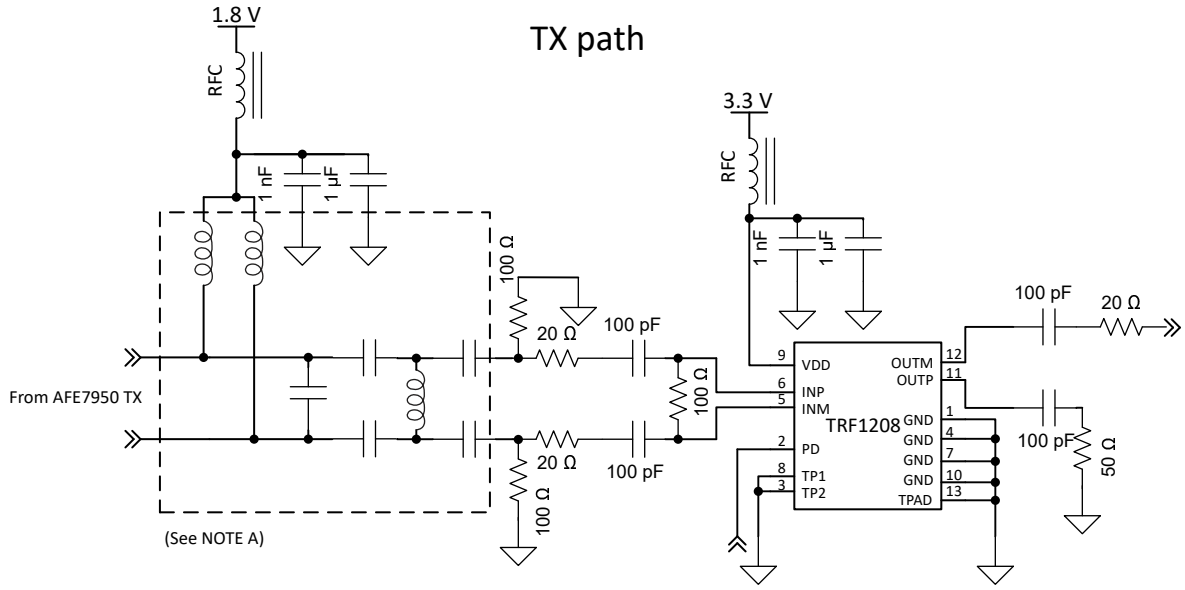
It shows two sections of the circuit between the driver amp and the ADC – namely the matching pad (or attenuator pad) and the anti-aliasing filter. Small form-factor RF quality passive components are recommended for these circuits. The output swing of TRF1208 is well suited to drive these ADCs full-scale at the same time not over-driving it avoiding the need for any voltage limiting device at the ADC.

The following figures show typical interface circuits for AFE7950 RX and TX chains in which TRF1208 is the S2D and D2S amplifier respectively.



A. AFE matching network – component type (whether L or C) and values depend on the channel (A, B, C, D, FB1, FB2) and frequency band

Figure 8-2. Interfacing with AFE7950 RX



A. AFE matching network – component type (whether L or C) and values depend on the channel (A, B, C, D) and frequency band

Figure 8-3. Interfacing with AFE7950 TX

8.1.2 Calculating Output Voltage Swing

This section gives an idea of the output voltage swings for different input power levels as a quick reference. The output is terminated with 100 Ω differential load in this case and power gain of 16 dB is assumed.

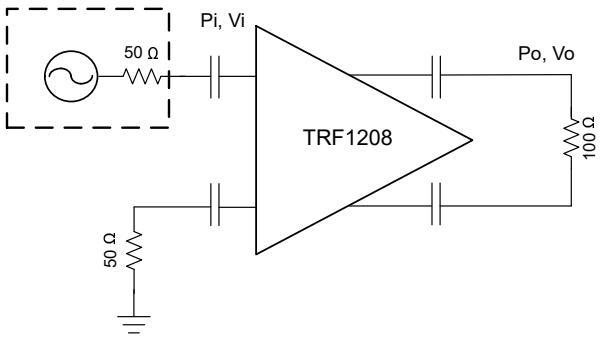


Figure 8-4. Power and Voltage Levels

Voltage gain = 20*log (V_o/V_i)

Power gain = 10*log (P_o/P_i) = 10*log ((V_o ^{2}/100)/(V_i ^{2}/50)) = 20*log (V_o/V_i) - 3 dB (1)

Table 8-1. Output Voltage Swings for Different Input Power Levels

Input		Output	
Pi (dBm)	Vi (Vpp)	Po (dBm)	Vo (Vpp)
-20	0.063	-4	0.564
-15	0.112	1	1.004
-10	0.2	6	1.785
-9	0.224	7	2.002

8.1.3 Thermal Considerations

The TRF1208 is packaged in a 2 mm × 2 mm WQFN-FCRLF package that has excellent thermal properties. The chip has a thermal pad underneath that should be connected to a ground plane. The ground plane should be shorted to the other ground pins of the chip at four corners if possible to allow heat propagation to the top layer of PCB. There should be a thermal via that connects the thermal pad plane on the top layer of the PCB to the inner layer ground planes to allow heat propagation to the inner layers.

The total power dissipation needs to be limited to keep the device junction temperature below 150°C for instantaneous power and below 125°C for continuous power.

8.2 Typical Application

An example of TRF1208 acting as ADC and DAC amplifiers for AFE7950 is explained in this section.

8.2.1 TRF1208 in Receive Chain

This section describes an RF receiver chain in which TRF1208 is working as a S2D (SE-to-diff) amp and driving a receive channel of AFE7950.

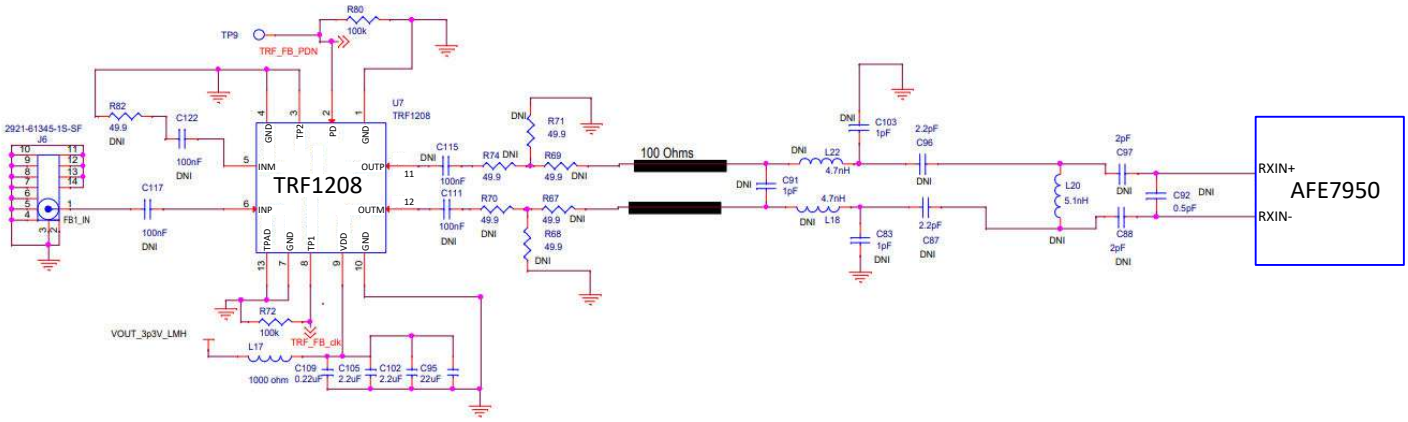


Figure 8-5. TRF1208 in Receive Chain with AFE7950

The previous figure is a generic schematics of a design in which TRF1208 drives an AFE7950 receive channel. The exact values of the components depend on the frequency band for which the AFE7950 front-end is matched.

8.2.1.1 Design Requirements

The AFE7950 channel is required to be matched to 8.2 GHz.

8.2.1.2 Detailed Design Procedure

The TRF1208 is configured as a S2D amplifier. The section close to TRF1208 output is an attenuator pad which is meant for robust matching. The section close to AFE7950 is the matching network for the AFE which is channel dependent. The matching components are chosen based on the AFE return-loss data and some trial and error since the board parameters can influence the exact values

Table 8-2 shows the bill of materials (BOM) values of the design for a channel that is matched to center frequency of 8.2 GHz.

Table 8-2. Component Values of RX Chain with Center Frequency = 8.2 GHz

Section	Designator	Type	Value	Part Number	Install / DNI
DC block cap	C117	cap	100 nF	530L104KT	Install
DC block cap	C115	cap	100 nF	530L104KT	Install
DC block cap	C111	cap	100 nF	530L104KT	Install
DC block cap	C122	cap	100 nF	530L104KT	Install
Attenuator	R74	resistor	10 Ω	ERJ-1GEF10R0C	Install
Attenuator	R70	resistor	10 Ω	ERJ-1GEF10R0C	Install
Attenuator	R69	resistor	10 Ω	ERJ-1GEF10R0C	Install
Attenuator	R67	resistor	10 Ω	ERJ-1GEF10R0C	Install
Attenuator	R71	resistor	140 Ω	ERJ-1GNF1400C	Install
Attenuator	R68	resistor	140 Ω	ERJ-1GNF1400C	Install
INM term	R82	resistor	50 Ω	ERJ-1GEF49R9C	Install
Matching	C91				DNI
Matching	L20				DNI
Matching	C103				DNI
Matching	C83				DNI
Matching	L22	inductor	0.1 nH	LQP03TG0N1B02#	Install
Matching	L18	inductor	0.1 nH	LQP03TG0N1B02#	Install
Matching	C96	inductor	0.1 nH	LQP03TG0N1B02#	Install

Table 8-2. Component Values of RX Chain with Center Frequency = 8.2 GHz (continued)

Section	Designator	Type	Value	Part Number	Install / DNI
Matching	C87	inductor	0.1 nH	LQP03TG0N1B02#	Install
Matching	C97	cap	0.8 pF	02015J0R8PBSTR	Install
Matching	C88	cap	0.8 pF	02015J0R8PBSTR	Install
Matching	C92	inductor	0.3 nH	LQP03TG0N3B02#	Install

8.2.2 TRF1208 in Transmit Chain

This section describes an RF transmit chain in which TRF1208 works as a diff-to-SE converter to convert the DAC output of AFE7950 into a single-ended signal that will drive a PA or a mixer.

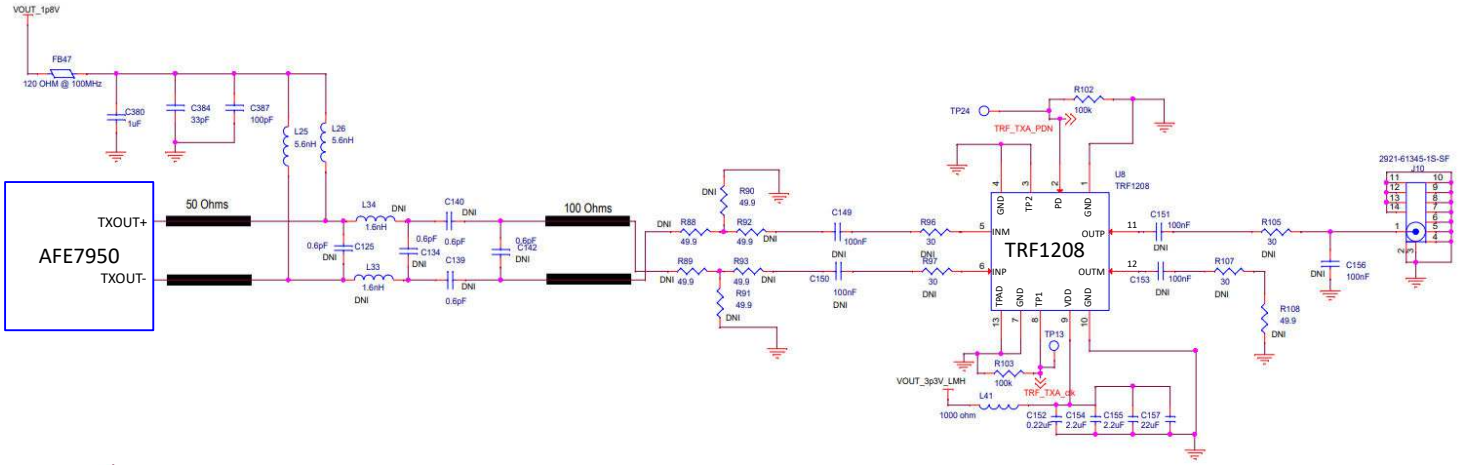


Figure 8-6. TRF1208 in Transmit Chain with AFE7950

The previous figure is a generic schematics of a design in which TRF1208 is used with AFE7950 in the transmit chain. The exact values of the components depend on the frequency band for which the AFE7950 front-end is matched.

8.2.2.1 Design Requirements

The AFE7950 channel is required to be matched to 8.2 GHz.

8.2.2.2 Detailed Design Procedure

The TRF1208 is configured as a D2S amplifier. OUTM pin of TRF1208 is terminated on 50 Ω and OUTP is taken out as the SE output. The section close to TRF1208 input is an attenuator pad which is meant for robust matching. The section close to AFE7950 is the matching network for the AFE which is channel dependent. The matching components are chosen based on the AFE return-loss data and some trial and error since the board parameters can influence the exact values.

Table 8-3 shows the BOM values of the design for a channel that is matched to center frequency of 8.2 GHz.

Table 8-3. Component Values of TX Chain with Center Frequency = 8.2 GHz

Section	Designator	Type	Value	Part Number	Install / DNI
Supply inductor	L25	inductor	2 nH	LQP03TG2N0B02#	Install
Supply inductor	L26	inductor	2 nH	LQP03TG2N0B02#	Install
Matching	C125				DNI
Matching	C142				DNI
Matching	C156				DNI
Matching	L34	capacitor	0.7 pF	02015J0R7PBSTR	Install
Matching	L33	capacitor	0.7 pF	02015J0R7PBSTR	Install

Table 8-3. Component Values of TX Chain with Center Frequency = 8.2 GHz (continued)

Section	Designator	Type	Value	Part Number	Install / DNI
Matching	C134	inductor	0.5 nH	LQP03TG0N5B02#	Install
Matching	C140	inductor	0.1 nH	LQP03TG0N1B02#	Install
Matching	C139	inductor	0.1 nH	LQP03TG0N1B02#	Install
DC block cap	C149	capacitor	100 nF	530L104KT	Install
DC block cap	C150	capacitor	100 nF	530L104KT	Install
DC block cap	C151	capacitor	100 nF	530L104KT	Install
DC block cap	C153	capacitor	100 nF	530L104KT	Install
Attenuator	R88	resistor	20 Ω	ERJ-1GNF20R0C	Install
Attenuator	R89	resistor	20 Ω	ERJ-1GNF20R0C	Install
Attenuator	R92	resistor	20 Ω	ERJ-1GNF20R0C	Install
Attenuator	R93	resistor	20 Ω	ERJ-1GNF20R0C	Install
Attenuator	R90	resistor	57.6 Ω	ERJ-1GNF57R6C	Install
Attenuator	R91	resistor	57.6 Ω	ERJ-1GNF57R6C	Install
Term	R105	resistor	0 Ω	ERJ-1GN0R00C	Install
Term	R107	resistor	0 Ω	ERJ-1GN0R00C	Install
Term	R96	resistor	10 Ω	ERJ-1GEF10R0C	Install
Term	R97	resistor	10 Ω	ERJ-1GEF10R0C	Install
Term	R108	resistor	50 Ω	ERJ-1GEF49R9C	Install

9 Power Supply Recommendations

TRF1208 requires a single 3.3 V supply. Supply decoupling is critical to high-frequency performance. Typically 2 or 3 capacitors are used for supply decoupling. The lowest-value capacitor should be a small form-factor component that is placed closest to the VDD pin of the device. There should be bulk decoupling capacitor that is of bigger value and size which can be placed next to the small capacitor. Additional layout recommendations are given in the Layout section.

10 Layout

10.1 Layout Guidelines

TRF1208 is a wide-band feedback amplifer with about 16 dB of gain. When designing with a wide-band RF amplifier with relatively high gain, certain board layout precautions must be taken to ensure stability and optimum performance. TI recommends that the board be multi-layered to maintain signal and power integrity and thermal performance. Figure 10-1 shows an example of a good layout. In this figure, only the top layer is shown.

The RF input and output lines are recommended to be routed as grounded coplanar waveguide (GCPW) lines. The second layer should be continuous ground layer without any ground-cuts near the amplifier area. The output differential lines have to be matched in length to minimize phase imbalance. Use small footprint passive components wherever possible. Care should be given also for the input side layout. The INP routing should be 50-ohm line and the termination on INM pin should have low parasitics by placing the ac-coupling cap and the 50 Ω resistor very close to the device. Use a RF quality 50 Ω resistor for termination. Ensure that ground planes on the top and internal layers are well stitched with vias.

Place thermal via under the device that connects the top thermal pad with ground planes in the inner layers of PCB. Also connect the thermal pad to the top layer ground plane through the ground pins as shown in the figure for improved heat dissipation.

10.2 Layout Example

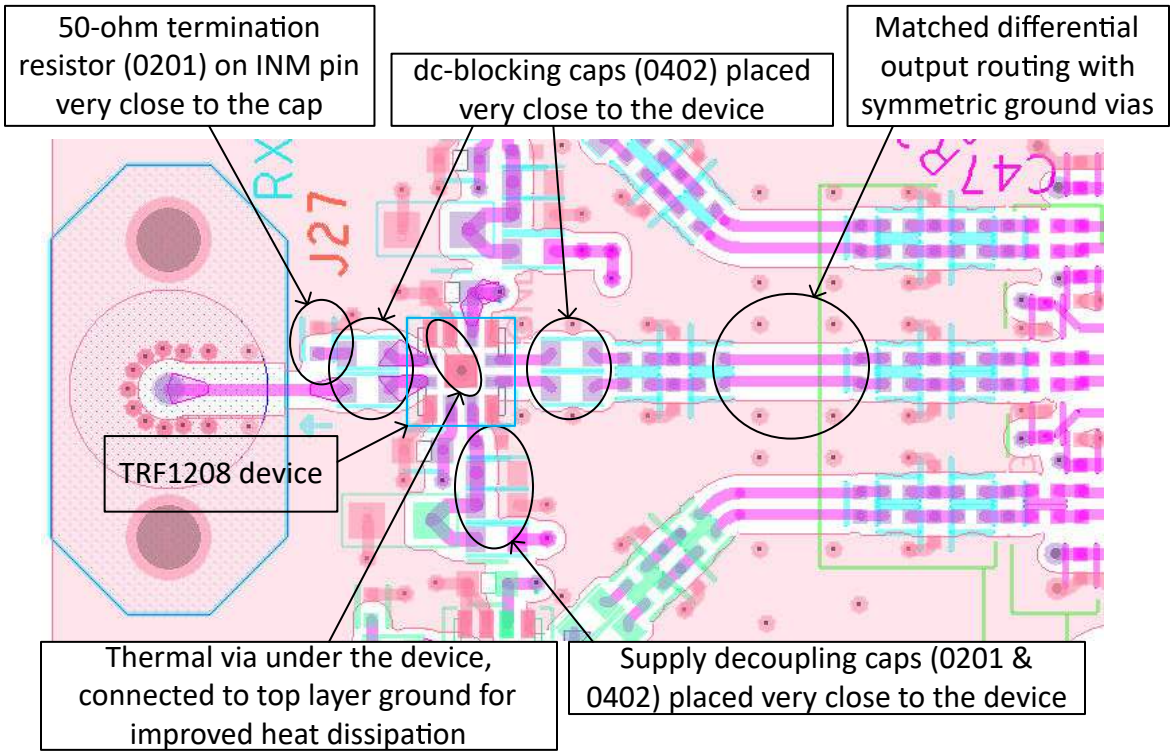


Figure 10-1. Layout Example – Placement and Top Layer Layout

The TRF1208 device can be evaluated using the TRF1208 EVM board, which can be ordered from TRF1208 product folder. Additional information about the evaluation board construction and test setup is given in the *TRF1208 EVM* User's Guide.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TRF1208 EVM User's Guide*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF1208RPVR	ACTIVE	WQFN-HR	RPV	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1208	Samples
TRF1208RPVT	ACTIVE	WQFN-HR	RPV	12	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1208	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

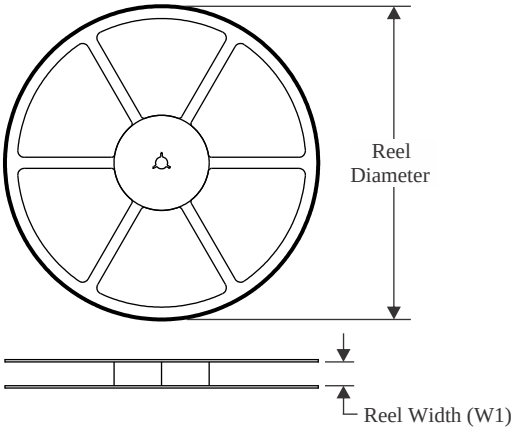
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

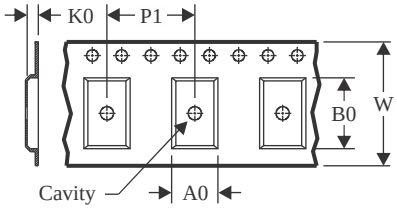
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

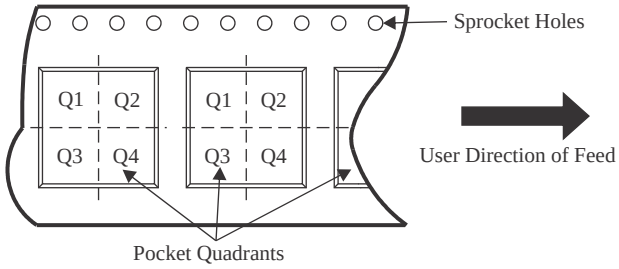


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

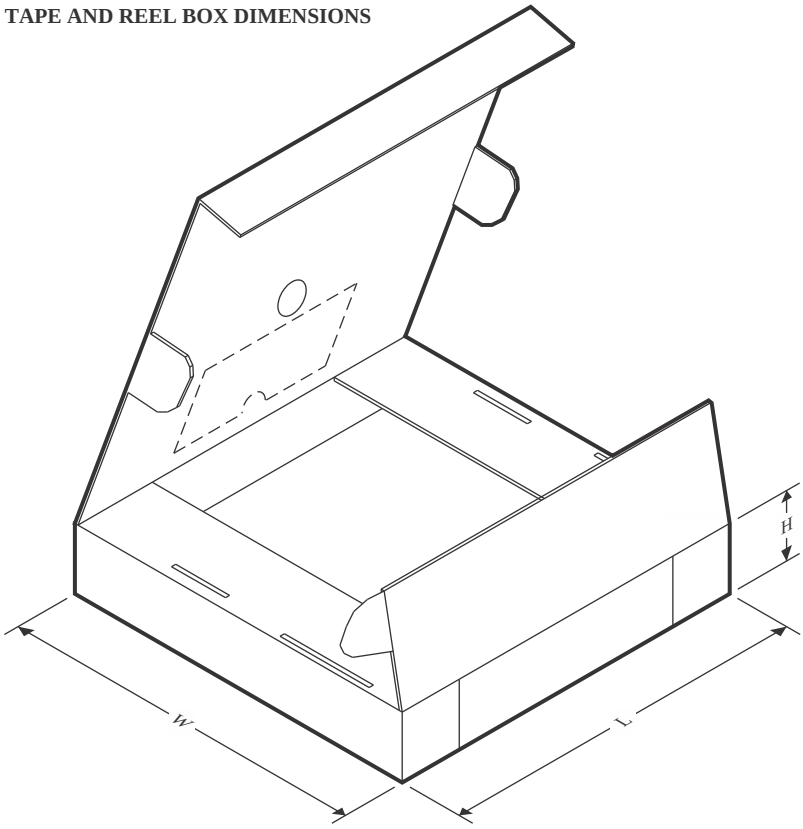
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1208RPVR	WQFN-HR	RPV	12	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q1
TRF1208RPVT	WQFN-HR	RPV	12	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

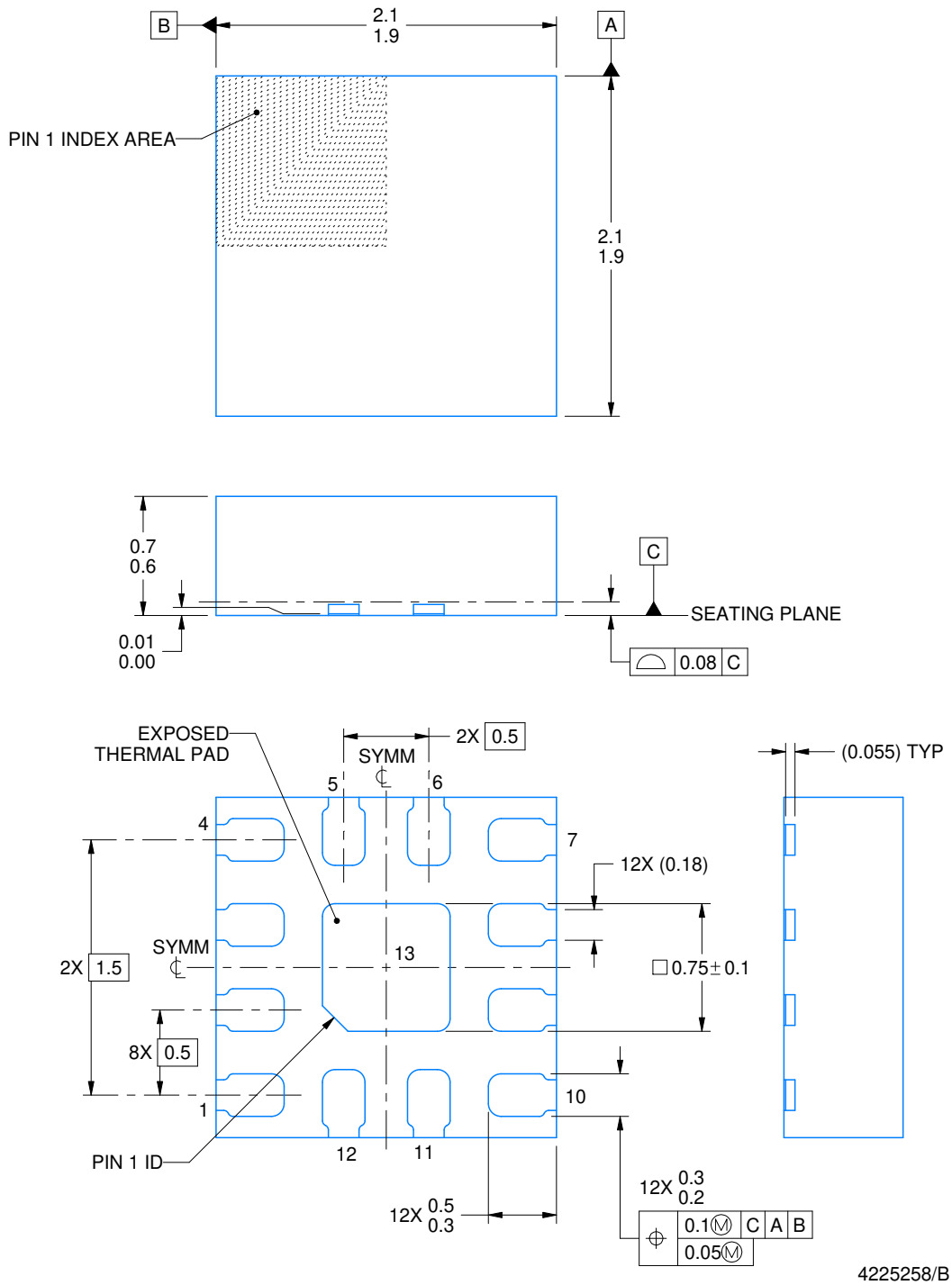
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1208RPVR	WQFN-HR	RPV	12	3000	205.0	200.0	33.0
TRF1208RPVT	WQFN-HR	RPV	12	250	205.0	200.0	33.0

RPV0012A

PACKAGE OUTLINE

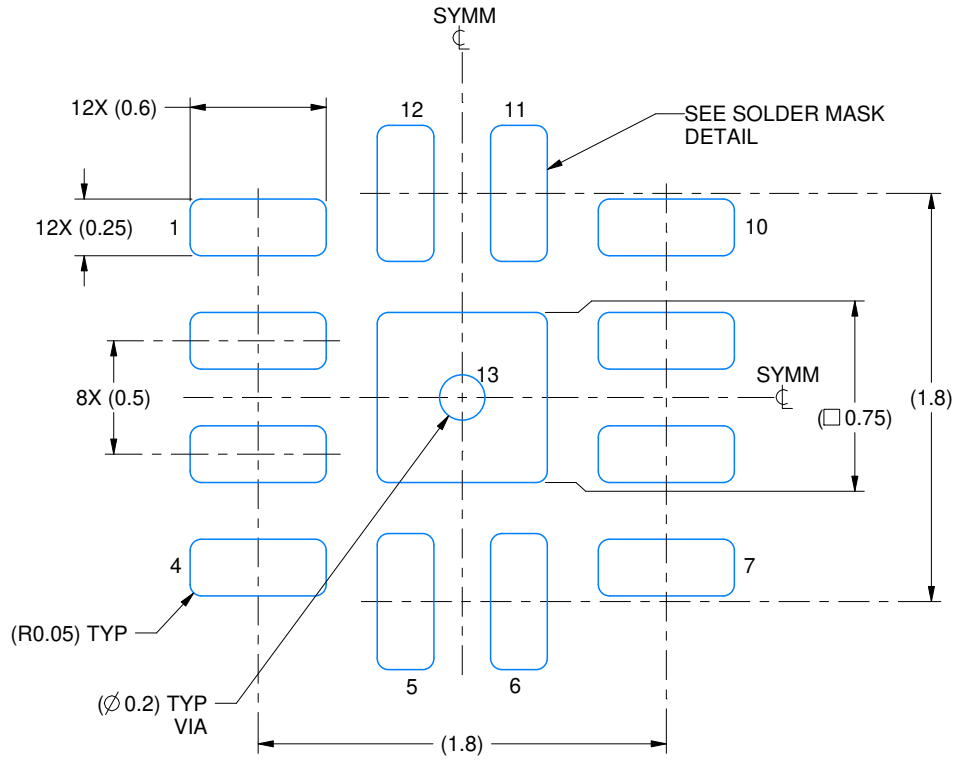
WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

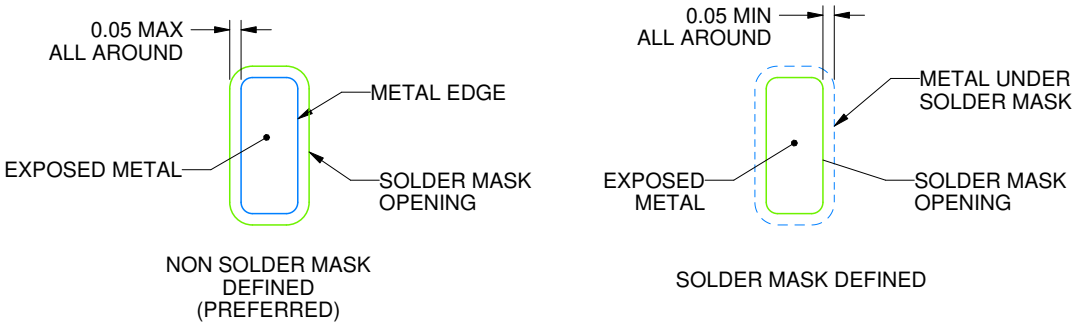


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

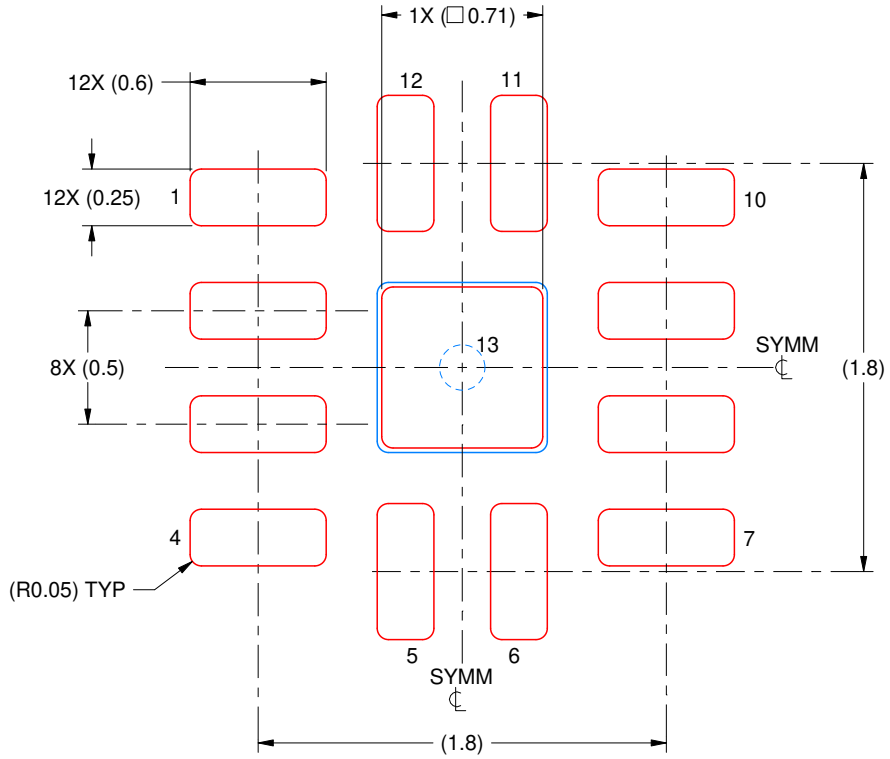


SOLDER MASK DETAILS

4225258/B 04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

EXPOSED PAD 13
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225258/B 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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