MP2130

High Efficiency, 3.5A, 6V, 1.2MHz Synchronous Step-Down Converter in an Ultra–Small QFN12 (2x2mm) Package

The Future of Analog IC Technology

DESCRIPTION

The MP2130 is a monolithic step-down switch mode converter with built-in internal power MOSFETs. It achieves 3.5A continuous output current from a 2.7V to 6V input voltage with excellent load and line regulation. The MP2130 is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) Battery. The output voltage can be regulated as low as 0.6V.

The Constant-On-time (COT) control scheme provides fast transient response high light-load efficiency and easy loop stabilization.

Fault condition protection includes cycle-by-cycle current limit and thermal shutdown.

The MP2130 requires a minimum number of readily available standard external components and is available in an ultra-small QFN12 (2x2mm) package.

The MP2130 is ideal for a wide range of applications including PDAs, portable instruments, DVD drives, small handhold and battery–powered devices.

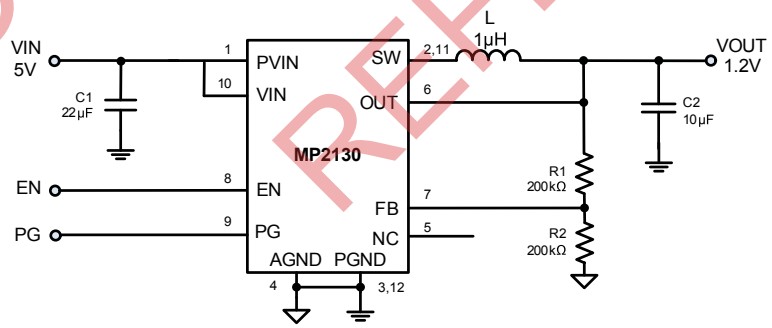
FEATURES

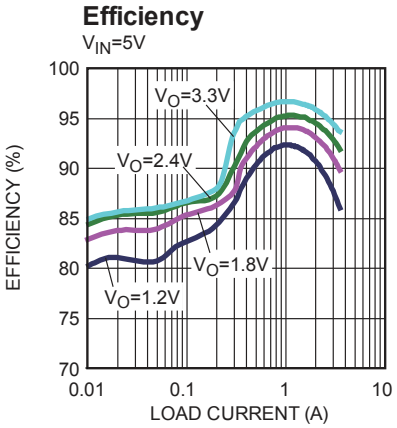
- Above 95% Peak Efficiency
- Above 80% Light Load Efficiency.
- Wide 2.7V to 6V Operating Input Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- 3.5A Output Current
- 50mΩ and 40mΩ Internal Power MOSFET
- 1.2MHz Frequency
- EN and Power Good for Power Sequencing
- Cycle-by-Cycle Over Current Protection
- Auto Discharge at Power-off
- Short Circuit Protection with Hiccup Mode
- Thermal Shutdown
- Stable with Low ESR Output Ceramic Capacitors
- Available in a QFN12 (2x2mm) Package

APPLICATIONS

- Storage Drives
- Portable/Handheld Devices
- Wireless/Networking Cards
- Low Voltage I/O System Power

TYPICAL APPLICATION



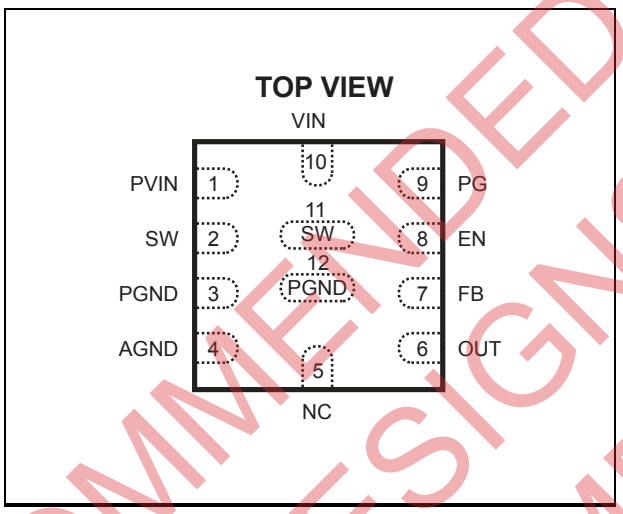


ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature
MP2130DG	QFN12 (2x2mm)	AB	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2130DG–Z);
For RoHS Compliant Packaging, add suffix –LF (e.g. MP2130DG–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 6.5V
V_{SW} ..... (-3V for <8ns) to (V_{IN} + 0.3V)
All Other Pins ..... -0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 1.6W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.7V to 6V
Output Voltage V_{OUT} ..... 0.6V to 5.5V
Maximum Junction Temp. (T_J) ..... +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN12 (2x2mm) ..... 80 ..... 16... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	2.7V ≤ V_{IN} ≤ 6V	0.591	0.600	0.609	V
Feedback Current	I_{FB}	V_{FB} = 0.6V		10		nA
PFET Switch On Resistance (5)	R_{DSON_P}	V_{IN}=3.6V		50		mΩ
NFET Switch On Resistance (5)	R_{DSON_N}	V_{IN}=3.6V		40		mΩ
Switch Leakage		V_{EN} = 0V, V_{IN}=6V, V_{SW} = 0V and 6V		0	2	μA
PFET Current Limit			3.6	4.5	6	A
NFET Switch Sinking Current	I_{NSW}	V_{OUT}=1.2V, V_{FB}=0.7V		100		μA
On Time	T_{ON}	V_{IN} = 5V, V_{OUT}=1.2V		200		ns
On Time		V_{IN}=3.6V, V_{OUT}=1.2V		277		ns
Minimum Off Time	T_{OFF}			30		ns
Soft-Start Time	T_{SS-ON}			1		ms
Soft-Stop Time	T_{SS-OFF}			1		ms
Power Good Upper Trip Threshold		FB with respect to the Regulation		+10		%
Power Good Lower Trip Threshold				-10		%
Power Good Delay				90		μs
Power Good Sink Current Capability	V_{PG_LO}	Sink 1mA			0.4	V
Power Good Logic High Voltage	V_{PG_HI}	V_{IN}=5V, V_{FB}=0.6V	4.9			V
Power Good Internal Pull Up Resistor	R_{PG}			500		kΩ
Under Voltage Lockout Threshold Rising			2.35	2.5	2.65	V
Under Voltage Lockout Threshold Hysteresis				400		mV
EN Input Logic Low Voltage					0.4	V
EN Input Logic High Voltage			1.2			V
EN Input Current		V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
Supply Current (Shutdown)		V_{EN} = 0V		0		μA
Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN}=3.6V		40		μA
Thermal Shutdown				150		°C
Thermal Hysteresis(5)				30		°C

Note:

5) Guaranteed by design.

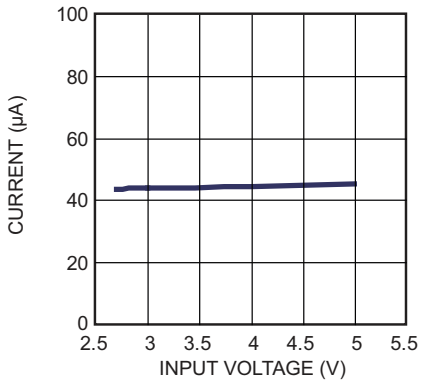
PIN FUNCTIONS

Pin #	Name	Description
1	PVIN	Supply Voltage to power FETs. PVIN is connected to VIN internally.
2, 11	SW	Switch Output. Pin 2 and 11 can be connected together.
3, 12	PGND	Power Ground. Pin 3 and 12 can be connected together.
4	AGND	Quiet ground for controller circuits
5	NC	Leave this pin open. Do not connect it to ground.
6	OUT	Input sense pin for output voltage
7	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
8	EN	On/Off Control.
9	PG	Power Good Indicator. The output of this pin is an open drain with internal pull up resistor to VIN. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level, otherwise it is LOW.
10	VIN	Supply Voltage to internal control circuitry. VIN is connected to PVIN internally.

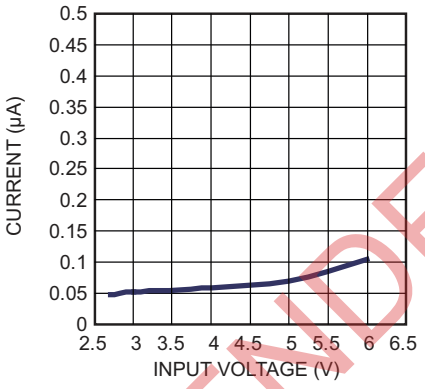
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=5V, V_{OUT}=1.2V, L=1µH, C_{OUT}=10µF, T_A = +25°C, unless otherwise noted

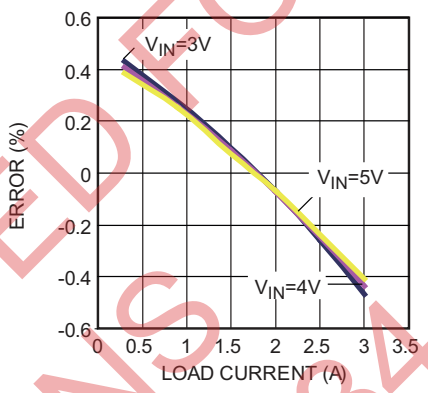
Quiescent Current vs. Input Voltage



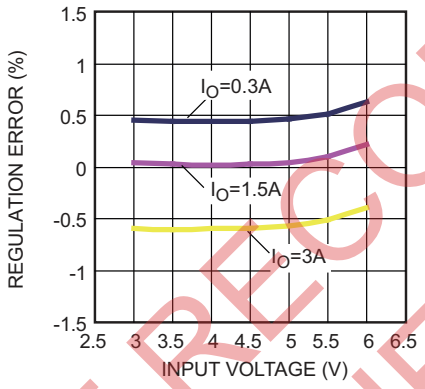
Shutdown Current vs. Input Voltage



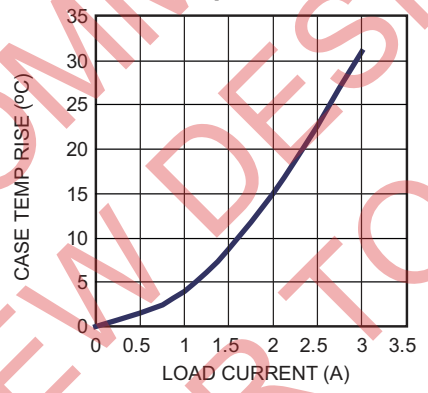
Load Regulation



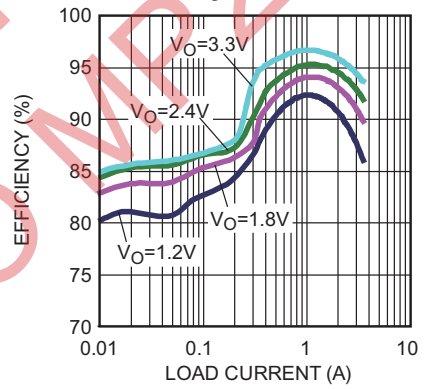
Line Regulation



Case Temp Rise

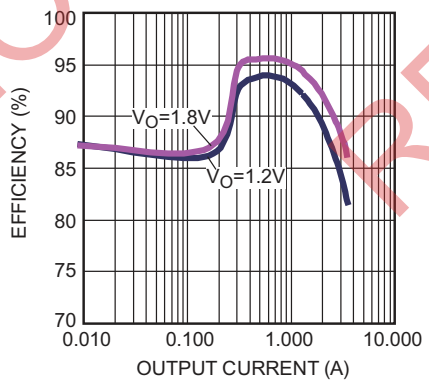


Efficiency



Efficiency

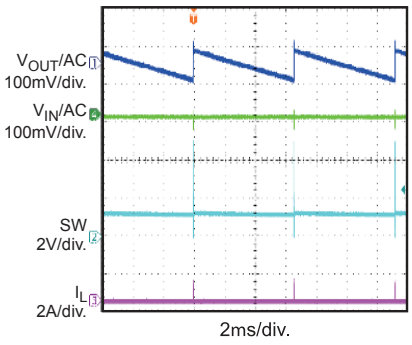
V_{IN}=3.3V



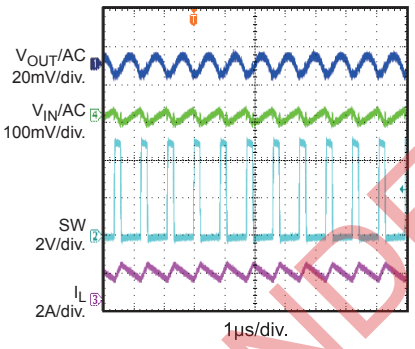
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, V_{OUT}=1.2V, L=1µH, C_{OUT}=10µF, T_A = +25°C, unless otherwise noted.

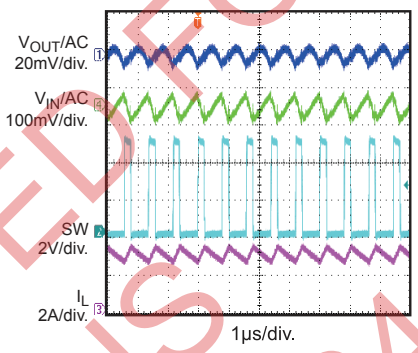
Input and Output Ripple
I_{OUT} = 0A



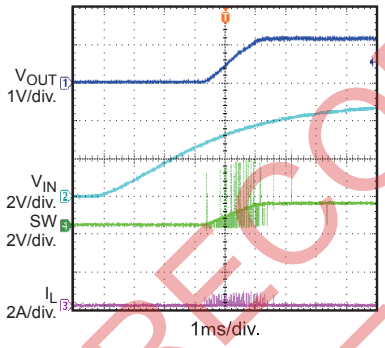
Input and Output Ripple
I_{OUT} = 1.5A



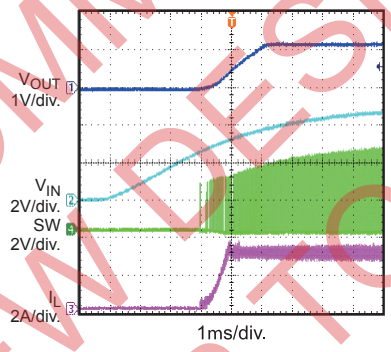
Input and Output Ripple
I_{OUT} = 3A



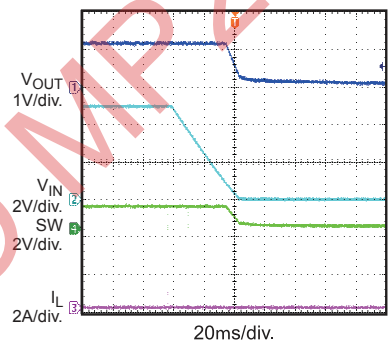
V_{IN} Power Up without Load



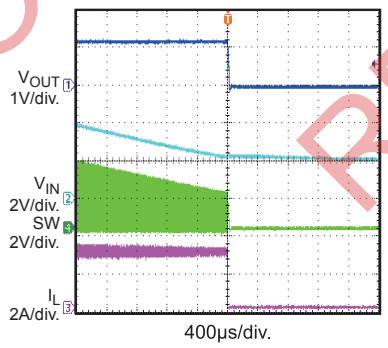
V_{IN} Power Up with 3A Load



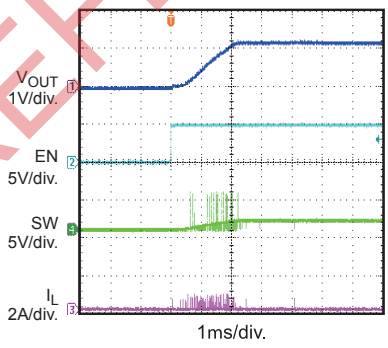
V_{IN} Shut down without Load



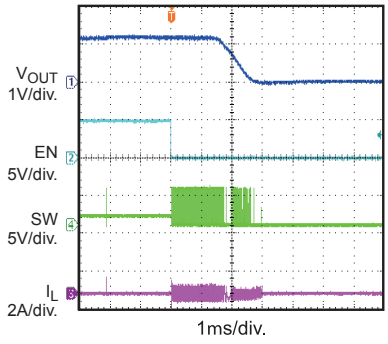
V_{IN} Shut down with 3A Load



EN Start Up without Load



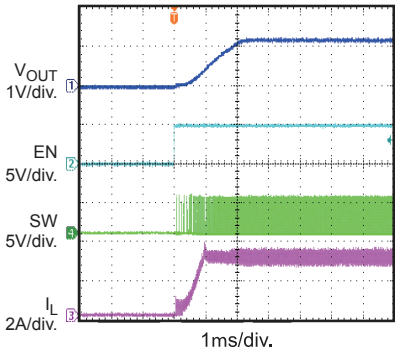
EN Shut Down without Load



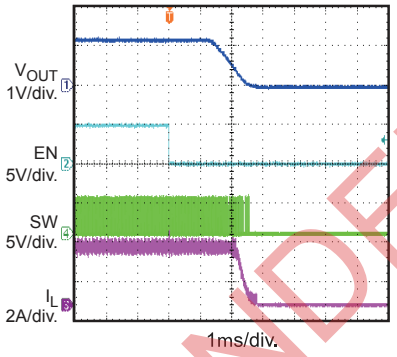
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, V_{OUT}=1.2V, L=1µH, C_{OUT}=10µF, T_A = +25°C, unless otherwise noted.

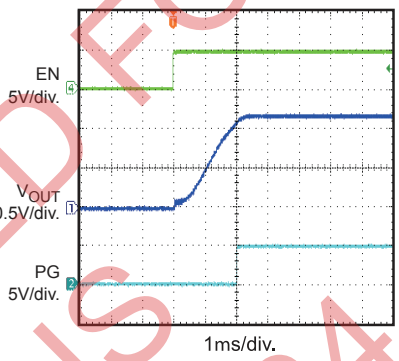
EN Start Up with 3A Load



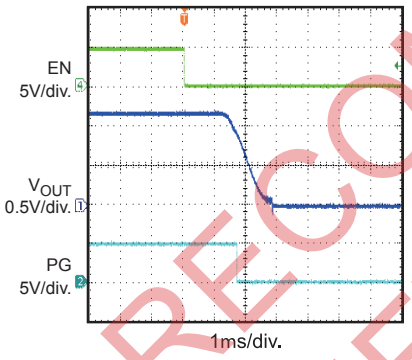
EN Shut Down with 3A Load



Power Good Through EN Start Up

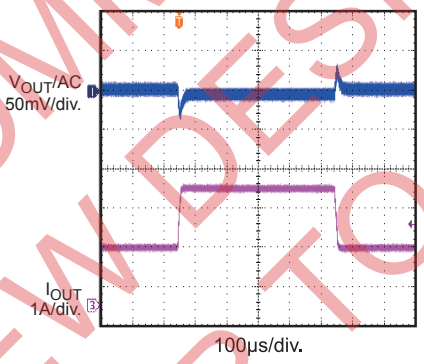


Power Good Through EN Shut Down

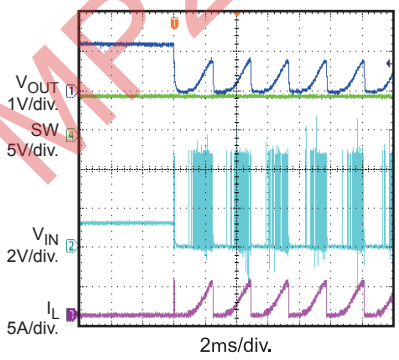


Load Transient Response

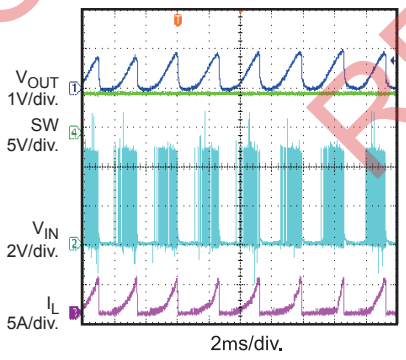
I_{OUT} = 1.5A to 3A



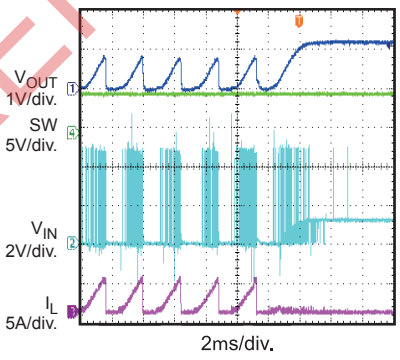
Short Circuit Entry



Short Circuit



Short Circuit Recovery



FUNCTIONAL BLOCKDIAGRAM

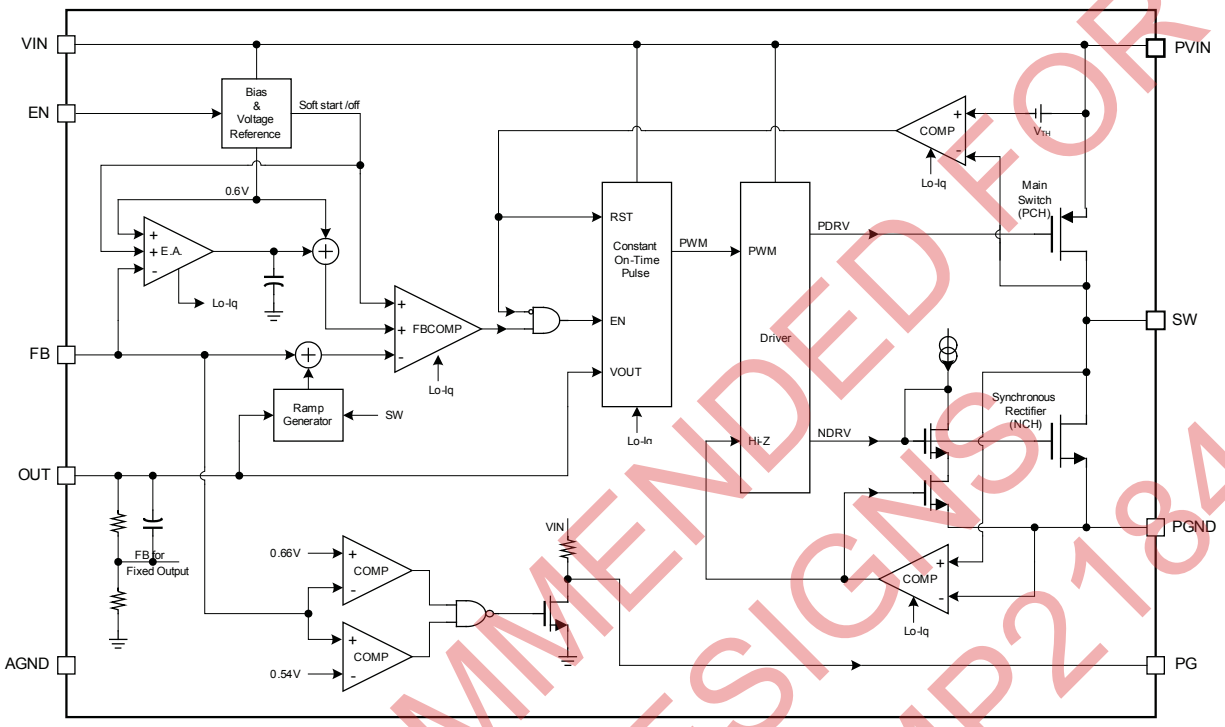


Figure 1—Functional Block Diagram

OPERATION

MP2130 uses constant on-time control with input voltage feed forward to stabilize the switching frequency over full input range. At light load, MP2130 employs a proprietary control of low side switch and inductor current to eliminate ringing on switching node and improve efficiency.

Constant On-time Control

Compare to fixed frequency PWM control, constant on-time control offers the advantage of simpler control loop and faster transient response. By using input voltage feed forward, MP2130 maintains a nearly constant switching frequency across input and output voltage range. The on-time of the switching pulse can be estimated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.833\mu s$$

To prevent inductor current run away during load transient, MP2130 fixes the minimum off time to be 30ns. However, this minimum off time limit will not affect operation of MP2130 in steady state in any way.

Light Load Operation

In light load condition, MP2130 uses a proprietary control scheme to save power and improve efficiency. Instead of turning off the low side switch immediately when inductor current start to reverse, MP2130 gradually ramp down and regulates the low side switch current to a minimal level, thus avoids the ringing at switching node that always occurs in discontinuous conduction mode (DCM) operation

Enable

When input voltage is greater than the under-voltage lockout threshold (UVLO), typically 2.5V, MP2130 can be enabled by pulling EN pin to higher than 1.2V. Leaving EN pin float or pull down to ground will disable MP2130. There is an internal 1Meg Ohm resistor from EN pin to ground.

Soft Start/Stop

MP2130 has built-in soft start that ramps up the output voltage in a controlled slew rate, avoiding overshoot at startup. The soft start time is about 1ms typical. At disable, MP2130 ramps down the internal reference thus allow the load to linearly discharge the output.

Power Good Indicator

MP2130 has an open drain with 500kΩ pull-up resistor pin for power good indicator PG. When FB pin is within +/-10% of regulation voltage, i.e. 0.6V, PG pin is pulled up to VIN by the internal resistor. If FB pin voltage is out of the +/-10% window, PG pin is pulled down to ground by an internal MOS FET. The MOS FET has a maximum R_{dson} of less than 100Ω.

Current limit

MP2130 has a typical 4.5A current limit for the high side switch. When the high side switch hits current limit, MP2130 will touch the hiccup threshold until the current lower down. This will prevent inductor current from continuing to build up which will result in damage of the components.

Short Circuit and Recovery

MP2130 enters short circuit protection mode when the inductor current hits the current limit, and tries to recover from short circuit with hiccup mode. In short circuit protection, MP2130 will disable output power stage, discharge soft-start cap and then automatically try to soft-start again. If the short circuit condition still holds after soft-start ends, MP2130 repeats this operation cycle till short circuit disappears and output rises back to regulation level.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 can not be too large neither too small considering the trade-off for stability and dynamic. Choose R1 to be around 120kΩ to 200kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1}$$

The feedback circuit is shown as Figure 2.

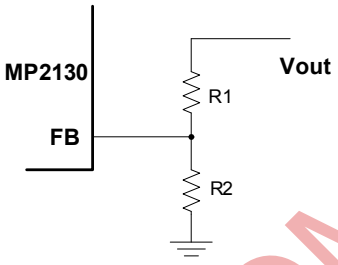


Figure 2— Feedback Network

Table 1 lists the recommended resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

Selecting the Inductor

A 0.82μH to 4.7μH inductor is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. For higher output voltage, 47μF may be needed for more stable system.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small and high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough

capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage.

Low ESR ceramic capacitors can be used with MP2130 to keep the output ripple low. Generally, 10μF output ceramic capacitor is enough for most of the cases. In higher output voltage condition, 22μF might be needed for a stable system.

Using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

Layout Recommendation of MP2130

Proper layout of the switching power supplies is very important, and sometimes critical to make it work properly. Especially, for the high switching converter, if the layout is not carefully done, the regulator could show poor line or load regulation, stability issues.

For MP2130, the high speed step-down regulator, the input capacitor should be placed as close as possible to the IC pins. As shown in Figure 6, the 0805 size ceramic capacitor is used, please make sure the two ends of the ceramic capacitor be directly connected to PIN1 (the Power Input Pin) and PIN 3 (the Power GND Pin).

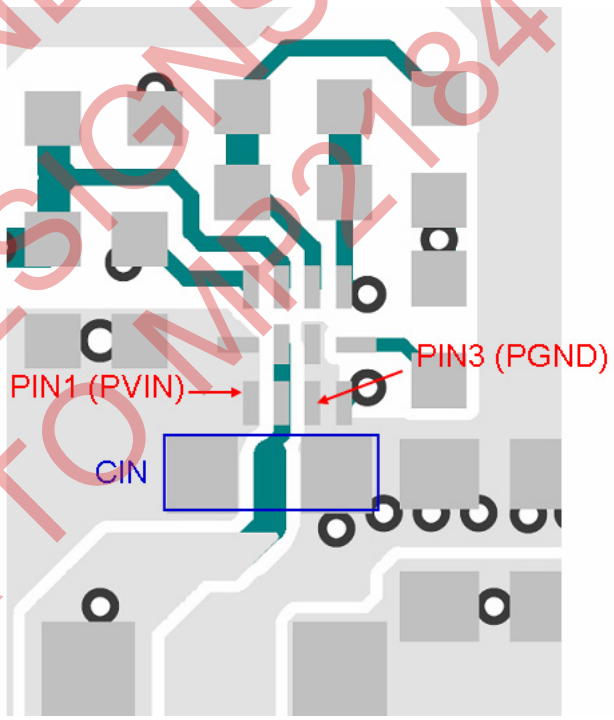
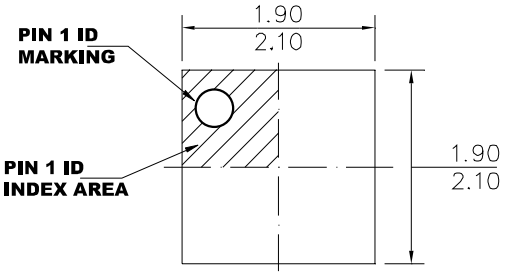


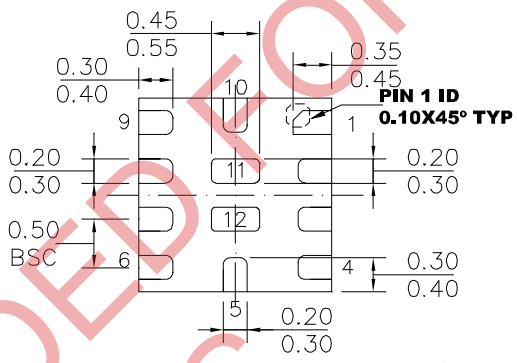
Figure 5—Two Ends off Input Decoupling Capacitor Close to Pin 1 and Pin 3

PACKAGE INFORMATION

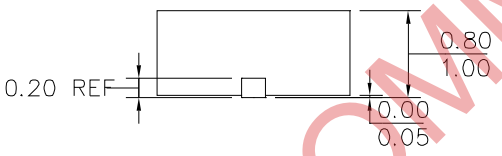
QFN12 (2x2mm)



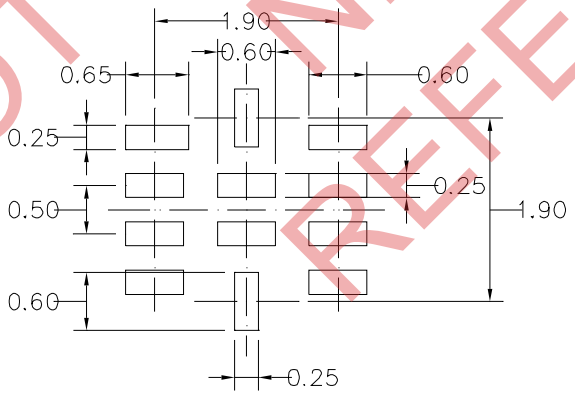
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.3	5/8/2021	Update the last page for the POD due to POD0092 has been updated from r3.0 to r4.0 per package dept.	P12