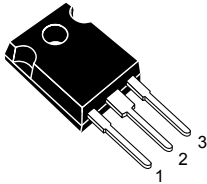
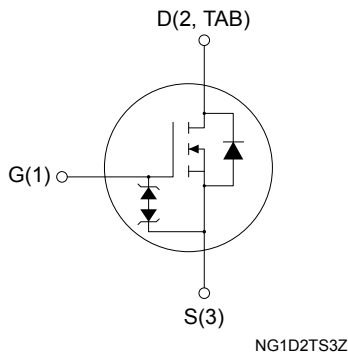


## N-channel 650 V, 93 mΩ typ., 32 A MDmesh DM2 Power MOSFET in a TO-247 package



TO-247



### Features

| Order code  | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|-------------|----------|-------------------|-------|
| STW35N65DM2 | 650 V    | 110 mΩ            | 32 A  |

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

#### Product status link

[STW35N65DM2](#)

#### Product summary

|                   |             |
|-------------------|-------------|
| <b>Order code</b> | STW35N65DM2 |
| <b>Marking</b>    | 35N65DM2    |
| <b>Package</b>    | TO-247      |
| <b>Packing</b>    | Tube        |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol                         | Parameter   | Value      | Unit |
|--------------------------------|---|------------|------|
| V <sub>GS</sub>                | Gate-source voltage (static)                          | ±25        | V    |
|                                | Gate-source voltage (dynamic AC (f > 1 Hz))           | ±30        |      |
| I <sub>D</sub>                 | Drain current (continuous) at T <sub>C</sub> = 25 °C  | 32         | A    |
|                                | Drain current (continuous) at T <sub>C</sub> = 100 °C | 20         |      |
| I <sub>DM</sub> <sup>(1)</sup> | Drain current (pulsed)                                | 90         | A    |
| P <sub>TOT</sub>               | Total power dissipation at T <sub>C</sub> = 25 °C     | 250        | W    |
| dv/dt <sup>(2)</sup>           | Peak diode recovery voltage slope                     | 100        | V/ns |
| di/dt <sup>(2)</sup>           | Peak diode recovery current slope                     | 1000       | A/μs |
| dv/dt <sup>(3)</sup>           | MOSFET dv/dt ruggedness                               | 100        | V/ns |
| T <sub>stg</sub>               | Storage temperature                                   | -55 to 150 | °C   |
| T <sub>J</sub>                 | Operating junction temperature                        |            |      |

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 32$  A,  $V_{DS\ peak} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .
3.  $V_{DS} \leq 520$  V.

**Table 2. Thermal data**

| Symbol                | Parameter                           | Value | Unit |
|-----------------------|-------------------------------------|-------|------|
| R <sub>thj-case</sub> | Thermal resistance junction-case    | 0.5   | °C/W |
| R <sub>thj-amb</sub>  | Thermal resistance junction-ambient | 50    | °C/W |

**Table 3. Avalanche characteristics**

| Symbol                         | Parameter                                       | Value | Unit |
|--------------------------------|---|-------|------|
| I <sub>AR</sub>                | Avalanche current, repetitive or not repetitive | 4     | A    |
| E <sub>AS</sub> <sup>(1)</sup> | Single pulse avalanche energy                   | 1150  | mJ   |

1. Starting T<sub>J</sub> = 25 °C, I<sub>D</sub> = I<sub>AR</sub>, V<sub>DD</sub> = 50 V.

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

**Table 4. Static**

| Symbol        | Parameter                         | Test conditions   | Min. | Typ. | Max.    | Unit             |
|---------------|-----------------------------------|---|------|------|---------|------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$   | 650  |      |         | V                |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$   |      |      | 1       | $\mu\text{A}$    |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ }^\circ\text{C}^{(1)}$ |      |      | 100     |                  |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$  |      |      | $\pm 5$ | $\mu\text{A}$    |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$  | 3    | 4    | 5       | V                |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$  |      | 93   | 110     | $\text{m}\Omega$ |

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

| Symbol                     | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit        |
|----------------------------|-------------------------------|--|------|------|------|-------------|
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$   | -    | 2540 | -    | $\text{pF}$ |
| $C_{oss}$                  | Output capacitance            |  | -    | 115  | -    | $\text{pF}$ |
| $C_{riss}$                 | Reverse transfer capacitance  |  | -    | 2.5  | -    | $\text{pF}$ |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0\text{ V}$  | -    | 204  | -    | $\text{pF}$ |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$  | -    | 4.2  | -    | $\Omega$    |
| $Q_g$                      | Total gate charge             | $V_{DD} = 520\text{ V}$ , $I_D = 32\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 14. Test circuit for gate charge behavior) | -    | 56.3 | -    | $\text{nC}$ |
| $Q_{gs}$                   | Gate-source charge            |  | -    | 12.7 | -    | $\text{nC}$ |
| $Q_{gd}$                   | Gate-drain charge             |  | -    | 27.6 | -    | $\text{nC}$ |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions   | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 325\text{ V}$ , $I_D = 16\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$   | -    | 23.4 | -    | ns   |
| $t_r$        | Rise time           |   | -    | 23   | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | -    | 72   | -    | ns   |
| $t_f$        | Fall time           |   | -    | 10.4 | -    | ns   |

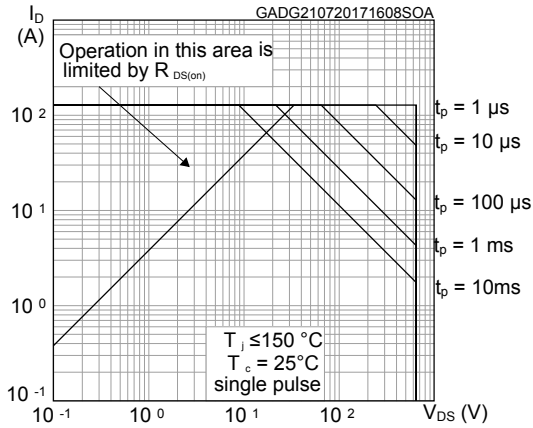
**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|--|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |  | -    |      | 32   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |  | -    |      | 90   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 32\text{ A}$   | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 32\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times)  | -    | 100  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  | -    | 0.42 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  | -    | 8.4  |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 32\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 205  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  | -    | 1.8  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  | -    | 17.6 |      | A             |

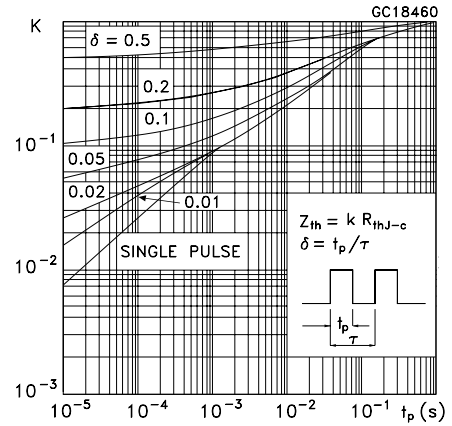
1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

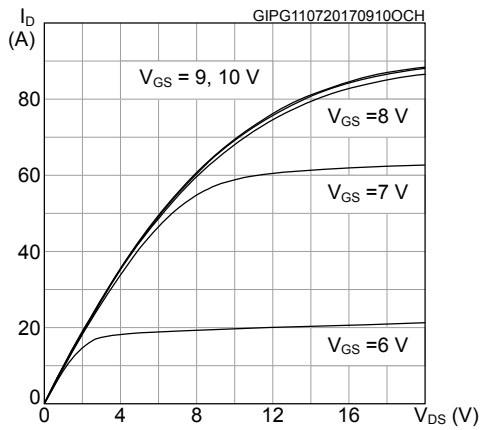
**Figure 1. Safe operating area**



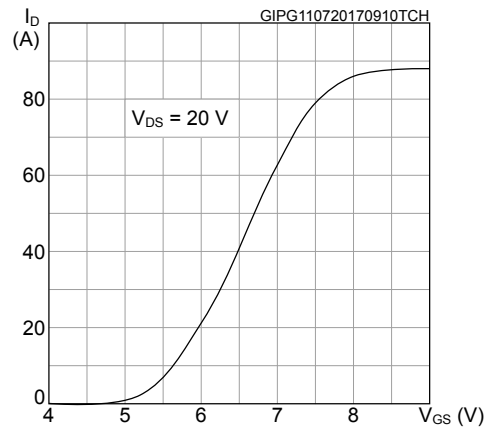
**Figure 2. Thermal impedance**



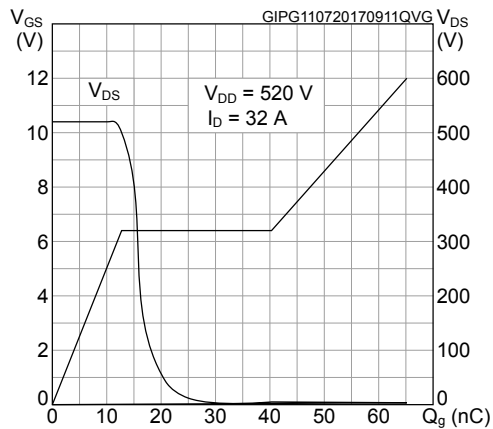
**Figure 3. Output characteristics**



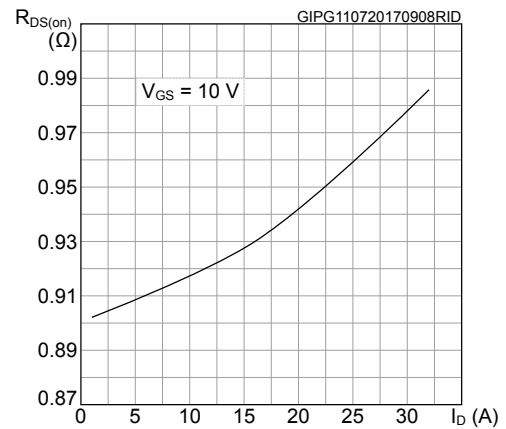
**Figure 4. Transfer characteristics**



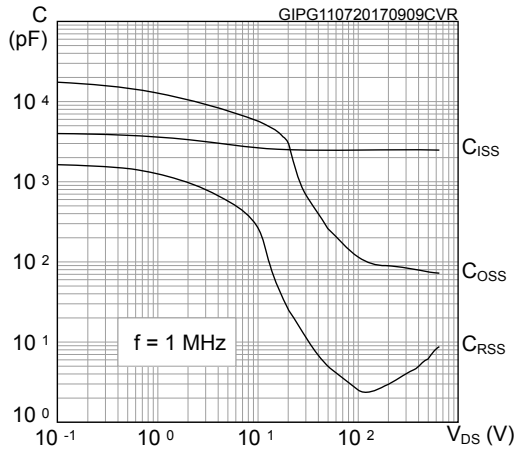
**Figure 5. Gate charge vs gate-source voltage**



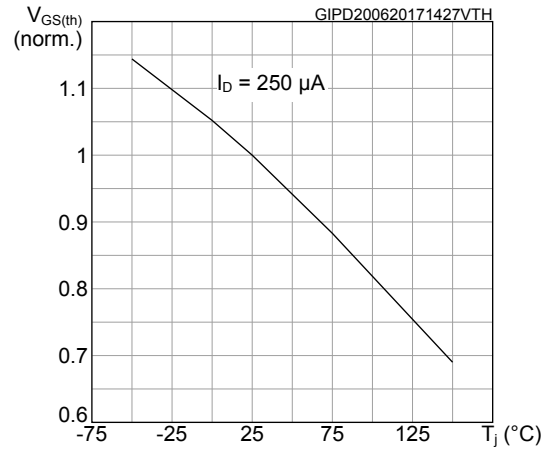
**Figure 6. Static drain-source on-resistance**



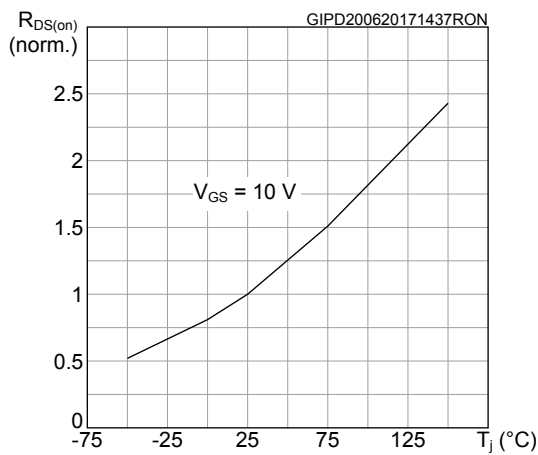
**Figure 7. Capacitance variations**



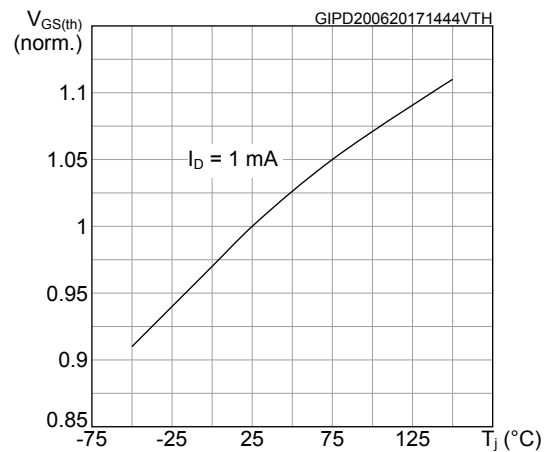
**Figure 8. Normalized gate threshold voltage vs temperature**



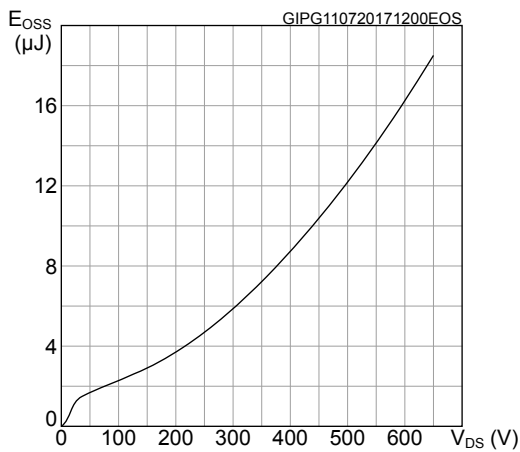
**Figure 9. Normalized on-resistance vs temperature**



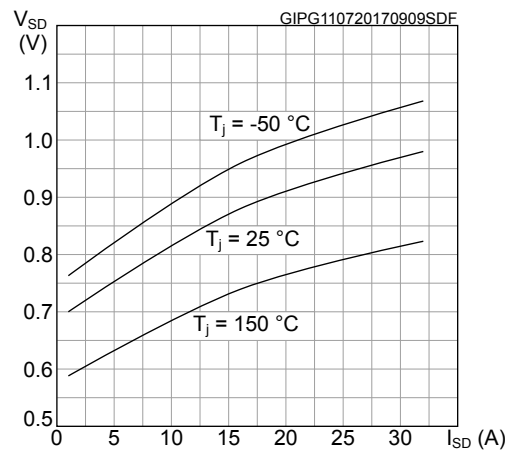
**Figure 10. Normalized V<sub>(BR)DSS</sub> vs temperature**



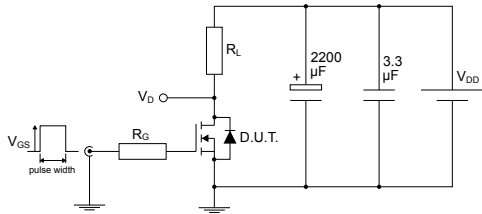
**Figure 11. Output capacitance stored energy**



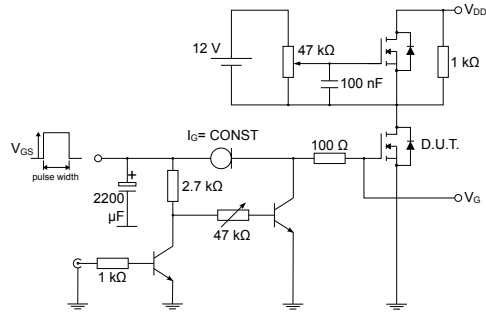
**Figure 12. Source-drain diode forward characteristics**



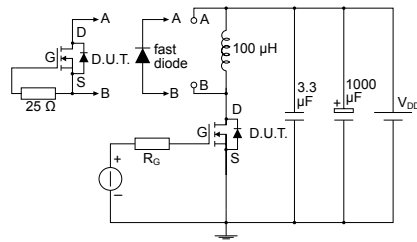
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


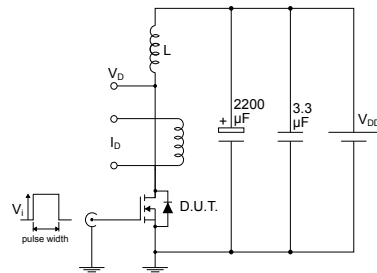
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


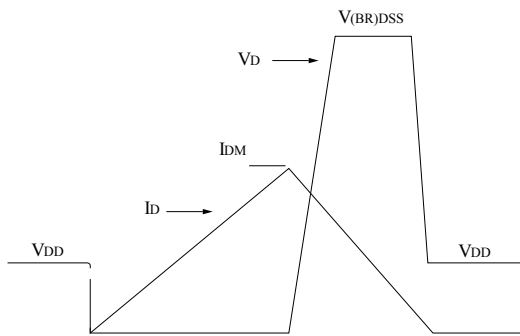
AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


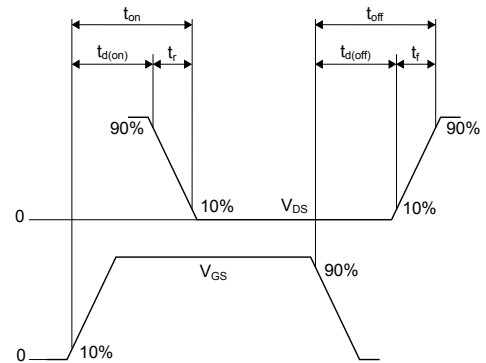
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**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


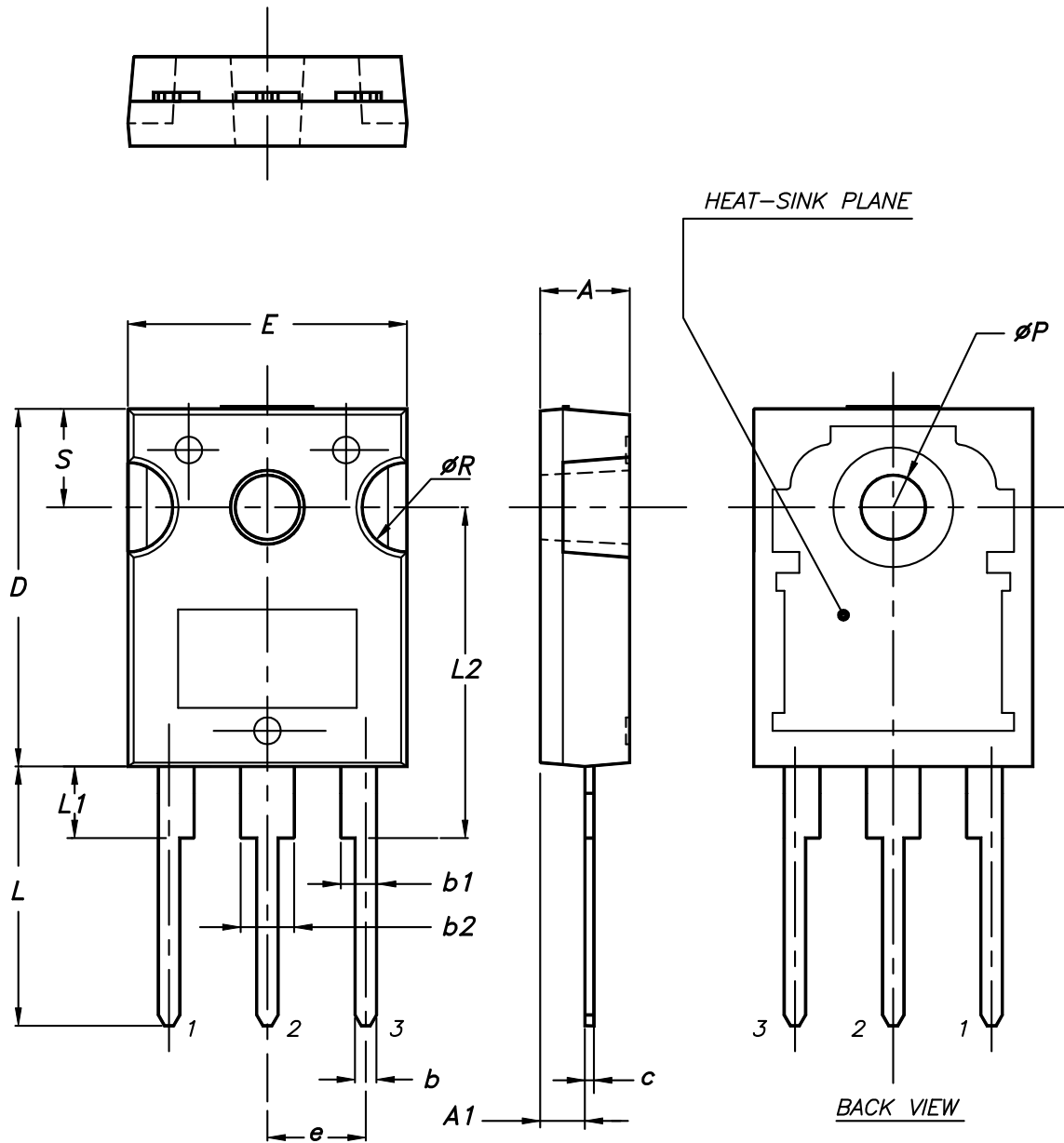
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-247 package information

Figure 19. TO-247 package outline



0075325\_9



**Table 8. TO-247 package mechanical data**

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 4.85  |       | 5.15  |
| A1   | 2.20  |       | 2.60  |
| b    | 1.0   |       | 1.40  |
| b1   | 2.0   |       | 2.40  |
| b2   | 3.0   |       | 3.40  |
| c    | 0.40  |       | 0.80  |
| D    | 19.85 |       | 20.15 |
| E    | 15.45 |       | 15.75 |
| e    | 5.30  | 5.45  | 5.60  |
| L    | 14.20 |       | 14.80 |
| L1   | 3.70  |       | 4.30  |
| L2   |       | 18.50 |       |
| ØP   | 3.55  |       | 3.65  |
| ØR   | 4.50  |       | 5.50  |
| S    | 5.30  | 5.50  | 5.70  |

## Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 21-Jul-2017 | 1        | Initial release  |
| 12-Dec-2017 | 2        | Document status change from preliminary data to production data.<br>Update <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 8: "Source-drain diode"</i> and <i>Figure 2: "Safe operating area"</i> .<br>Minor text changes. |
| 31-Aug-2020 | 3        | Updated <i>Table 1. Absolute maximum ratings</i> .<br>Minor text changes.  |

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