ISL78419

Integrated Automotive TFT-LCD Power Supply Regulator

FN8292
Rev 3.00
June 27, 2014

The ISL78419 is an integrated power management IC (PMIC) for TFT-LCDs used in central display, rear seat entertainment and virtual dashboards. The device integrates a boost converter for generating AV_{DD}, an LDO regulator for V_{LOGIC}. V_{ON} and V_{OFF} are generated by a charge pump driven by the switch node of the boost converter. The ISL78419 also includes a V_{ON} slice circuit, reset function, and a high performance VCOM amplifier with a Digitally Controlled Potentiometer (DCP) that is used as a VCOM calibrator.

The AV_{DD} boost converter features a 1.5A/0.18Ω boost FET with 600kHz/1200kHz switching frequency.

The integrated logic LDO includes a 350mA FET for driving the low voltage needed by external digital circuitry.

The gate pulse modulator can control the gate voltage up to 30V, and both the rate and slew delay times are selectable.

The supply monitor generates a reset signal when the system is powered down based on a user selected threshold level (programming resistor).

The ISL78419 provides a digitally controlled VCOM output using I^2C interface. One VCOM amplifier is also integrated in the chip to provide a fast slewing 150mA drive (sourcing or sinking). The output of the VCOM is powered up with the voltage stored at the last programmed 8-bit (internal) EEPROM setting.

The ISL78419 is rated to operate over the temperature range of (-40°C to +105°C) and is qualified according to AEC-Q100.

Features

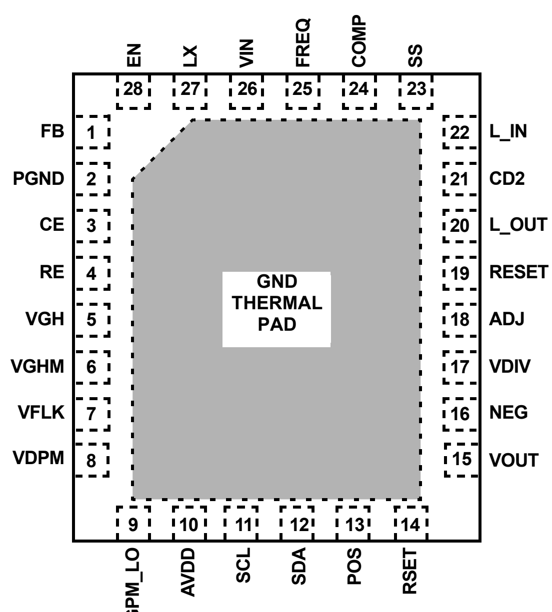
- 2.5V to 5.5V input
- 1.5A, 0.18Ω integrated boost FET
- V_{ON}/V_{OFF} supplies generated by charge pumps driven by the boost switch node
- LDO for V_{LOGIC} channel
- 600kHz/1200kHz selectable switching frequency
- Integrated gate pulse modulator
- Reset signal generated by supply monitor
- Integrated VCOM amplifier
- DCP
  - I^2C serial interface, address: 0101000, MSB left
  - Wiper position stored in 8-bit nonvolatile memory and recalled on power-up
  - Endurance, 1,000 data changes per bit
- UVLO, UVP, OVP, OCP, and OTP protection
- Pb-free (RoHS compliant)
- 28 Ld 4x5 QFN
- AEC-Q100 qualified

Applications

- Automotive TFT displays
  - Central displays, rear seat entertainment and dashboards

Pin Configuration

ISL78419 (28 LD 4x5 QFN)
TOP VIEW



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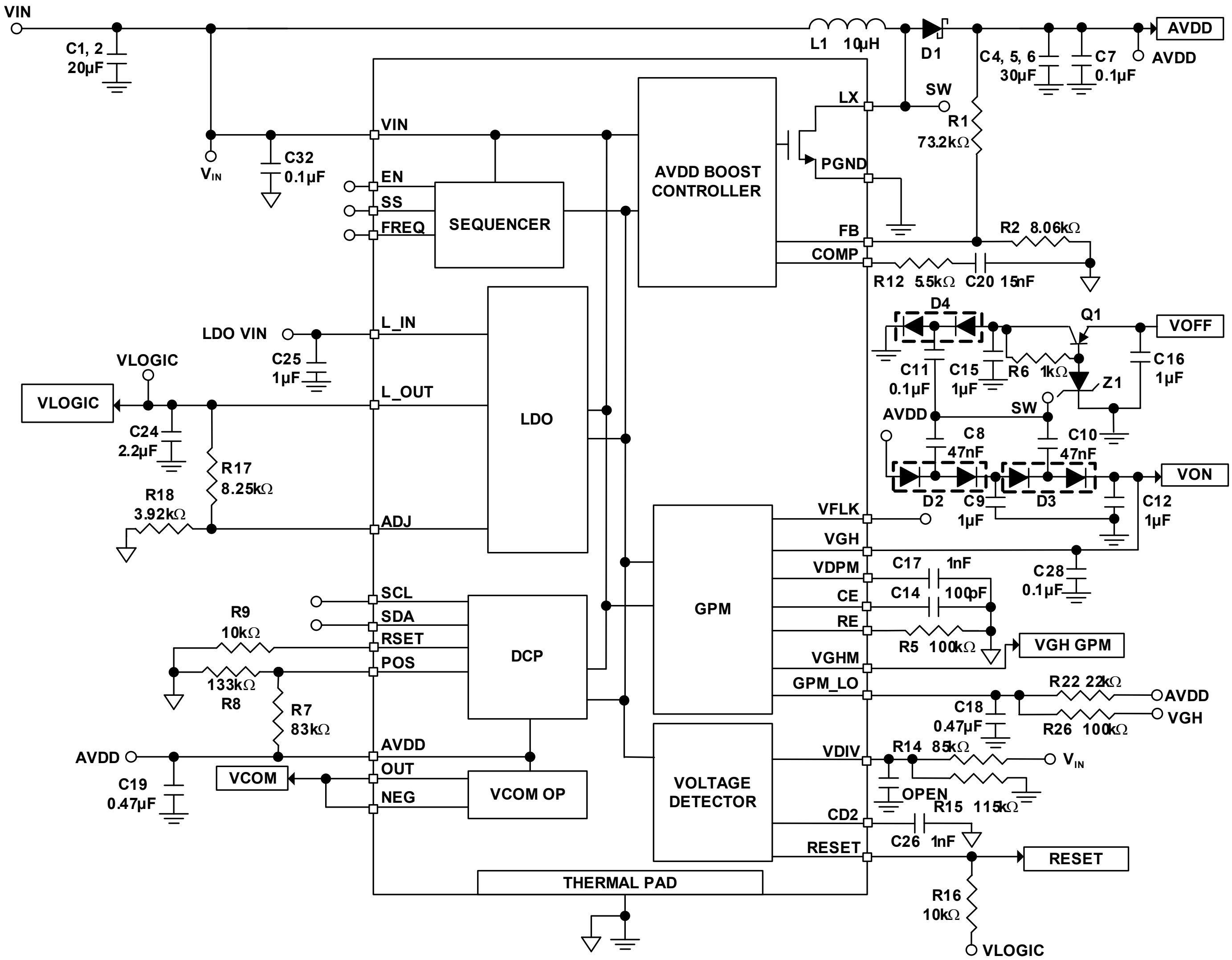
Application Diagram



Pin Descriptions

PIN#	SYMBOL	DESCRIPTION
1	FB	AV_{DD} boost converter feedback. Connect to the center of a voltage divider between AV_{DD} and GND to set the AV_{DD} voltage.
2	PGND	Power ground
3	CE	Gate Pulse Modulator Delay Control. Connect a capacitor between this pin and GND to set the delay time.
4	RE	Gate Pulse Modulator Slew Control. Connect a resistor between this pin and GND to set the falling slew rate.
5	VGH	Gate Pulse Modulator High Voltage Input. Place a 0.1µF decoupling capacitor close to the VGH pin.
6	VGHM	Gate Pulse Modulator Output for gate driver IC
7	VFLK	Gate Pulse Modulator Control input from T_{CON}
8	VDPM	Gate Pulse Modulator Enable. Connect a capacitor from VDPM to GND to set the delay time before GPM is enabled. A current source charges the capacitor on VDPM.
9	GPM_LO	Gate Pulse Modulator Low Voltage Input; place a 0.47µF decoupling capacitor close to the GPM_LO pin.
10	AVDD	DCP and VCOM amplifier high voltage analog supply; place a 0.47µF decoupling capacitor close to the AVDD pin.
11	SCL	I^2C compatible clock input

Pin Descriptions (Continued)

PIN#	SYMBOL	DESCRIPTION
12	SDA	I^2C compatible serial bidirectional data line
13	POS	VCOM Amplifier Non-inverting input
14	RSET	DCP sink current adjustment pin; connect a resistor between this pin and GND to set the resolution of the DCP output voltage.
15	VOUT	VCOM Amplifier output
16	NEG	VCOM Amplifier inverting input
17	VDIV	Voltage detector threshold. Connect to the center of a resistive divider between V_{IN} and GND.
18	ADJ	VLOGIC LDO feedback. Connect to the center of a resistive divider between L_OUT and GND to set V_{LOGIC} voltage for T_{CON}.
19	RESET	Voltage detector reset output
20	L_OUT	LDO output. Connect at least one 1µF capacitor to GND for stable operation.
21	CD2	Voltage detector rising edge delay. Connect a capacitor between this pin and GND to set the rising edge delay.
22	L_IN	LDO input. Connect a 1µF decoupling capacitor close to this pin.
23	SS	Boost Converter Soft-Start. Connect a capacitor between this pin and GND to set the soft-start time.
24	COMP	Boost converter compensation pin. Connect a series resistor and capacitor between this pin and GND to optimize transient response and stability.
25	FREQ	Boost Converter frequency select; pull it to logic high to operate boost at 1.2MHz. Connect this pin to GND to operate boost at 600kHz.
26	VIN	IC input supply. Connect a 0.1µF decoupling capacitor close to this pin.
27	LX	AV_{DD} boost converter switching node
28	EN	AV_{DD} enable pin

Ordering Information

PART NUMBER (Notes Notes 1, 2, 3)	PART MARKING	V_{IN} RANGE (V)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL78419ARZ	78419 ARZ	2.5 to 5.5	-40 to +105	28 Ld 4x5 QFN	L28.4x5A

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78419 For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

RE, VGHM, GPM_LO and VGH to GND . . . .-0.3 to +36V
LX, AVDD, POS, NEG, VOUT to GND . . . . -0.3 to +18V
Voltage Between GND and PGND. . . . . ±0.5V
All Other Pins to GND . . . . -0.3 to +6.0V
ESD Rating
Human Body Model (Tested per JESD22-A114E). 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per AEC-Q100-11). 1kV
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld 4x5 QFN Package (Notes 4, 5)	38	4.5

Ambient Temperature . . . .-40°C to +105°C
Functional Junction Temperature. . . . .-40°C to +150°C
Storage Temperature . . . .-65°C to +150°C
Lead Temperature During Soldering . . . . +260°C
Pb-Free Reflow Profile . . . . see TB493

Recommended Operating Conditions

Temperature . . . .-40°C to +105°C
Supply Voltage . . . . 2.5V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN} = ENABLE = 3.3V, AV_{DD} = 8V, V_{LDO} = 2.5V, V_{ON} = 24V, V_{OFF} = - 6V. **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS
GENERAL						
VIN	V_{IN} Supply Voltage Range		**2.5**	3.3	**5.5**	V
I_{S_DIS}	V_{IN} Supply Currents when Disabled	V_{IN} < UVLO		390	**500**	µA
I_S	V_{IN} Supply Currents	ENABLE = 3.3V, overdrive AV_{DD} and V_{GH}		0.7	**1.0**	mA
I_{ENABLE}	ENABLE Pin Current	ENABLE = 0V		0		µA
LOGIC INPUT CHARACTERISTICS - ENABLE, FLK, SCL, SDA, FREQ						
V_{IL}	Low Voltage Threshold				**0.65**	V
V_{IH}	High Voltage Threshold		**1.75**			V
R_{IL}	Pull-Down Resistor	Enable, FLK, FREQ	**0.85**	1.25	**1.65**	MΩ
INTERNAL OSCILLATOR						
f_{OSC}	Switching Frequencies	FREQ = low, T_A = +25°C	550	600	650	kHz
		FREQ = high, T_A = +25°C	1100	1200	1300	kHz
AVDD BOOST REGULATOR						
DAVDD/ DIOUT	AVDD Load Regulation	50mA < I_{LOAD} < 250mA		0.2		%
DAVDD/ DVIN	AVDD Line Regulation	I_{LOAD} = 150mA, 2.5V < V_{IN} < 5.5V		0.15		%
V_{FB}	Feedback Voltage (V_{FB})	I_{LOAD} = 100mA, T_A = +25°C	0.792	0.8	0.808	V
I_{FB}	FB Input Bias Current				**100**	nA
$r_{DS(ON)}$	Switch ON-Resistance	T_A = +25°C		180	260	mΩ
I_{LIM}	Switch Current Limit		**1.125**	1.5	**1.875**	A
D_{MAX}	Max Duty Cycle	Freq = 1.2MHz	**80**	90		%
EFF		Freq = 1.2MHz, I_{AVDD} = 100mA		91		%
LDO REGULATOR						
DV_{LDO}/ DV_{IN}	Line Regulation	I_{LDO} = 1mA, 3.0V < V_{IN1} < 5.5V		1		mV/V

Electrical Specifications V_{IN} = ENABLE = 3.3V, AV_{DD} = 8V, V_{LDO} = 2.5V, V_{ON} = 24V, V_{OFF} = - 6V. Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS
DV_{LDO}/DI_{OUT}	Load Regulation	1mA < I_{LDO} < 350mA		0.2		%
V_{DO}	Dropout Voltage	Output drops by 2%, I_{LDO} = 350mA		225	**300**	mV
I_{LIML}	Current Limit	Output drops by 5%	**330**	425		mA
V_{ADJ}	ADJ Reference Voltage	I_{LOAD} = 50mA, T_A = +25°C	0.792	0.8	0.808	V
I_{ADJ}	ADJ Input Bias Current				**0.1**	µA
GATE PULSE MODULATOR						
V_{GH}	VGH Voltage		**7**		**33**	V
V_{IH_VDPM}	V_{DPM} Enable Threshold		**1.13**	1.215	**1.30**	V
I_{VGH}	VGH Input Current	VFLK = 0		125		µA
		RE = 100kΩ, VFLK = V_{IN}		27.5		µA
V_{GPM_LO}	GPM_LO Voltage		**2**		**V_{GH}-2**	V
I_{GPM_LO}	VGPM_LO Input Current		**-2**	0.1	**2**	µA
VCE_{th1}	CE Threshold Voltage 1			0.6xV_{IN}	**0.8xV_{IN}**	V
VCE_{th2}	CE Threshold Voltage 2			1.215		V
I_{CE}	CE Current			100		µA
R_{VGHM_PD}	VGHM Pull-down Resistance			1.1		kΩ
R_{ONVGH}	VGH to VGHM ON-resistance			23		Ω
IDPM	VDPM Charge Current			10		µA
SUPPLY MONITOR						
V_{IH_VDIV}	VDIV High Threshold	VDIV rising	**1.265**	1.280	**1.295**	V
V_{IL_VDIV}	VDIV Low Threshold	VDIV falling	**1.21**	1.222	**1.234**	V
VthCD2	CD2 Threshold voltage		**1.200**	1.217	**1.234**	V
I_{CD2}	CD2 Charge Current			10		µA
R_{IL_RESET}	RESET Pull-down Resistance			650		Ω
t_{DELAY_RESET}	RESET Delay on the Rising Edge			121.7k* CD		s
VCOM AMPLIFIER R_{LOAD} = 10kΩ, C_{LOAD} = 10pF, unless otherwise stated						
I_{S_com}	VCOM Amplifier Supply Current			0.7	**1.08**	mA
V_{OS}	Offset Voltage			2.5	**15**	mV
I_B	Non-inverting Input Bias Current			0		nA
CMIR	Common-Mode Input Voltage Range		**0**		**AV_{DD}**	V
CMRR	Common-Mode Rejection Ratio		**60**	75		dB
PSRR	Power Supply Rejection Ratio		**70**	85		dB
V_{OH}	Output Voltage Swing High	I_{OUT}(source) = 0.1mA		AV_{DD} - 1.39		mV
		I_{OUT}(source) = 75mA		AV_{DD} - 1.27		V
V_{OL}	Output Voltage Swing Low	I_{OUT}(sink) = 0.1mA		1.2		mV
		I_{OUT}(sink) = 75mA		1		V
I_{SC}	Output Short Circuit Current	Pull-up	**150**	225		mA
		Pull-down	**150**	200		mA
SR	Slew Rate			25		V/µs
BW	Gain Bandwidth	-3dB gain point		20		MHz

Electrical Specifications

V_{IN} = ENABLE = 3.3V, AV_{DD} = 8V, V_{LDO} = 2.5V, V_{ON} = 24V, V_{OFF} = - 6V. Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS
DIGITAL CONTROLLED POTENTIOMETER						
SET_{VR} (Note 12)	SET Voltage Resolution			8		Bits
SET_{DNL} (Notes 8, 9, 14)	SET Differential Nonlinearity	T_A = +25°C			±1	LSB
SET_{ZSE} (Notes 10, 14)	SET Zero-Scale Error	T_A = +25°C			±2	LSB
SET_{FSE} (Notes 11, 14)	SET Full-Scale Error	T_A = +25°C			±8	LSB
I_{RSET}	RSET Current				**100**	µA
AVDD to SET	AVDD to SET Voltage Attenuation			1:20		V/V
FAULT DETECTION THRESHOLD						
V_{UVLO}	Undervoltage Lockout Threshold	PV_{IN} rising	**2.25**	2.33	**2.41**	V
		PV_{IN} falling	**2.125**	2.20	**2.27**	V
OVP_{AVDD} (Note 13)	Boost Overvoltage Protection Off Threshold to Shutdown IC		**15.0**	15.5	**16.0**	V
T_{OFF}	Thermal Shutdown all Channels	Temperature rising		153		°C
POWER SEQUENCE TIMING						
t_{ss}VLOGIC	VLOGIC Soft-Start Time			0.45		ms
I_{ss}	Boost Soft-Start Current		**3**	5.5	**8**	µA

Serial Interface Specifications

For SCL and SDA Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP (Note 7)	MAX (Note 14)	UNITS
f_{SCL} (Note 6)	SCL Frequency				**400**	kHz
t_{IN} (Note 6)	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the maximum specification is suppressed			**50**	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{IN}, until SDA exits the 30% to 70% of V_{IN} window			480	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{IN} during the following START condition	480			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{IN} crossing	480			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{IN} crossing	400			ns
$t_{SU:STA}$	START Condition Set-up Time	SCL rising edge to SDA falling edge; both crossing 70% of V_{IN}	480			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{IN} to SCL falling edge crossing 70% of V_{IN}	400			ns
$t_{SU:DAT}$	Input Data Set-up Time	From SDA exiting the 30% to 70% of V_{IN} window, to SCL rising edge crossing 30% of V_{IN}	40			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{IN} to SDA entering the 30% to 70% of V_{IN} window	0			ns
$t_{SU:STO}$	STOP Condition Set-up Time	From SCL rising edge crossing 70% of V_{IN}, to SDA rising edge crossing 30% of V_{IN}	400			ns

Serial Interface Specifications For SCL and SDA Unless Otherwise Noted. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP (Note 7)	MAX (Note 14)	UNITS
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge; both crossing 70% of V_{IN}	400			ns
C_{SCL}	Capacitive on SCL			5		pF
C_{SDA}	Capacitive on SDA			5		pF
t_{Wp}	Non-Volatile Write Cycle Time			25		ms
	EEPROM Endurance	T_A = +25°C		1		kCyc
	EEPROM Retention	T_A = +25°C		88		kHrs

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Typical values are for T_A = +25°C and V_{IN} = 3.3V.
8. LSB = $|V_{255} - V_1|/254$. V_{255} and V_1 are the measured voltages for the DCP register set to FF hex and 01 hex respectively.
9. DNL = $|V_{i+1} - V_i|/LSB-1$, $i \in [1, 255]$
10. ZS error = (V_1 -VMIN)/LSB. VMIN = (VAVDD*R2) * [1-254*R1/(255*20*RSET)]/ (R1+R2).
11. FS error = (V_{255} - VMAX)/LSB. VMAX = (VAVDD*R2) * [1-0*R1/(255*20*RSET)]/ (R1+R2).
12. Established by design. Not a parametric specification.
13. Boost will stop switching as soon as boost output reaches OVP threshold.
14. Compliance to limits is assured by characterization and design.

Typical Performance Curves

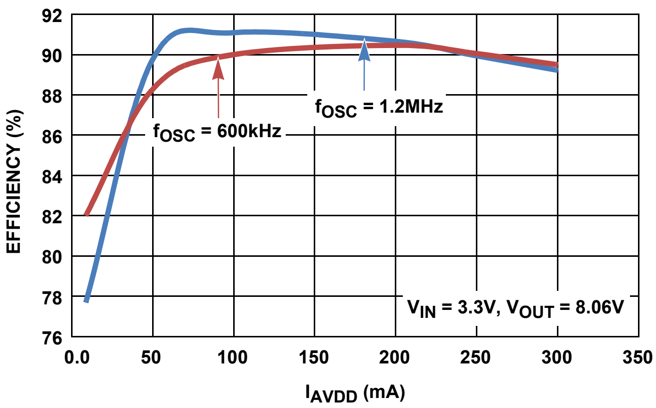


FIGURE 1. AV_{DD} EFFICIENCY vs I_{AVDD}

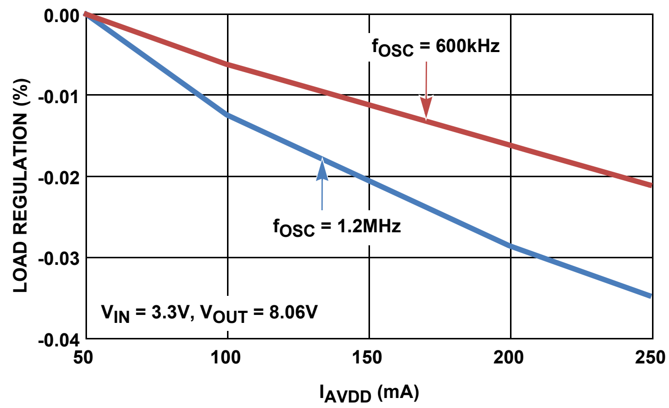


FIGURE 2. AV_{DD} LOAD REGULATION vs I_{AVDD}

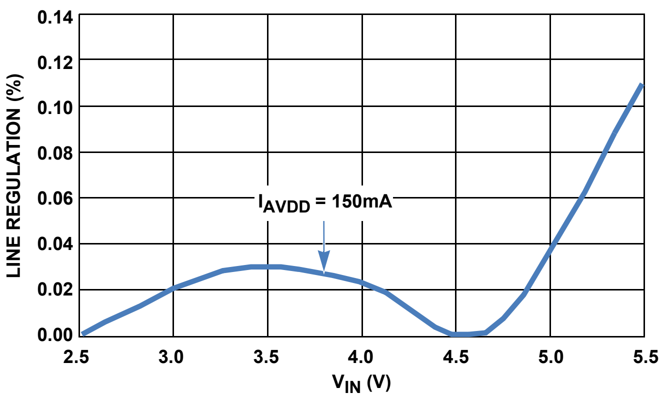


FIGURE 3. AV_{DD} LINE REGULATION vs V_{IN}

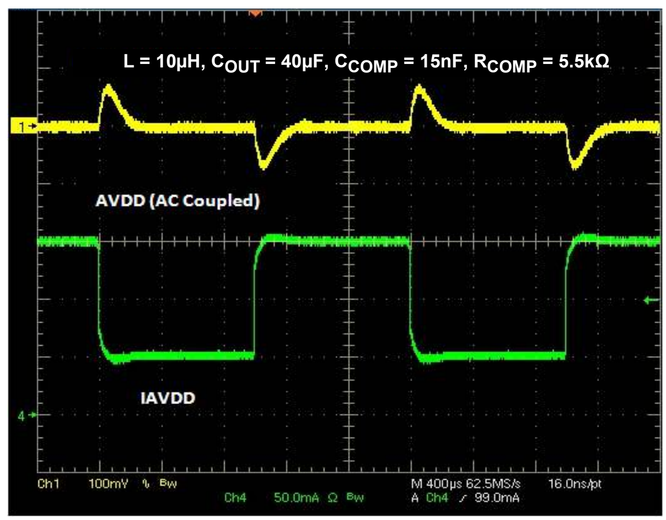


FIGURE 4. BOOST CONVERTER TRANSIENT RESPONSE

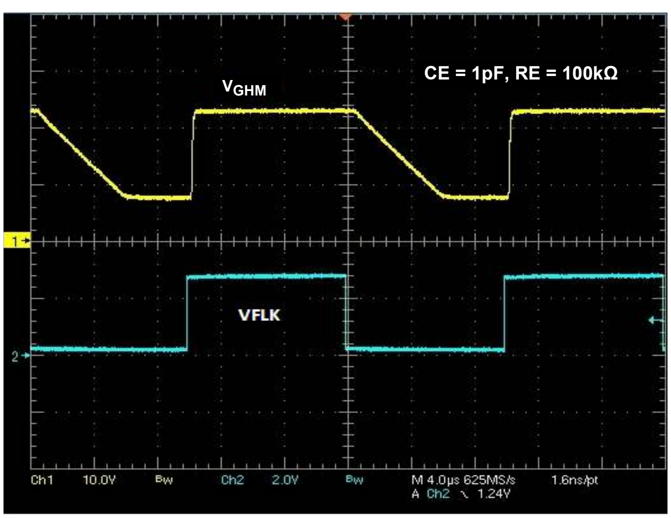


FIGURE 5. GPM CIRCUIT WAVEFORM

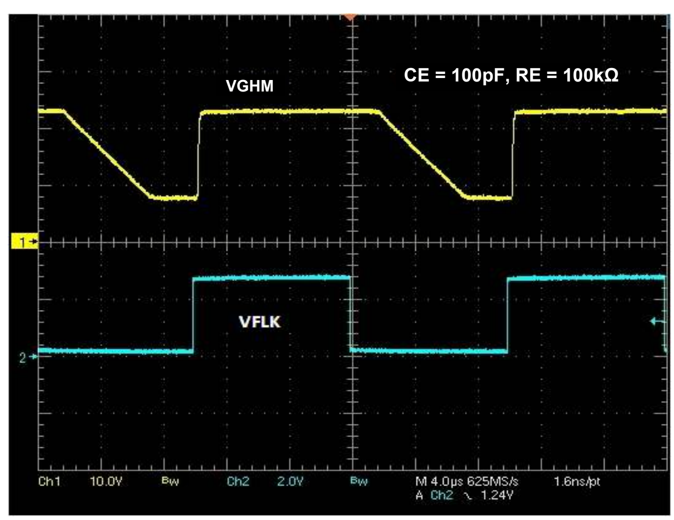


FIGURE 6. GPM CIRCUIT WAVEFORM

Typical Performance Curves (Continued)

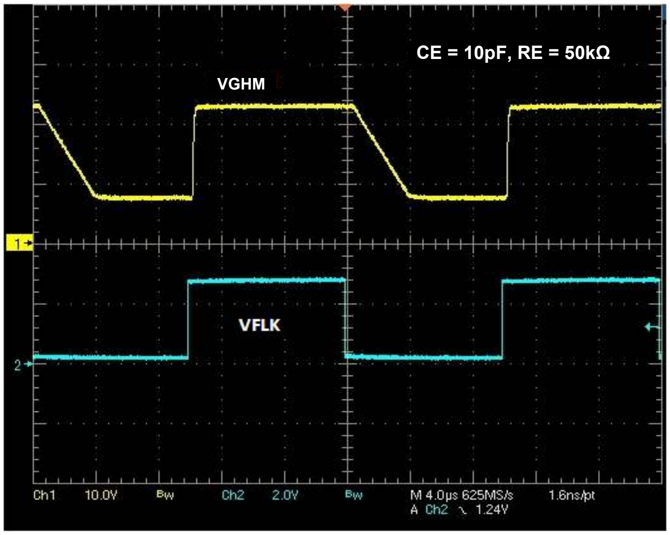


FIGURE 7. GPM CIRCUIT WAVEFORM

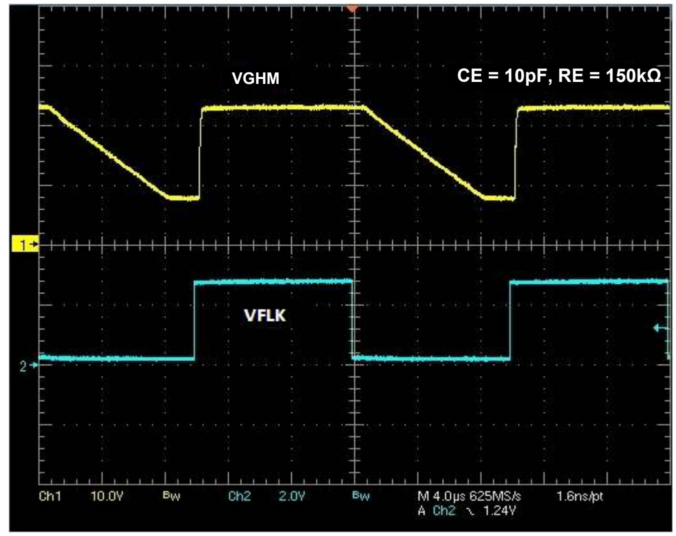


FIGURE 8. GPM CIRCUIT WAVEFORM

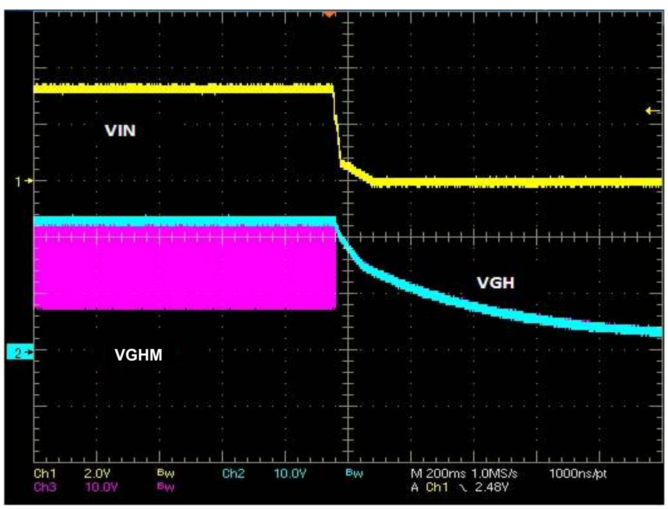


FIGURE 9. V_{GHM} FOLLOWS V_{GH} WHEN THE SYSTEM POWERS OFF

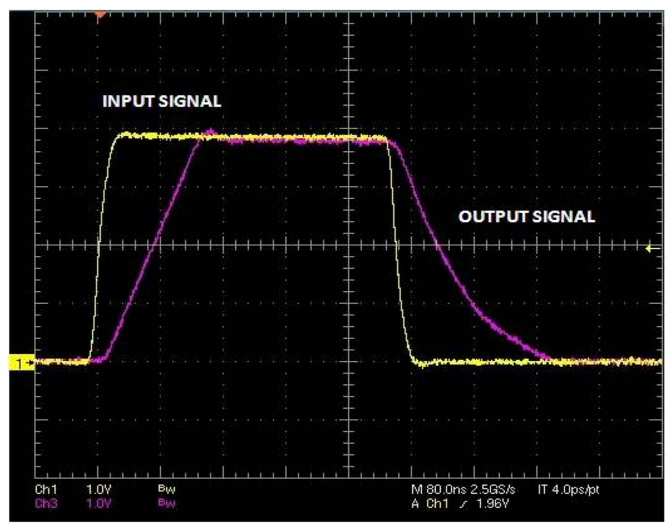


FIGURE 10. VCOM RISING SLEW RATE

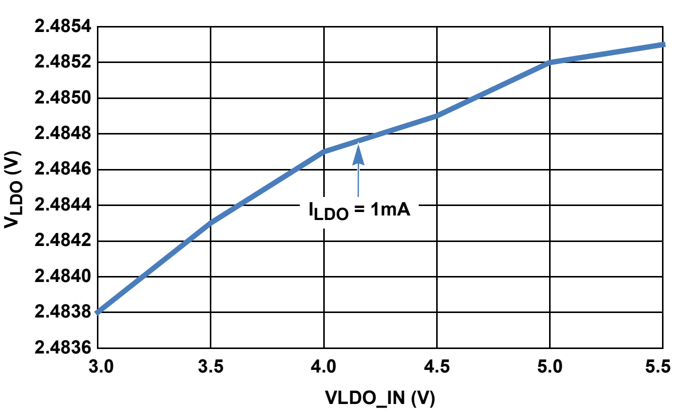


FIGURE 11. LDO LINE REGULATION vs V_{IN}

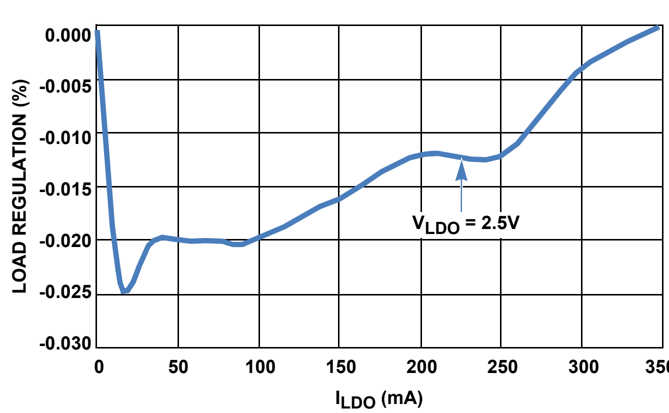


FIGURE 12. LDO LOAD REGULATION vs I_{LDO}

Applications Information

Enable Control

With V_{IN} > UVLO, only the Logic output channel is activated. All other functions in ISL78419 are shut down when the enable pin is pulled down. When the voltage at the enable pin reaches high threshold, the whole chip turns on.

Frequency Selection

The ISL78419 switching frequency can be user selected to operate at either constant 600kHz or 1.2MHz. Lower switching frequency can save power dissipation at very light load conditions. Also, low switching frequency more easily leads to discontinuous conduction mode, while higher switching frequency allows for smaller external components, such as inductor and output capacitors, etc. Higher switching frequency will get higher efficiency within some loading ranges depending on V_{IN}, V_{OUT}, and external components, as shown in Figure 1. Connecting the FREQ pin to GND sets the PWM switching frequency to 600kHz, or connecting FREQ pin to V_{IN} for 1.2MHz.

Soft-Start

The soft-start is provided by an internal current source to charge the external soft-start capacitor. The ISL78419 ramps up the current limit from 0A up to the full value, as the voltage at the SS pin ramps from 0V to 0.8V. Hence, the soft-start time is 3.2ms when the soft-start capacitor is 22nF, 6.8ms for 47nF and 14.5ms for 100nF.

Operation

The boost converter is a current mode PWM converter operating at either 600kHz or 1.2MHz. It can operate in both discontinuous conduction mode (DCM) at light load and continuous conduction mode (CCM). In continuous conduction mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by Equation 1:

$$\frac{V_{Boost}}{V_{IN}} = \frac{1}{1-D} \qquad \text{(EQ. 1)}$$

Where D is the duty cycle of the switching MOSFET.

The boost regulator uses a summing amplifier architecture consisting of gm stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle-by-cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined by Equation 2:

$$V_{Boost} = \frac{R_1 + R_2}{R_2} \times V_{FB} \qquad \text{(EQ. 2)}$$

The current through the MOSFET is limited to $1.5A_{PEAK}$.

This restricts the maximum output current (average) based on Equation 3:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \qquad \text{(EQ. 3)}$$

Where ΔI_L is the peak-to-peak inductor ripple current, and is set by Equation 4:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \qquad \text{(EQ. 4)}$$

Where f_S is the switching frequency (600kHz or 1.2MHz).

Capacitor

An input capacitor is used to suppress the voltage ripple injected into the boost converter. The ceramic capacitor with a capacitance larger than 10µF is recommended. The voltage rating of the input capacitor should be larger than the maximum input voltage. Some input capacitors are recommended in Table 1.

TABLE 1. BOOST CONVERTER INPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	MFG	PART NUMBER
10µF/6.3V	0603	TDK	C1608X5R0J106M
10µF/16V	1206	TDK	C3216X7R1C106M
10µF/10V	0805	Murata	GRM21BR61A106K
22µF/10V	1210	Murata	GRB32ER61A226K

Inductor

The boost inductor is a critical part that influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH are used to match the internal slope compensation. The inductor must be able to handle the following average and peak currents shown in Equation 5:

$$I_{LAVG} = \frac{I_O}{1-D} \qquad I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \qquad \text{(EQ. 5)}$$

Some inductors are recommended in Table 2 for different design considerations.

Rectifier Diode

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The reverse voltage rating of this diode should be higher than the maximum output voltage. The rectifier diode must meet the output current and peak inductor current requirements. Table 3 shows some recommendations for boost converter diode.

TABLE 2. BOOST CONVERTER INDUCTOR RECOMMENDATION

INDUCTOR	DIMENSIONS (mm)	MFG	PART NUMBER	NOTE
10µH/ $4A_{PEAK}$	8.3x8.3x4.5	Sumida	CDR8D43-100NC	Efficiency optimization
6.8µH/ $1.8A_{PEAK}$	5.0x5.0x2.0	TDK	PLF5020T-6R8M1R8	
10µH/ $2.2A_{PEAK}$	6.6x7.3x1.2	Cyntec	PCME061B-100MS	PCB space/profile optimization

TABLE 3. BOOST CONVERTER RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	MFG
PMEG2010ER	20V/1A	SOD123W	NXP
MSS1P2U	20V/1A	MicroSMP	VISHAY

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components:

1. The voltage drop due to the inductor ripple current flowing through the ESR of the output capacitor.
2. Charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_s} \qquad \text{(EQ. 6)}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across them increases. C_{OUT} in Equation 6 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at 0V.

Table 4 shows some selections of output capacitors.

TABLE 4. BOOST OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	MFG	PART NUMBER
10µF/25V	1210	TDK	C3225X7R1E106M
10µF/25V	1210	Murata	GRM32DR61E106K

Compensation

The boost converter of ISL78419 can be compensated by an RC network connected from the COMP pin to ground. A 15nF and 5.5kΩ RC network is used in the evaluation. The larger value resistor and lower value capacitor can lower the transient overshoot, however, at the expense of the stability of the loop.

Linear Regulator (LDO)

The ISL78419 includes an LDO with adjustable output. It can supply current up to 350mA. The output voltage is adjusted by connection of the ADJ pin.

The efficiency of the LDO depends on the difference between input voltage and output voltage (Equation 7) by assuming LDO quiescent current is much lower than LDO output current:

$$\eta(\%) = \left(\frac{V_{LDO\_IN}}{V_{LDO\_OUT}}\right) \times 100\% \qquad \text{(EQ. 7)}$$

The less difference between input and output voltage, the higher efficiency it is.

Ceramic capacitors are recommended for the LDO input and output capacitors. Intersil recommends an output capacitor within the 1µF to 4.7µF range and a maximum feedback resistor impedance of 20kΩ. Larger capacitors help to reduce noise and deviation during transient load change. Some capacitors are recommended in Table 5.

TABLE 5. LDO OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	MFG	PART NUMBER
1µF/10V	0603	TDK	C1608X7R1A105K
1µF/6.3V	0603	MURATA	GRM188R70J105K
2.2µF/6.3V	0603	TDK	C1608X7R0J225K

Supply Monitor Circuit

The Supply Monitor circuit monitors the voltage on VDIV, and sets open-drain output RESET low when VDIV is below 1.28V (rising) or 1.22V (falling).

There is a delay on the rising edge, controlled by a capacitor on CD2. When VDIV exceeds 1.28V (rising), CD2 is charged up from 0V to 1.217V by a 10µA current source. Once CD2 exceeds 1.217V, RESET will go tri-state. When VDIV falls below 1.22V, RESET will become low with a 650Ω pull-down resistance. The delay time is controlled by Equation 8:

$$t_{delay} = 121.7k \times CD2 \qquad \text{(EQ. 8)}$$

For example, the delay time is 12.17ms if the CD2 = 100nF.

Figure 13 shows the Supply Monitor Circuit timing diagram.

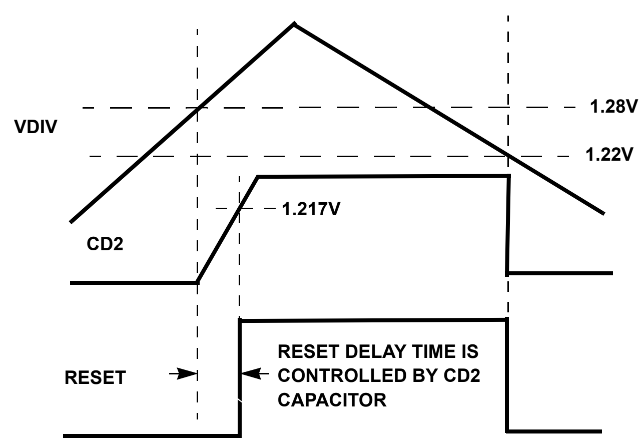


FIGURE 13. SUPPLY MONITOR CIRCUIT TIMING DIAGRAM

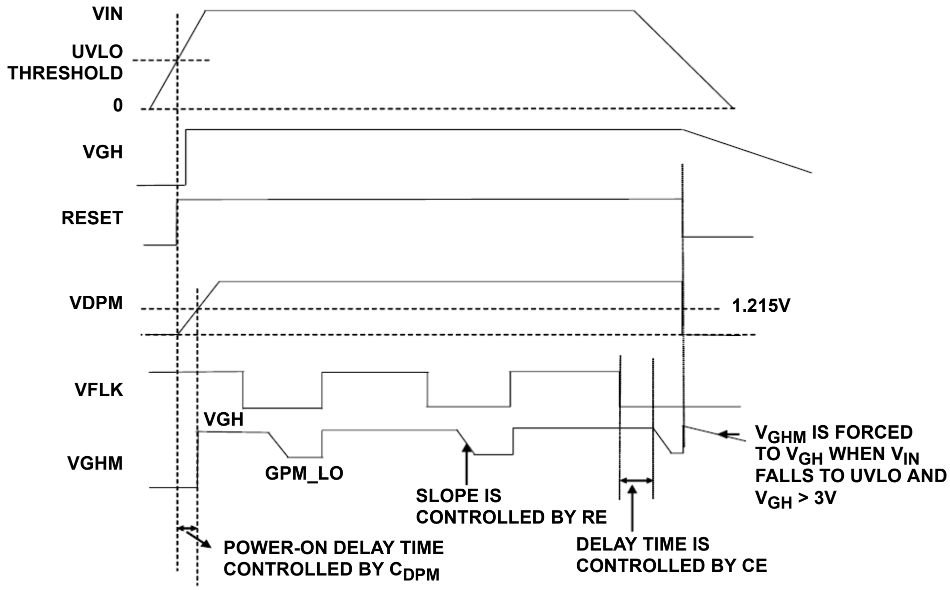


FIGURE 14. GATE PULSE MODULATOR TIMING DIAGRAM

Gate Pulse Modulator Circuit

The gate pulse modulator circuit functions as a three way multiplexer, switching V_{GHM} between ground, GPM_LO and V_{GH}. Voltage selection is provided by digital inputs VDPM (enable) and VFLK (control). High-to-low delay and slew control is provided by external components on pins CE and RE, respectively.

When VDPM is LOW, the block is disabled and VGHM is grounded. When the input voltage exceeds UVLO threshold, VDPM starts to drive an external capacitor. Once VDPM exceeds 1.215V, the GPM circuit is enabled, and the output VGHM is determined by VFLK, RESET signal and V_{GH} voltage. If the RESET signal is high and VFLK is high, V_{GHM} is pulled to V_{GH}. When VFLK goes low, there is a delay controlled by capacitor CE, following which, V_{GHM} is driven to GPM_LO, with a slew rate controlled by resistor RE. Note that GPM_LO is used only as a reference voltage for an amplifier, and thus does not have to source or sink a significant DC current.

Low-to-High transition is determined primarily by the switch resistance and the external capacitive load. High-to-low transition is more complex. Take the case where the block is already enabled (VDPM is high). When VFLK is high, if CE is not externally pulled above threshold voltage 1, pin CE is pulled low. On the falling edge of VFLK, a current is passed into pin CE to charge the external capacitor up to threshold voltage 2, providing a delay which is adjustable by varying the capacitor on CE. Once this threshold is reached, the output starts to be pulled down from V_{GH} to GPM_LO. The maximum slew current is equal to 500/(RE + 40k), and the dv/dt slew rate is Isl/C_{LOAD}, where C_{LOAD} is the load capacitance applied to V_{GHM}. The slew rate reduces as V_{GHM} approaches GPM_LO.

If CE is always pulled up to a voltage above threshold 1, zero delay mode is selected; thus there will be no delay from FLK falling to the point where V_{GHM} starts to fall. Slew down currents will be identical to the previous case.

At power-down, when V_{IN} falls to UVLO, V_{GHM} will be tied to V_{GH} until the V_{GH} voltage falls to 3V. Once the V_{GH} voltage falls below 3V, V_{GHM} will not be actively driven until V_{IN} is driven. Figure 14 shows the V_{GHM} voltage based on V_{IN}, V_{GH} and RESET.

VCOM Amplifier

The VCOM amplifier is designed to control the voltage on the back plane of an LCD display. This plane is capacitively coupled to the pixel drive voltage, which alternately cycles positive and negative at the line rate for the display. Thus, the amplifier must be capable of sourcing and sinking pulses of current, which can occasionally be quite large (in the range of 100mA for typical applications).

The ISL78419 VCOM amplifier's output current is limited to 225mA typical. This limit level, which is roughly the same for sourcing and sinking, is included to maintain reliable operation of the part. It does not necessarily prevent a large temperature rise if the current is maintained. (In this case, the whole chip may be shut down by the thermal trip to protect functionality.) If the display occasionally demands current pulses higher than this limit, the reservoir capacitor will provide the excess and the amplifier will top the reservoir capacitor back up once the pulse has stopped. This will happen in the µs time scale in practical systems and for pulses 2 or 3 times the current limit; the VCOM voltage will have settled again before the next line is processed.

DCP Memory Description

The ISL78419 contains 1 non-volatile byte known as the Initial Value Register (IVR). It is accessed by the I^2C interface operations with Address 00h. The IVR contains the value that is loaded into the volatile Wiper Register (WR) at power-up.

The volatile WR, and the non-volatile IVR of a DCP are accessed with the same address.

The Access Control Register (ACR) determines which word at address 00h is accessed (IVR or WR). The volatile ACR must be set as follows:

- When the ACR is all zeroes, which is the default at power-up:
  - A read operation to address 0 outputs the value of the non-volatile IVR
  - A write operation to address 0 writes the identical values to the WR and IVR of the DCP
- When the ACR is 80h:
  - A read operation to address 0 outputs the value of the volatile WR
  - A write operation to address 0 only writes to the volatile WR

It is not possible to write to an IVR without writing the same value to its WR.

00h and 80h are the only values that should be written to address 2. All other values are reserved and must not be written to address 2.

TABLE 6. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
2	-	ACR
1	Reserved	
0	IVR	WR

WR: Wiper Register, IVR: Initial Value Register.

I^{2}C Serial Interface

The ISL78419 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data on to the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the DCP of the ISL78419 operates as a slave device in all applications. The fall and rise time of SDA and SCL signal should be in the range listed in Table 8. Capacitive load on I^{2}C bus is also specified in Table 8.

All communication over the I^{2}C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 15). On power-up of the ISL78419, the SDA pin is in the input mode.

All I^{2}C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. The DCP continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 15). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I^{2}C interface must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA while SCL is high (see Figure 15). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only places the device in its standby mode. A STOP condition during a write operation to a non-volatile write byte, initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK (Acknowledge) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 16).

The ISL78419 DCP responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL78419 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 0101000 as the seven MSBs. The LSB is in the Read/Write bit. Its value is "1" for a Read operation, and "0" for a Write operation (see Table 7).

TABLE 7. IDENTIFICATION BYTE FORMAT

0	1	0	1	0	0	0	R/$\overline{W}$
(MSB)							(LSB)

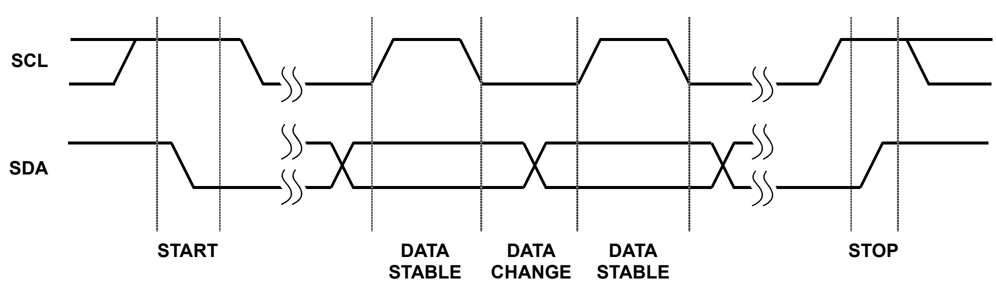


FIGURE 15. VALID DATA CHANGES, START AND STOP CONDITIONS

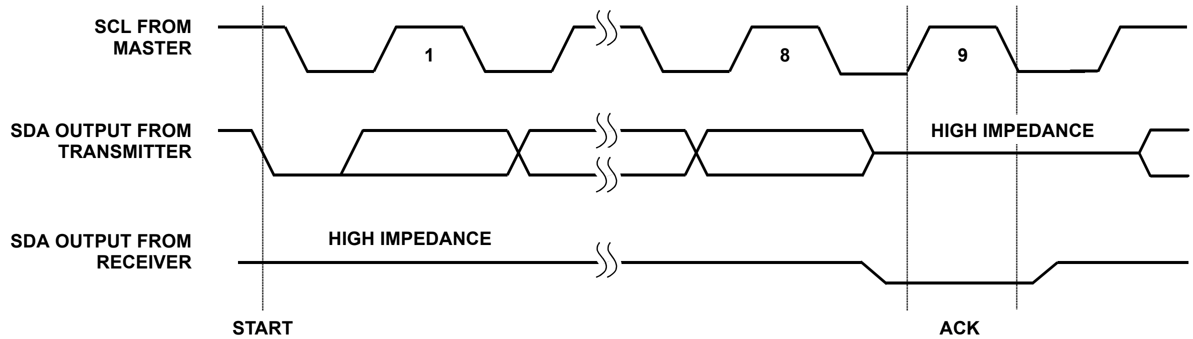


FIGURE 16. ACKNOWLEDGE RESPONSE FROM RECEIVER

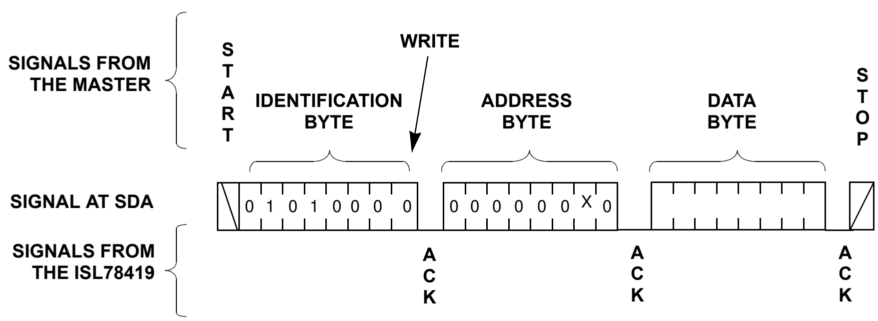


FIGURE 17. BYTE WRITE SEQUENCE

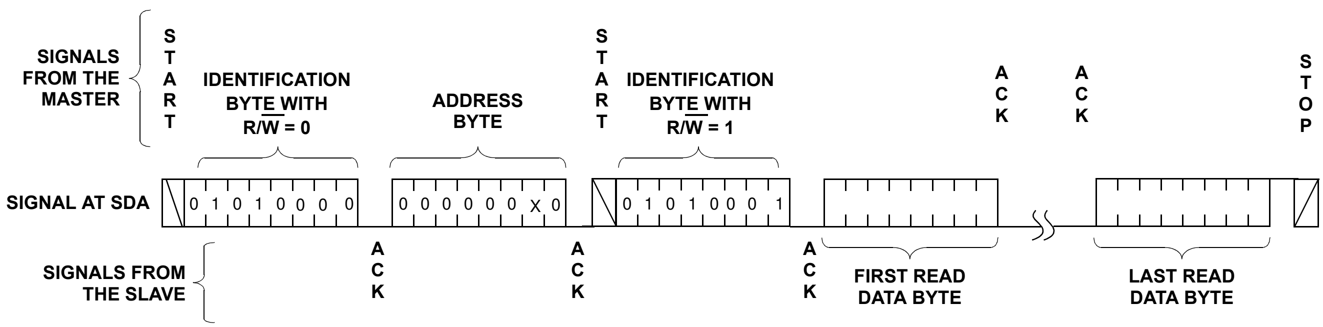


FIGURE 18. READ SEQUENCE

Write Operation

A write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition (see Figure 17). After each of the three bytes, the ISL78419 responds with an ACK. At this time, if the Data Byte is to be written only to volatile registers, the device enters its standby state. If the Data Byte is to be written also to non-volatile memory, the ISL78419 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins and the SDA output is at high impedance state. When the internal non-volatile write cycle is completed, the ISL78419 enters its standby state. The byte at address 02h determines if the Data Byte is to be written to volatile and/or non-volatile memory.

Data Protection

A STOP condition also acts as a protection of non-volatile memory. A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0 or 2, the Data Byte is transferred to the Wiper Register (WR) or to the Access Control Register respectively, at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte. If the Address Byte is 0, and the Access Control Register is all zeros (default), then the STOP condition initiates the internal write cycle to non-volatile memory.

TABLE 8. I^2C INTERFACE SPECIFICATION

PARAMETER	MIN	TYP	MAX	UNITS
SDA and SCL Rise Time			1000	ns
SDA and SCL Fall Time			300	ns
I^2C Bus Capacitive Load			400	pF

Read Operation

A read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 18). The master initiates the operation issuing the following sequence: a START, the Identification Byte with the R/W bit set to "0", an Address Byte, a second START, and a second Identification Byte with the R/W bit set to "1". After each of the three bytes, the ISL78419 responds with an ACK; then the ISL78419 transmits the Data Byte. The master then terminates the read operation (issuing a STOP condition) following the last bit of the Data Byte (see Figure 16).

The byte at address 02h determines if the Data Bytes being read are from volatile or non-volatile memory.

Communication with ISL78419

There are 3 register addresses in the ISL78419, of which two can be used. Address 00h and address 02h are used to control the device. Address 01h is reserved and should not be used. Address 00h contains the non-volatile Initial Value Register (IVR), and the volatile Wiper Register (WR). Address 02h contains only a volatile word and is used as a pointer to either the IVR or WR.

Register Description: Access Control

The Access Control Register (ACR) is volatile and is at address 02h. It is 8 bits, and only the MSB is significant; all other bits should be zero (0). The ACR controls which word is accessed at register 00h as follows:

- 00h = Non-volatile IVR
- 80h = Volatile WR

All other bits of the ACR should be written 0 or 1. Power-up default for this address is 00h.

Register Description: IVR and WR

The output of the DCP is controlled directly by the WR. Writes and reads can be made directly to this register to control and monitor without any non-volatile memory changes. This is done by setting address 02h to data 80h, then writing the data.

The non-volatile IVR stores the power-up value of the DCP output. On power-up, the contents of the IVR are transferred to the WR.

To write to the IVR, first address 02h is set to data 00h, then the data is written. Writing a new value to the IVR register will set a new power-up position for the wiper. Also, writing to this register will load the same value into the WR as the IVR. Therefore, if a new value is loaded into the IVR, not only will the non-volatile IVR change, but the WR will also contain the same value after the write, and the wiper position will change. Reading from the IVR will not change the WR, if its contents are different.

Writing a new value to the IVR

Write to ACR first

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A	

Then, write to IVR

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A	D0	D7	D6	D5	D4	D3	D2	D1	A	

Note that the WR will also reflect this new value since both registers get writen at the same time

D0:LSB, D7:MSB

Writing a new value to WR only

Write to ACR first

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	

Then, write to WR

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A	D0	D7	D6	D5	D4	D3	D2	D1	A	

Note that the IVR value will NOT change

D0:LSB, D7:MSB

Reading from IVR

Write to the ACR first

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	0	0	0	0	0	0	0	0	A	

Then set the IVR address

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A

Read from the IVR

	0	1	0	1	0	0	0	1	A	D0	D7	D6	D5	D4	D3	D2	D1	

Example 2

Reading from the WR

Write to the ACR first

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	1	0	A	1	0	0	0	0	0	0	0	A	

Then set the WR address

	0	1	0	1	0	0	0	0	A	0	0	0	0	0	0	0	0	A

Read from the WR

	0	1	0	1	0	0	0	1	A	D0	D7	D6	D5	D4	D3	D2	D1	

FIGURE 19.

Initial VCOM Setting

A 256-step resolution is provided under digital control, which adjusts the sink current of the output. The output is connected to an external voltage divider, so that the device will have the capability to reduce the voltage on the output by increasing the output sink current. The equations that control the output are given in the following. The initial setting value is at 128. The WR value is set back to 128 if any error occurs during I^2C read or write communication. When writing to the EEPROM, V_{GH} needs to be higher than 12V when AV_{DD} is 8V. Outside these conditions, writing operations may be not successful. The maximum resistor value of RSET is determined by Equations 9 and 10:

$$RSET > V\_AVDD/(20 \times 100\mu A) \qquad \text{(EQ. 9)}$$

$$IOUT = \frac{255 - Setting}{255} \cdot \frac{V_{AVDD}}{20(RSET)} \qquad \text{(EQ. 10)}$$

Where R_L, R_U and RSET in Equation 11 correspond to R_7, R_8 and R_9 in the “Application Diagram” on page 3.

$$VOUT = \frac{R_L \cdot V_{AVDD}}{(R_U + R_L)} \cdot \left(1 - \frac{255 - Setting}{255} \times \frac{R_U}{20(RSET)}\right) \qquad \text{(EQ. 11)}$$

Start-up Sequence

When V_{IN} rising exceeds UVLO, it takes 120µs to read the settings stored in the chip in order to activate the chip correctly. After all the settings are written in the registers, V_{LOGIC} starts up with a 0.5ms soft-start time. When both VLOGIC is in regulation and EN is high, the boost converter starts up. The Gate Pulse modulator output V_{GHM} is held low until VDPM is charged to 1.215V. The detailed power-on sequence is shown in Figure 20.

Layout Recommendation

The device's performance, including efficiency, output noise, transient response and control loop stability, is affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

Following are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{DC} and V_{REF} bypass capacitors close to the pins.
3. Loops with large AC amplitudes and fast slew rate should be made as small as possible.
4. The feedback network should sense the output voltage directly from the point of load, and be as far away from the LX node as possible.
5. The power ground (PGND) should be connected at the ISL78419 exposed die plate area.
6. The exposed die plate, on the underside of the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB, as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. Minimize feedback input track lengths to avoid switching noise pick-up.

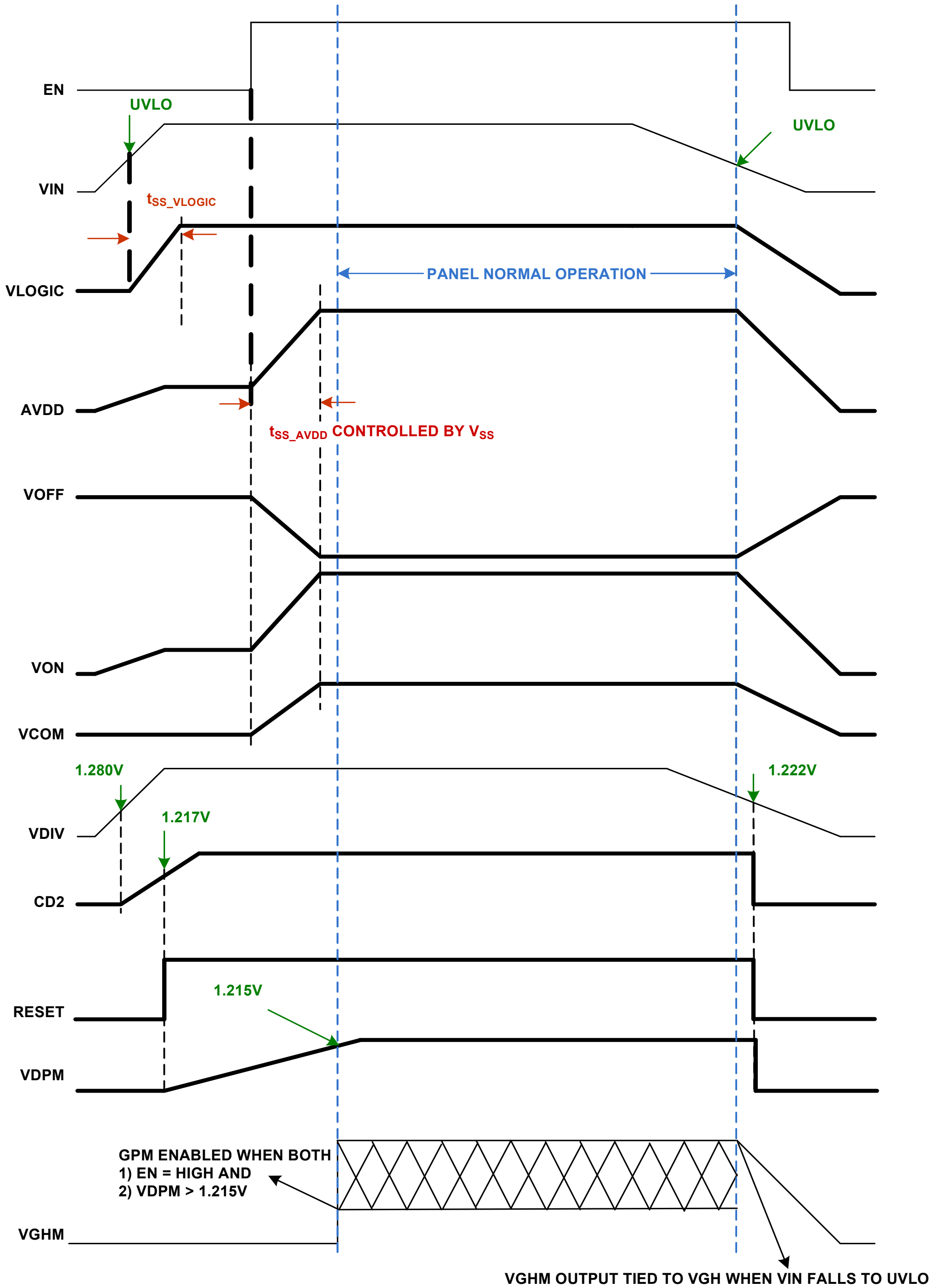


FIGURE 20. ISL78419 POWER-ON/OFF SEQUENCE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
June 27, 2014	FN8292.3	Moved Table of Contents from page 4 to page 2 page 5 - - Replaced Charged Device Model (tested per JESD22-C101)....1kv with Charged Device Model (tested per AEC-Q100-11)....1kv - Thermal Information, changed Pb-Free Reflow Profile link from pb-freereflow.asp to TB493 page 19 - Updated "About Intersil" verbiage
January 24, 2014	FN8292.2	Page 19 - 2nd line of the disclaimer changed from: "Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted" to: "Intersil Automotive Qualified products are manufactured, assembled and tested utilizing TS16949 quality systems as noted" - Updated "About Intersil" verbiage
December 3, 2012	FN8292.1	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

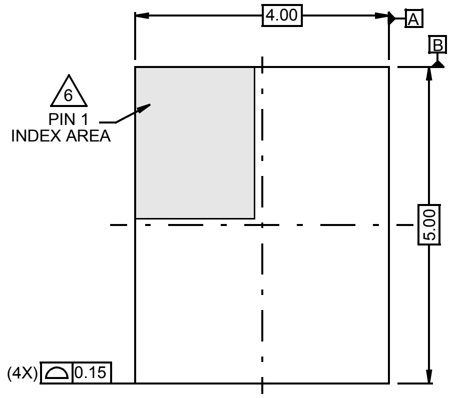
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

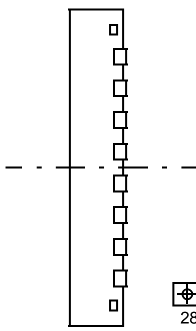
Package Outline Drawing

L28.4x5A

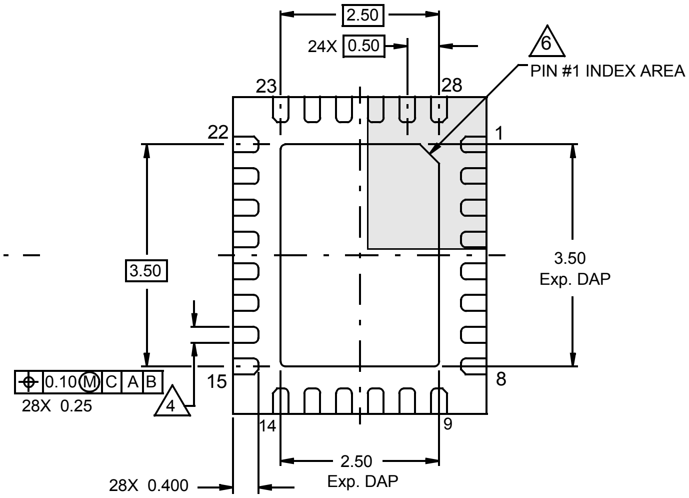
28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 06/08



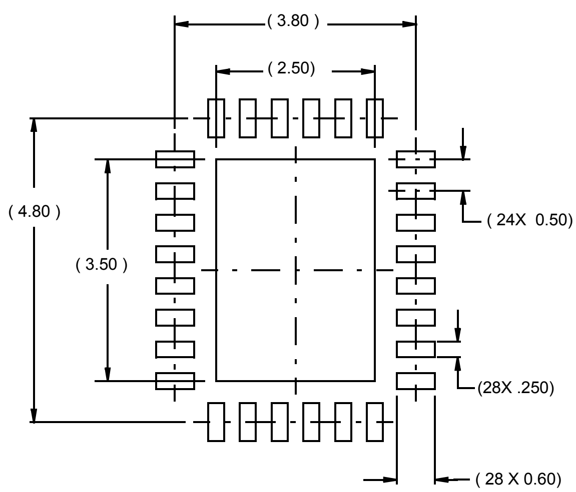
TOP VIEW



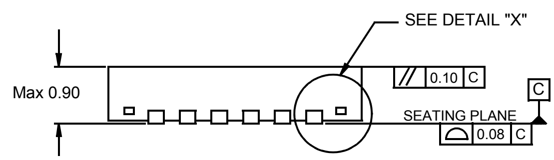
SIDE VIEW



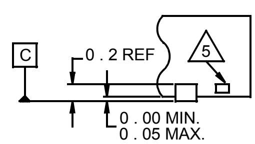
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.