

**54LS/74LS352** *010165*  
**DUAL 4-INPUT MULTIPLEXER**

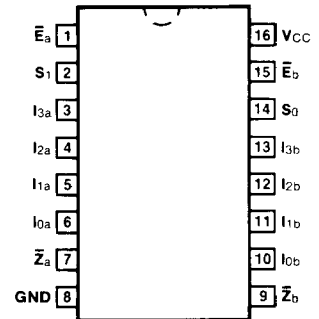
**DESCRIPTION** — The '352 is a very high speed dual 4-input multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The '352 is the functional equivalent of the '153 except with inverted outputs.

- **INVERTED VERSION OF THE '153**
- **SEPARATE ENABLES FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODE LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

**ORDERING CODE:** See Section 9

| PKGS            | PIN OUT | COMMERCIAL GRADE   | MILITARY GRADE   | PKG TYPE |
|-----------------|---------|--|--|----------|
|                 |         | V <sub>CC</sub> = +5.0 V ±5%,<br>T <sub>A</sub> = 0°C to +70°C | V <sub>CC</sub> = +5.0 V ±10%,<br>T <sub>A</sub> = -55°C to +125°C |          |
| Plastic DIP (P) | A       | 74LS352PC  |  | 9B       |
| Ceramic DIP (D) | A       | 74LS352DC  | 54LS352DM  | 6B       |
| Flatpak (F)     | A       | 74LS352FC  | 54LS352FM  | 4L       |

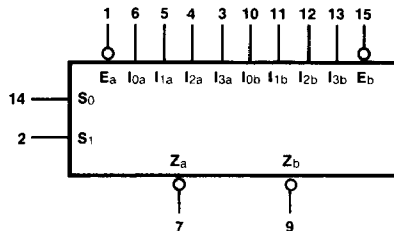
**CONNECTION DIAGRAM  
 PINOUT A**



**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES                         | DESCRIPTION                      | 54/74LS (U.L.) HIGH/LOW |
|-----------------------------------|----------------------------------|-------------------------|
| I <sub>0a</sub> — I <sub>3a</sub> | Side A Data Inputs               | 0.5/0.25                |
| I <sub>0b</sub> — I <sub>3b</sub> | Side B Data Inputs               | 0.5/0.25                |
| S <sub>0</sub> , S <sub>1</sub>   | Common Select Inputs             | 0.5/0.25                |
| $\bar{E}_a$                       | Side A Enable Input (Active LOW) | 0.5/0.25                |
| $\bar{E}_b$                       | Side B Enable Input (Active LOW) | 0.5/0.25                |
| $\bar{Z}_a$ , $\bar{Z}_b$         | Multiplexer Outputs (Inverted)   | 10/5.0<br>(2.5)         |

**LOGIC SYMBOL**



V<sub>CC</sub> = Pin 16  
 GND = Pin 8

**FUNCTIONAL DESCRIPTION** — The '352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs ( $S_0, S_1$ ). The two 4-input multiplexer circuits have individual active LOW Enables ( $\bar{E}_a, \bar{E}_b$ ) which can be used to strobe the outputs independently. When the Enables ( $\bar{E}_a, \bar{E}_b$ ) are HIGH, the corresponding outputs ( $\bar{Z}_a, \bar{Z}_b$ ) are forced HIGH.

The logic equations for the outputs are shown below.

$$\bar{Z}_a = \bar{E}_a \cdot (I_{0a} \cdot S_1 \cdot S_0 + I_{1a} \cdot S_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot S_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\bar{Z}_b = \bar{E}_b \cdot (I_{0b} \cdot S_1 \cdot S_0 + I_{1b} \cdot S_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot S_0 + I_{3b} \cdot S_1 \cdot S_0)$$

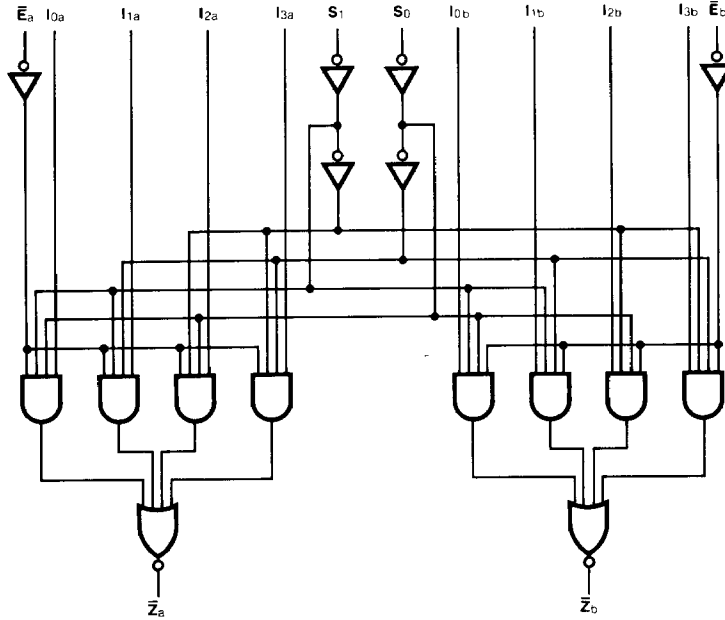
The '352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is a function generator. The '352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

| SELECT INPUTS |       | INPUTS (a or b) |       |       |       | OUTPUT |           |
|---------------|-------|-----------------|-------|-------|-------|--------|-----------|
| $S_0$         | $S_1$ | $\bar{E}$       | $I_0$ | $I_1$ | $I_2$ | $I_3$  | $\bar{Z}$ |
| X             | X     | H               | X     | X     | X     | X      | H         |
| L             | L     | L               | L     | X     | X     | X      | H         |
| L             | L     | L               | H     | X     | X     | X      | L         |
| H             | L     | L               | X     | L     | X     | X      | H         |
| H             | L     | L               | X     | H     | X     | X      | L         |
| L             | H     | L               | X     | X     | L     | X      | H         |
| L             | H     | L               | X     | X     | H     | X      | L         |
| H             | H     | L               | X     | X     | X     | L      | H         |
| H             | H     | L               | X     | X     | X     | H      | L         |

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| SYMBOL          | PARAMETER            | 54/74LS |     | UNITS | CONDITIONS            |
|-----------------|----------------------|---------|-----|-------|-----------------------|
|                 |                      | Min     | Max |       |                       |
| I <sub>CC</sub> | Power Supply Current |         | 10  | mA    | V <sub>CC</sub> = Max |

AC CHARACTERISTICS: V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C

| SYMBOL                               | PARAMETER   | 54/74LS                |          | UNITS | CONDITIONS      |
|--------------------------------------|---|------------------------|----------|-------|-----------------|
|                                      |   | C <sub>L</sub> = 15 pF |          |       |                 |
|                                      |   | Min                    | Max      |       |                 |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>S <sub>n</sub> to Z <sub>n</sub> |                        | 22<br>38 | ns    | Figs. 3-1, 3-20 |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>E <sub>n</sub> to Z <sub>n</sub> |                        | 15<br>20 | ns    | Figs. 3-1, 3-5  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>I <sub>n</sub> to Z <sub>n</sub> |                        | 12<br>12 | ns    | Figs. 3-1, 3-4  |