Electra House, 32 Southtown Road Great Yarmouth, Norfolk NR31 0DU, England Telephone +44 (0)1493 602602 Email:sales@midasdisplays.com www.midasdisplays.com

MCCOG128064D6W-FPTLW	128 x 64	N/A	LCD Module				
	Specification						
Version: 1		Date: 30/10/202	20				
	Revision						
1 27/10/202	0 First Is:	sue					

Display F					
Resolution	128 x 64				
Appearance	Black on White				
Logic Voltage	3V				
Interface	Parallel / SPI	R	COHS		
Font Set	N/A	Parallel / SPI N/A Transflactive			
Display Mode	Transflective		mphant		
LC Type	FSTN				
Module Size	4 <mark>5</mark> .00 x 40.00 x 10.40 <mark>mm</mark>				
Operating Temperature	-20°C ~ +7 <mark>0</mark> °C				
Construction	COG	Box Quantity	Weight / Display		
LED Backlight	White				

*- For full design functionality, please use this specification in conjunction with the ST7565R specification. (Provided Separately)

Display Accessories					
Part Number	Description				

Optional Variants						
Appearances	Voltage					

1. FUNCTIONS & FEATURES

• MCCOG128064D6W-FPTLW Series LCD Type:

• Viewing Direction : 6 O'clock

• Driving Scheme : 1/65 Duty Cycle, 1/9 Bias

• Power Supply Voltage(Typ.) : 3.0 V

■ LCD Operation Voltage :9.0 V

• Display Contents :128x64 Dots

Backlight : LED,Lightguide,White

• Operating temperature :-20°C \sim +70°C

• Storage temperature :-30°C \sim +80°C

RoHS Compliant

2. MECHANICAL SPECIFICATIONS

• Module Size: $: 45.0(L) \times 40.00(W) \times 10.4(T) \text{mm}$ (without FPC)

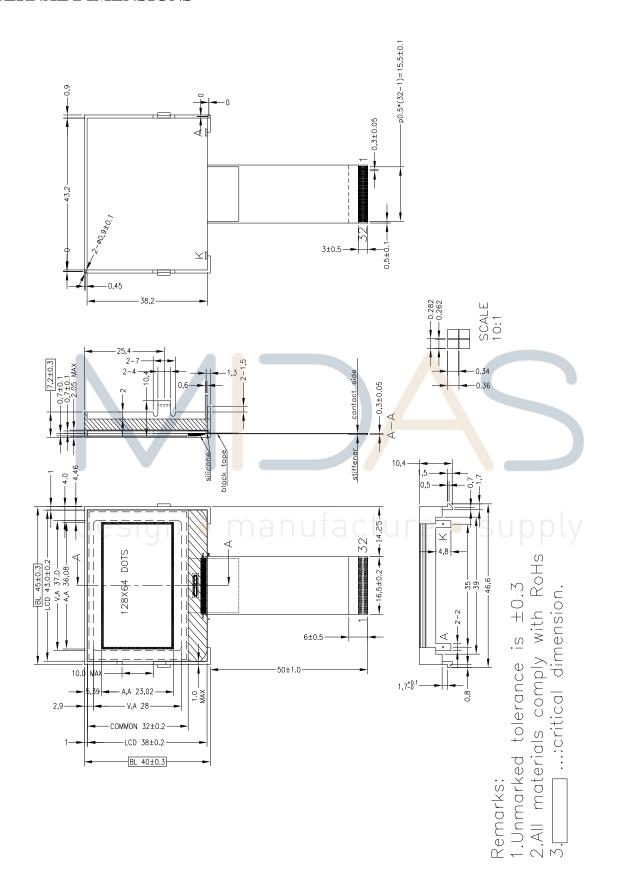
• Viewing Area Size: : 37.00(W) x 28.00(H) mm

• Active Area Size : 36.08(W) x 23.02(H)mm

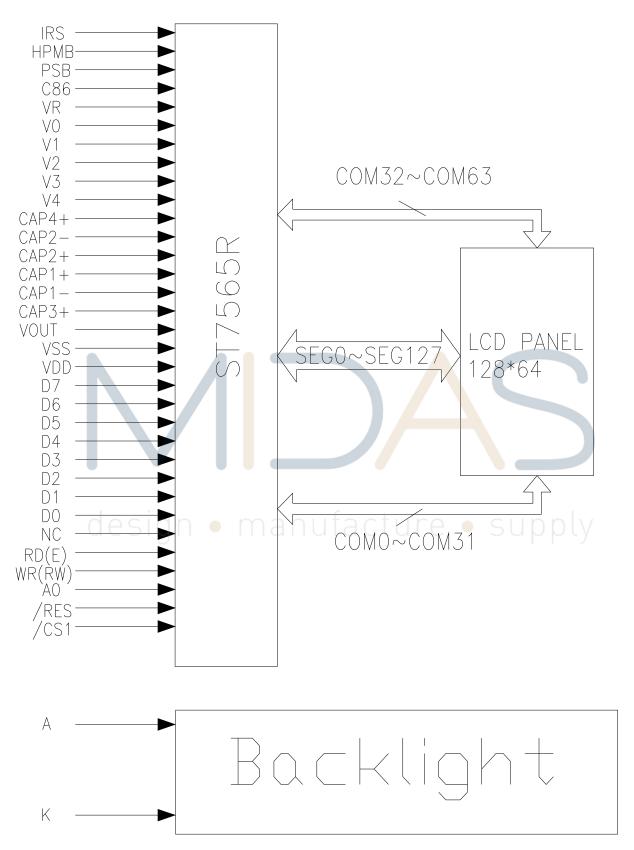
• Dot pitch: : 0.282(W) x 0.36(H)mm

• Dot Size: : 0.262(W) x 0.34(H) mm

EXTERNAL DIMENSIONS



BLOCK DIAGRAM



PIN DESCRIPTION

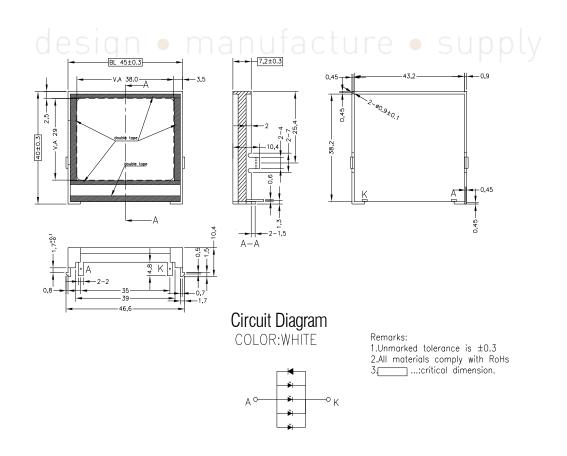
Pin No.	Name	Description
		This terminal selects the resistors for the V0 voltage level adjustment.
1	IRS	IRS = "H": Use the internal resistors IRS = "I": Do not use the internal resistors. The VO veltage level is
		IRS = "L": Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal
		This is the power control terminal for the power supply circuit for liquid crystal drive.
2	HPMB	/HPM = "H": Normal mode
		/HPM = "L": High power mode (suggested) This pin configures the interface to be parallel mode or serial mode.
3	PSB	P/S = "H": Parallel data input/output.
_		P/S = "L": Serial data input.
4	G0.6	This is the MPU interface selection pin.
4	C86	C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 Series MPU interface.
5	VD	This is the internal-output VREG power supply for the LCD power supply voltage
3	VR	regulator.
6	V0	
7	V1	
8	V2	LCD driver supplies voltages
9	V3	
10	V4	
11	CAP4+	
12	CAP2-	
13	CAP2+	
14	CAP1+	DC/DC voltage converter.
15	CAP1-	
16	CAP3+	
17	VOUT	cian a manufacture a cunnly
18	VSS	Ground
19	VDD	Voltage supply
20	D7	
21	D6	
22	D5	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU
23	D4	data bus. When the serial interface (SPI-4) is selected (P/S = "L"):
24	D3	D7 : serial data input (SI) ; D6 : the serial clock input (SCL).
25	D2	D0 to D5 should be connected to VDD or floating.
26	D1	When the chip select is not active, D0 to D7 are set to high impedance.
27	D0	
41	טע	• When connected to 8080 series MPU, this pin is treated as the "/RD" signal of the 8080
		MPU and is LOW-active.
28	RD(E)	The data bus is in an output status when this signal is "L".
	112 (2)	• When connected to 6800 series MPU, this pin is treated as the "E" signal of the 6800 MPU and is HIGH-active.
		This is the enable clock input terminal of the 6800 Series MPU.
		• When connected to 8080 series MPU, this pin is treated as the "/WR" signal of the 8080
		MPU and is LOW-active.
29	WR(RW)	The signals on the data bus are latched at the rising edge of the /WR signal. • When connected to 6800 series MPU, this pin is treated as the "R/W" signal of the 6800
29	** 1.(1.**)	MPU and decides the access type:
		When R/W = "H": Read.
		When R/W = "L": Write.

30	A0	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
31	/RES	This is the chip select signal.
32	/CS1	The RESET signal

A	Supply voltage for backlight LED+
K	Supply voltage for backlight LED-

BACKLIGHT CHARACTERISTICS

Item	Symbol	min.	typ.	max.	Unit	Condition
Forward Voltagt	Vf	2. 9	3. 1	3. 3	V	
Power Dissipation	Pd	174	186	198	mW	
Luminous Uniformity	ΔLv	70			%	If= 60 mA
Luminance	Lv	420	500		cd/m ²	
Color Coordinate	Х	0. 260		0.30		T=25° C
	Y	0. 270		0. 31		1 20
Lifetime		50	0000h		Hours	



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD	-0.3 ~ 3.6	V
Power supply voltage (VDD standard)	V0,VOUT	-0.3 ~ 13.5	V
Power supply voltage (VDD standard)	V1, V2, V3, V4	-0.3 to V0	V
Operating temperature	TOPR	-20 to +70	°C
Storage temperature	TSTR	-30 to +80	°C

ELECTRICAL CHARACTERISTICS

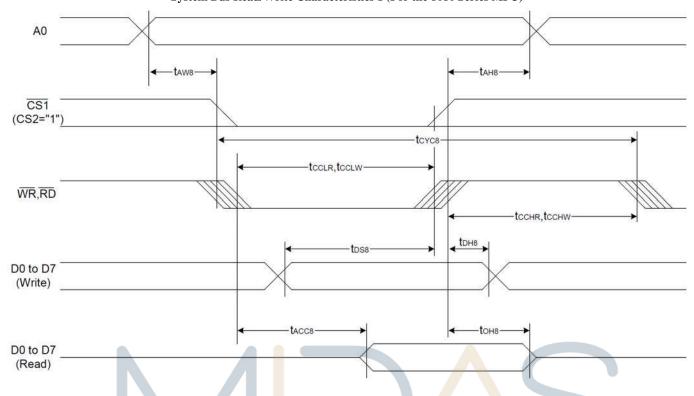
1. DC CHARACTERISTICS

Item	Sym	Condition	STA	units		
Item	bol	Condition	Min.	Typ.	Max.	uiiits
Operating Voltage	V_{DD}	Relative to VSS	2.7	3.0	3.3	
LCD driving voltage	V_{LCD}	Relative to VSS	8.7	9.0	9.3	
High-level Input Voltage	V_{IHC}		0.8 x VDD		VDD	V
Low-level Input Voltage	V_{ILC}		VSS		0.2 x VDD	v
High-level Output Voltage	V _{OHC}	IOH = -0.5 mA	0.8 x VDD		VDD	
Low-level Output Voltage	V _{OLC}	IOH = -0.5 mA	VSS		0.2 x VDD	
Consumption current	I_{DD}			TBD		mA

design • manufacture • supply

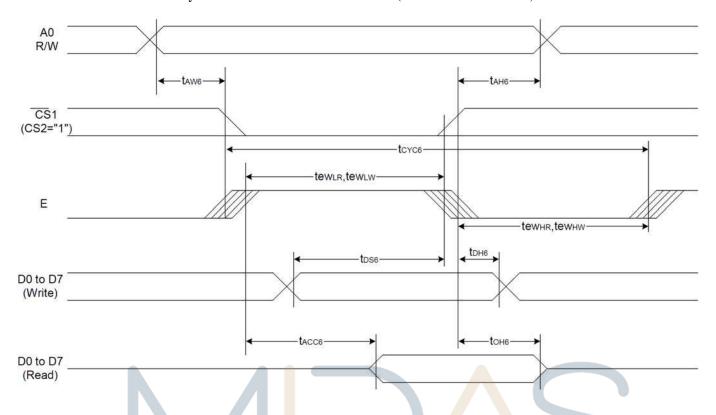
2. AC CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)



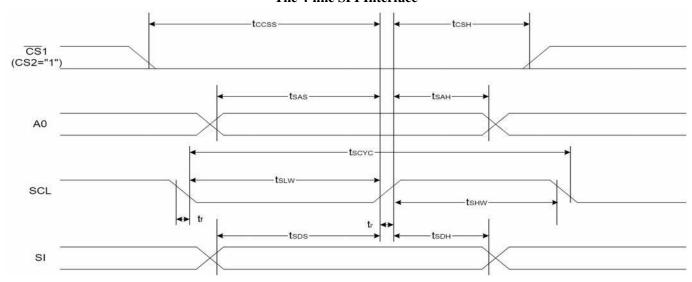
Item	Signal Sym	Symbol	ool Condition	Rati	Units	
itelii	Signal	Symbol	Condition	Min.	Max.	Ullits
Address hold time		taн8		0		
Address setup time	A0	t _{AW8}		0	_	
System cycle time		tcyc8	_	240	_]
Enable L pulse width (WRITE)	WR	tccLw	lacture •	580	рц]
Enable H pulse width (WRITE)	VVIX	t ccHW		80	_]
Enable L pulse width (READ)	RD	tcclr		140	_	Ns
Enable H pulse width (READ)	ND ND	t cchr		80		
WRITE Data setup time		t _{DS8}		40	_]
WRITE Address hold time	D0 to D7	t DH8		0	_]
READ access time	50 10 57	tacc8	C _L = 100 pF		70]
READ Output disable time		toн8	CL = 100 pF	5	50	

System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)



Itom	Signal Symbo		Condition	Rati	Units	
Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		tah6		0	-	
Address setup time	A0	taw6		0	_	
System cycle time 🗍 🖯 S 📗		tcyc6	facture •	240	рIJ]
Enable L pulse width (WRITE)		tewlw		80	1]
Enable H pulse width (WRITE)	VVIX	tewnw		80	_	
Enable L pulse width (READ)	RD	tewlr		80	_	ns
Enable H pulse width (READ)	KD.	tewhr		140		
WRITE Data setup time		tDS6		40	_	
WRITE Address hold time	D0 to D7	tDH6		0	_]
READ access time	ים מו טע	tacc6	C _L = 100 pF		70]
READ Output disable time		toн6	C _L = 100 pF	5	50]

The 4-line SPI Interface

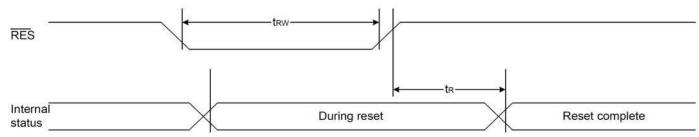


Item	Signal	Signal Symbol Condition		Rati	Units		
item	Signai	Symbol	Condition	Min.	Max.	Units	
4-line SPI Clock Period		Tscyc		50	_		
SCL "H" pulse width	SCL	Tshw		25	_]	
SCL "L" pulse width		TsLW		25		1	
Address setup time	A0	Tsas		20		1	
Address hold time	AU	Tsah		10	_	ns	
Data setup time	SI	Tsds		20]	
Data hold time	5	Тѕон		10			
CS-SCL time	cs	Tcss		20	-		
CS-SCL time	CS	Tesh		40		1	

l Ham.	Cianal	Cumbal	Condition	Rating Max.		Units		
ltem	Signal	Symbol	Condition					
4-line SPI Clock Period		Tscyc	Carc	200	7			
SCL "H" pulse width	SCL	Тѕнѡ		80	·—			
SCL "L" pulse width		Tstw		80		ns		
Address setup time	A0	Tsas		60	_			
Address hold time	A0	Тѕан		30				
Data setup time	CI.	Tsps		60	22-27			
Data hold time	SI	Тѕон		30	-	7		
CS-SCL time	00	Tcss		40				
CS-SCL time	cs	Тсѕн		100				

 $^{^{\}star}1$ The input signal rise and fall time (tr, tf) are specified at 15 ns or less. $^{\star}2$ All timing is specified using 20% and 80% of VDD as the standard.

Reset Timing

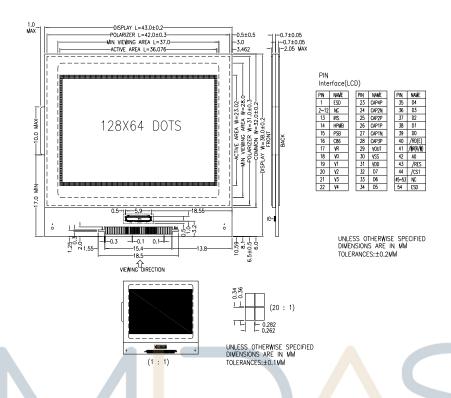


COMMAND TABLE

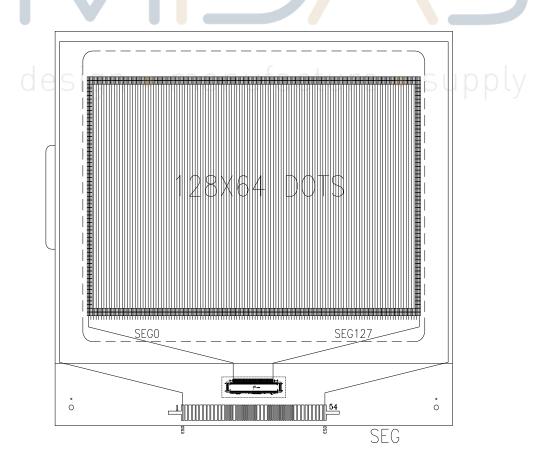
(COMMAND FOR ST7565R)

Command Code													
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	- Function	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON	
(2) Display start line set	0	1	0	0	1		Disp	lay st	art a	ddre	ss	Sets the display RAM display start line address	
(3) Page address set	0	1	0	1	0	1	1	Р	age	addr	ess	Sets the display RAM page address	
(4) Column address set upper bit Column address set lower bit	0	1	0	0	0	0	1	co Le	ast s	add ignif	cant ress icant ress	Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.	
(5) Status read	0	0	1		Sta	itus		0	0	0	0	Reads the status data	
(6) Display data write	1	1	0					W	rite d	ata		Writes to the display RAM	
(7) Display data read	1	0	1					Re	ad d	ata		Reads from the display RAM	
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse	
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse	
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	Display all points 0: normal display 1: all points ON	
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565R)	
(12) Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0	
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write	
(14) Reset	0	.1	0	1	1	1	0	0	0	1	0	Internal reset	
(15) Common output mode select	90	5 [(1	1	0	a	0	* 6) *[*	Select COM output scan direction 0: normal direction 1: reverse direction	
(16) Power control set	0	1	0	0	0	1	0	1	0	pera mod		Select internal power supply operating mode	
(17) V ₀ voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Res	sisto	r ratio	Select internal resistor ratio(Rb/Ra) mode	
(18) Electronic volume mode set Electronic volume	0	1	0	1 0	0	0	0 lectro	0	0	0	1	Set the V ₀ output voltage electronic volume register	
register set (19) Static indicator				_									
ON/OFF Static indicator	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON	
register set				0	0	0	0	0	0	0	Mode		
(20) Booster ratio set	0	1	0	1 0	1	1	1	1	0	0 ste	0 ep-up	select booster ratio 00: 2x,3x,4x 01: 5x	
(21) Power save	0	1	0							V	alue	11: 6x Display OFF and display all	
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	points ON compound command Command for non-operation	
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not	
(-3) 1001												use this command	

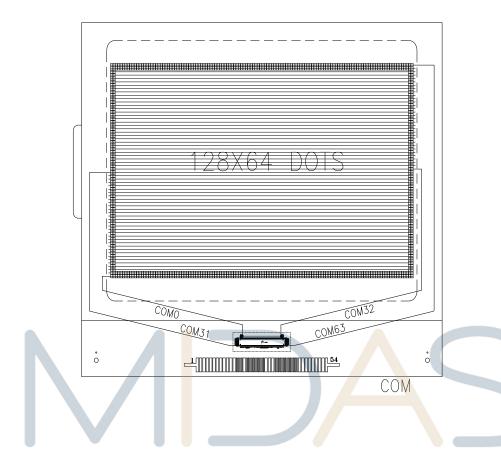
LCD ARTWORK



SEG LAYOUT

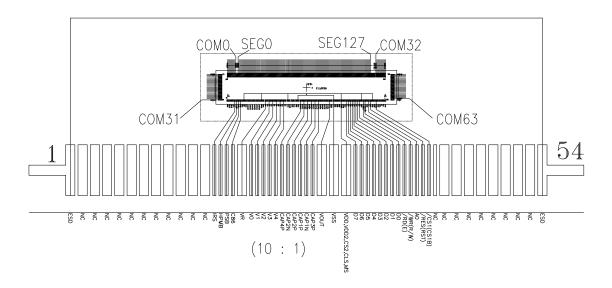


COM LAYOUT



IC LAYOUT

design • manufacture • supply



RELIABILITY TEST

Operating life time: Longer than 50000 hours

(at room temperature without direct irradiation of sunlight)

Reliability characteristics shall meet following requirements.

TEMPERATURE TESTS	NORMAL GRADE					
High temperature storage	+80°C * 96HR					
Low temperature storage	-30°C * 96HR					
High temperature operation	+70°C * 96HR					
Low temperature operation	-20°C * 96HR					
High temperature, High humidity	+60°C 90%RH 96HR					
Thermal shock	-20°C * 30 min ◀ 10s ▼ 5Cycles 70°C * 30 min					
Vibration test	Frequency * Swing * Time 40Hz * 4mm * 4hrs					
Drop test	Drop height * Times 1.0m * 6 times					

QUALITY DESCRIPTION & APPLICATION NOTE

Please refer to "General Inspection Criteria" document

design • manufacture • supply