# Silicon, SPDT Switch, Nonreflective, 100 MHz to 13 GHz

# ADRF5019

## FEATURES

**Nonreflective 50 Ω design**
**Low insertion loss: 0.8 dB at 8 GHz**
**High isolation: 45 dB at 8 GHz**
**High input linearity**
   **P1dB: 39 dBm**
   **IP3: 60 dBm typical**
**High power handling**
   **35 dBm insertion loss path**
   **27 dBm hot switching**
**ESD rating: 2 kV (Class 2) HBM**
**No low frequency spurious**
**0.05 dB RF settling time: 375 ns**
**0.1 dB RF settling time: 300 ns**
**16-lead, 3 mm × 3 mm LFCSP**
**Pin-compatible with HMC1118, low frequency cutoff version**

## APPLICATIONS

**Test instrumentation**
**Microwave radios and very small aperture terminals (VSATs)**
**Military radios, radars, and electronic counter measures (ECMs)**
**Fiber optics and broadband telecommunications**

## GENERAL DESCRIPTION

The ADRF5019 is a nonreflective, single pole, double throw (SPDT) RF switch manufactured in a silicon process.

The ADRF5019 operates from 100 MHz to 13 GHz with better than 0.8 dB insertion loss and 45 dB of isolation at 8 GHz. The ADRF5019 has a nonreflective design, and the RF ports are internally terminated to 50 Ω.

The ADRF5019 switch requires a dual supply voltage of +3.3 V and −2.5 V and positive control voltage inputs. This switch employs complementary metal-oxide semiconductor (CMOS)-compatible and low voltage transistor transistor logic (LVTTL)-compatible controls.
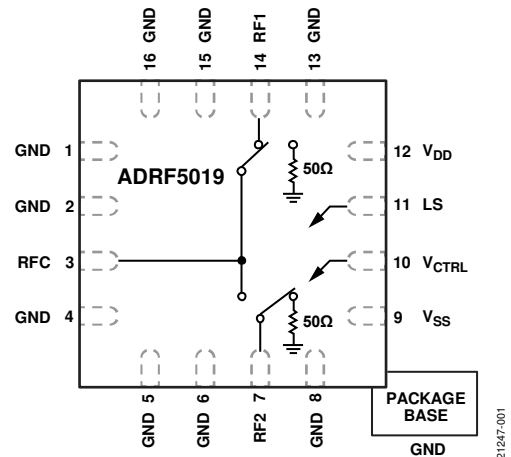
## FUNCTIONAL BLOCK DIAGRAM



*Figure 1.*

The ADRF5019 can also operate with a single positive supply voltage ($V_{DD}$) applied. The negative supply voltage ($V_{SS}$) is tied to ground. Even in single-supply operation mode, the ADRF5019 can cover the 100 MHz to 13 GHz operating frequency and maintain good power handling performance. See the Applications Information section for more details.

The ADRF5019 is pin-compatible with the HMC1118, the low frequency cutoff version, which operates from 9 kHz to 13.0 GHz.

The ADRF5019 comes in a 16-lead, lead frame chip scale package (LFCSP) and operates from −40°C to +105°C.

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## REVISION HISTORY

**8/2019—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL SPECIFICATIONS

$V_{DD}$ = 3.3 V, $V_{SS}$ = −2.5 V, LS = 3.3 V, $V_{CTRL}$ = 0 V or 3.3 V, and $T_{CASE}$ = 25°C in a 50 Ω system, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FREQUENCY RANGE | f | | 100 | | 13,000 | MHz |
| INSERTION LOSS | IL | | | | | |
| Between RFC and RF1 or RFC and RF2 (On) | | 100 MHz to 3 GHz | | 0.6 | | dB |
| | | 100 MHz to 8 GHz | | 0.8 | | dB |
| | | 100 MHz to 10 GHz | | 1.0 | | dB |
| | | 100 MHz to 13 GHz | | 1.5 | | dB |
| RETURN LOSS | RL | | | | | |
| Between RFC and RF1 or RFC and RF2 (On) | | 100 MHz to 3 GHz | | 26 | | dB |
| | | 100 MHz to 8 GHz | | 22 | | dB |
| | | 100 MHz to 13 GHz | | 9 | | dB |
| RF1 or RF2 (Off) | | 100 MHz to 3 GHz | | 26 | | dB |
| | | 100 MHz to 8 GHz | | 14 | | dB |
| | | 100 MHz to 13 GHz | | 5 | | dB |
| ISOLATION | | | | | | |
| Between RFC and RF1 or RCF and RF2 (Off) | | 100 MHz to 3 GHz | | 50 | | dB |
| | | 100 MHz to 8 GHz | | 45 | | dB |
| | | 100 MHz to 10 GHz | | 35 | | dB |
| | | 100 MHz to 13 GHz | | 25 | | dB |
| SWITCHING CHARACTERISTICS | | | | | | |
| Dual Supply | | $V_{DD}$ = 3.3 V, $V_{SS}$ = −2.5 V | | | | |
| Rise Time and Fall Time | $t_{RISE}$, $t_{FALL}$ | 10% to 90% of RF output | | 35 | | ns |
| On Time and Off Time | $t_{ON}$, $t_{OFF}$ | 50% of triggered digital control input voltage ($V_{CTL}$) to 90% of RF output | | 150 | | ns |
| RF Settling Time | | | | | | |
| 0.1 dB | | 50% of triggered $V_{CTL}$ to 0.1 dB of final RF output | | 300 | | ns |
| 0.05 dB | | 50% of triggered $V_{CTL}$ to 0.05 dB of final RF output | | 375 | | ns |
| Single Supply | | $V_{DD}$ = 3.3 V, $V_{SS}$ = 0 V | | | | |
| Rise Time and Fall Time | $t_{RISE}$, $t_{FALL}$ | 10% to 90% of RF output | | 180 | | ns |
| On Time and Off Time | $t_{ON}$, $t_{OFF}$ | 50% of triggered $V_{CTL}$ to 90% of RF output | | 285 | | ns |
| INPUT LINEARITY[1] | | 100 MHz to 13 GHz | | | | |
| Dual Supply | | $V_{DD}$ = 3.3 V, $V_{SS}$ = −2.5 V | | | | |
| Input Compression | | | | | | |
| 0.1 dB | P0.1dB | | | 38 | | dBm |
| 1 dB | P1dB | | | 39 | | dBm |
| Intermodulation Distortion | | | | | | |
| Input Third-Order Intercept | IIP3 | Two tone input power = 12 dBm each tone, Δf = 1 MHz | | 60 | | dBm |
| Single Supply | | $V_{DD}$ = 3.3 V, $V_{SS}$ = 0 V | | | | |
| Input Compression | | | | | | |
| 0.1 dB | P0.1dB | | | 25 | | dBm |
| 1 dB | P1dB | | | 28 | | dBm |
| Intermodulation Distortion | | | | | | |
| Input Third-Order Intercept | IIP3 | Two tone input power = 12 dBm each tone, Δf = 1 MHz | | 55 | | dBm |
| SUPPLY CURRENT | | $V_{DD}$ pin and $V_{SS}$ pin | | | | |
| Positive Supply Current | $I_{DD}$ | | | 20 | | μA |
| Negative Supply Current | $I_{SS}$ | | | 0.5 | | μA |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DIGITAL CONTROL INPUTS | | $V_{CTRL}$ pin and LS pin | | | | |
| Voltage | | | | | | |
| Low | $V_{INL}$ | | 0 | | 0.8 | V |
| High | $V_{INH}$ | | 2 | | 3.3 | V |
| Current | | | | | | |
| Low and High Current | $I_{INL}$, $I_{INH}$ | | | <1 | | µA |
| RECOMMENDED OPERATING CONDITONS | | | | | | |
| Supply Voltage | | | | | | |
| Positive | $V_{DD}$ | | 3.0 | | 3.6 | V |
| Negative | $V_{SS}$ | | −2.75 | | −2.25 | V |
| Digital Control Input Voltage | $V_{CTL}$ | | 0 | | $V_{DD}$ | V |
| RF Input Power, Dual Supply[2] | $P_{IN}$ | $V_{DD}$ = 3.3 V, $V_{SS}$ = −2.5 V, f = 2 GHz, $T_{CASE}$ = 85°C [3] | | | | |
| Insertion Loss Path | | RF signal is applied to RFC or through connected RF1 or RF2 | | | 35 | dBm |
| Isolation Path | | RF signal is applied to the terminated RF1 or RF2 | | | 27 | dBm |
| Hot Switching | | RF signal is present at RFC while switching between RF1 and RF2 | | | 27 | dBm |
| RF Input Power, Single Supply[2] | $P_{IN}$ | $V_{DD}$ = 3.3 V, $V_{SS}$ = 0 V, f = 2 GHz, $T_{CASE}$ = 85°C [3] | | | | |
| Insertion Loss Path | | RF signal is applied to RFC or through connected RF1 or RF2 | | | 27 | dBm |
| Isolation Path | | RF signal is applied to the terminated RF1 or RF2 | | | 22 | dBm |
| Hot Switching | | RF signal is present at RFC while switching between RF1 and RF2 | | | 22 | dBm |
| Case Temperature | $T_{CASE}$ | | −40 | | +105 | °C |

[1] For input linearity performance vs. frequency, see Figure 13 to Figure 20.
[2] For power derating vs. frequency, see Figure 2 and Figure 3. Power derating is applicable for insertion loss path, terminated path, and hot switching power specifications.
[3] For operation at 105°C, the power handling degrades from the $T_{CASE}$ = 85°C specification by 3 dB.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| Positive Supply Voltage | −0.3 V to +3.7 V |
| Negative Supply Voltage | −2.8 V to +0.3 V |
| Digital Control Inputs | |
|     Voltage | −0.3 V to $V_{DD}$ + 0.3 V |
|     Current | 3 mA |
| RF Input Power, Dual Supply[1] ($V_{DD}$ = 3.3 V, $V_{SS}$ = −2.5 V, f = 2 GHz at $T_{CASE}$ = 85°C[2]) | |
|     Insertion Loss Path | 37 dBm |
|     Isolation Path | 28 dBm |
|     Hot Switching | 30 dBm |
| RF Input Power, Dual Supply[1] ($V_{DD}$ = 3.3 V, $V_{SS}$ = 0 V, f = 2 GHz at $T_{CASE}$ = 85°C[2]) | |
|     Insertion Loss Path | 28 dBm |
|     Isolation Path | 23 dBm |
|     Hot Switching | 23 dBm |
| RF Input Power Under Unbiased Condition ($V_{DD}$, $V_{SS}$ = 0 V) | 23 dBm |
| Temperature | |
|     Junction, $T_J$ | 135°C |
|     Storage Range | −65°C to +150°C |
|     Reflow | 260°C |
| Electrostatic Discharge (ESD) Sensitivity | |
| Human Body Model (HBM) | 2 kV (Class 2) |

[1] For power derating vs. frequency, see Figure 2 and Figure 3. Power derating is applicable for insertion loss path, terminated path, and hot switching power specifications.
[2] For operation at 105°C, the power handling degrades from the $T_{CASE}$ = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal resistance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JC}$ is the junction to case bottom (channel to package bottom) thermal resistance.

**Table 3. Thermal Resistance**

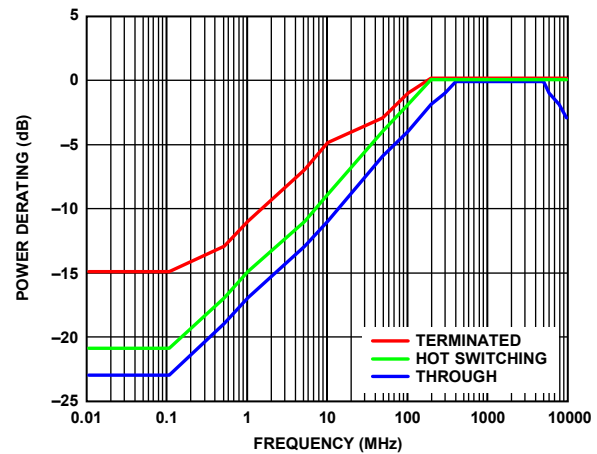| Package Type | $\theta_{JC}$ | Unit |
|---|---|---|
| CP-16-38 | | |
|     Through Path | 106 | °C/W |
|     Terminated Path | 100 | °C/W |

## POWER DERATING CURVES



Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{CASE}$ = 85°C



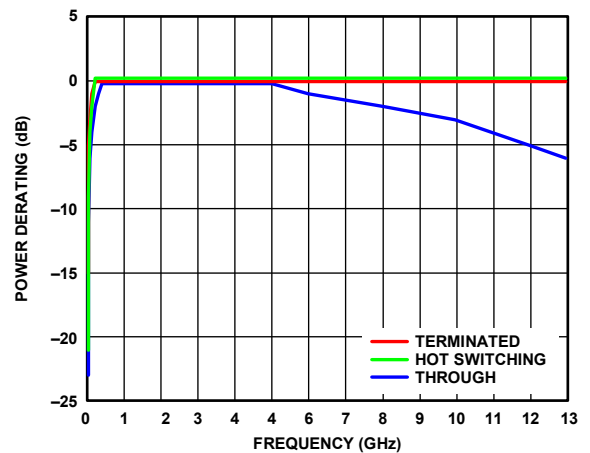Figure 3. Power Derating vs. Frequency, High Frequency Detail, $T_{CASE}$ = 85°C

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

**ADRF5019**
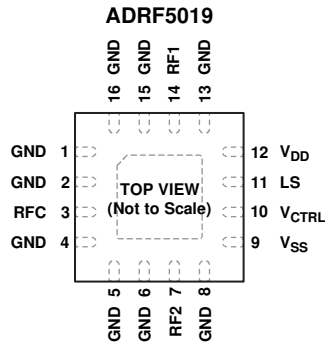


NOTES
1. EXPOSED PAD. THE EXPOSED PAD MUST BE
   CONNECTED TO THE RF AND DC GROUND
   OF THE PCB.

*Figure 4. Pin Configuration (Top View)*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 2, 4 to 6, 8, 13, 15, 16 | GND | Ground. These pins must be connected to the RF and dc ground of the PCB. |
| 3 | RFC | RF Common Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| 7 | RF2 | RF Throw Port 2. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| 9 | $V_{SS}$ | Negative Supply Voltage Pin. See Figure 8 for the interface schematic. |
| 10 | $V_{CTRL}$ | Control Input Pin. See Figure 6 for interface schematic. See Table 5 for the truth table. |
| 11 | LS | Logic Select Input Pin. See Figure 6 for the interface schematic. See Table 5 for the truth table. |
| 12 | $V_{DD}$ | Positive Supply Voltage Pin. See Figure 7 for the interface schematic. |
| 14 | RF1 | RF Throw Port 1. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| | EPAD | Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB. |

## INTERFACE SCHEMATICS
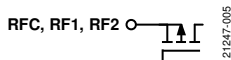


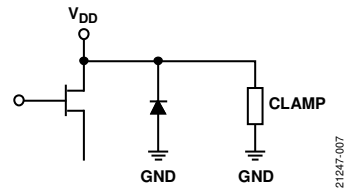*Figure 5. RFC, RF1, and RF2 Pin Interface Schematic*
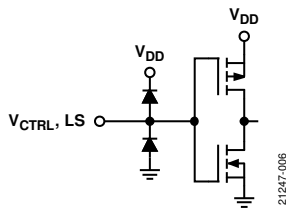


*Figure 7. $V_{DD}$ Pin Interface Schematic*
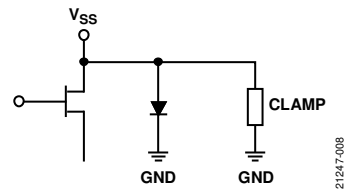


*Figure 6. Digital Pins Interface Schematic*



*Figure 8. $V_{SS}$ Pin Interface Schematic*

# TYPICAL PERFORMANCE CHARACTERISTICS
## INSERTION LOSS, RETURN LOSS, AND ISOLATION

$V_{DD}$ = 3.3 V, $V_{SS}$ = −2.5 V, $V_{CTRL}$ and LS = 0 V or $V_{DD}$, and $T_{CASE}$ = 25°C in a 50 Ω system, unless otherwise noted.
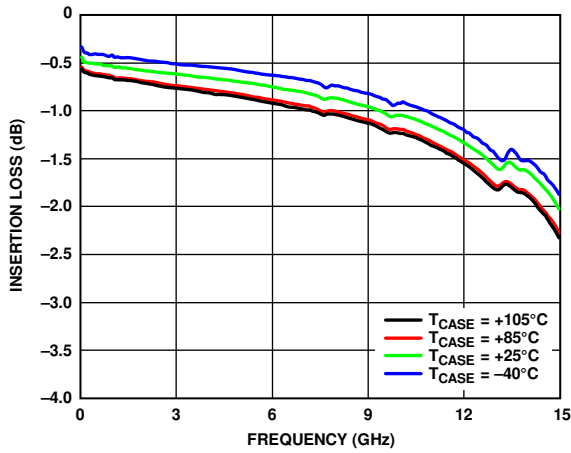


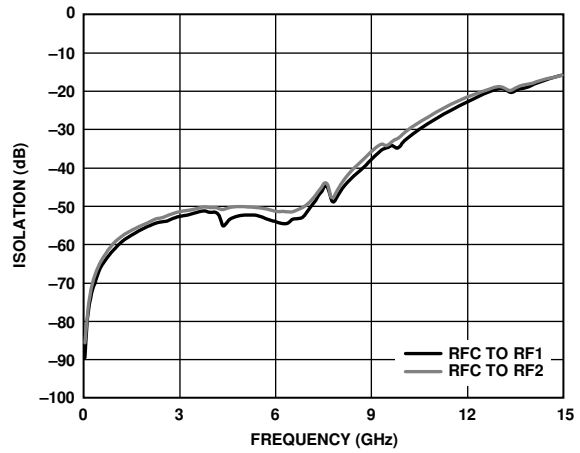*Figure 9. Insertion Loss vs. Frequency over Temperature*



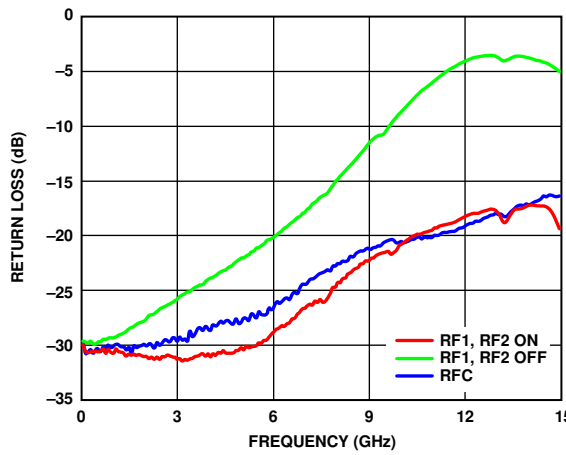*Figure 11. Isolation Between RFC and RFx Ports vs. Frequency*

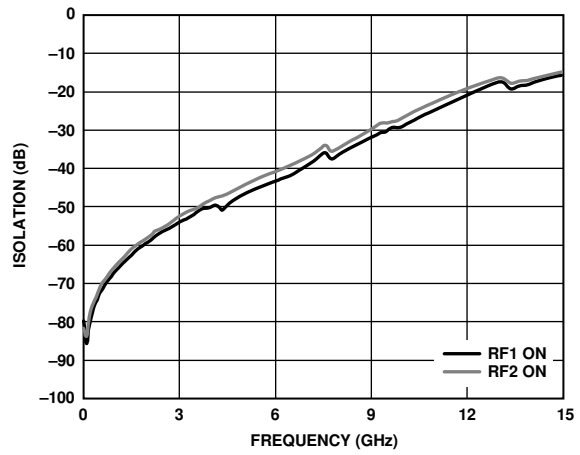

*Figure 10. Return Loss vs. Frequency*



*Figure 12. Isolation Between RF1 and RF2 Ports vs. Frequency*

## INPUT COMPRESSION AND INPUT THIRD-ORDER INTERCEPT

$V_{DD}$ = 3.3 V, $V_{CTRL}$ and LS = 0 V or $V_{DD}$, and $T_{CASE}$ = 25°C in a 50 Ω system, unless otherwise noted. All of the large signal performance parameters are measured on the ADRF5019-EVALZ evaluation board.
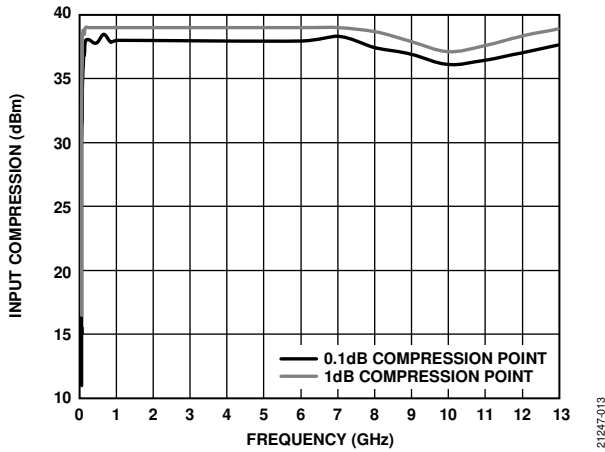


*Figure 13. P0.1dB and P1dB Input Compression vs. Frequency, $V_{SS}$ = −2.5 V*



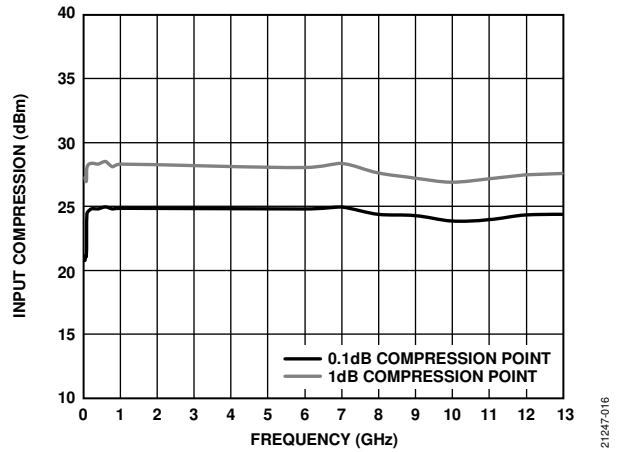*Figure 16. P0.1dB and P1dB Input Compression vs. Frequency, $V_{SS}$ = 0 V*



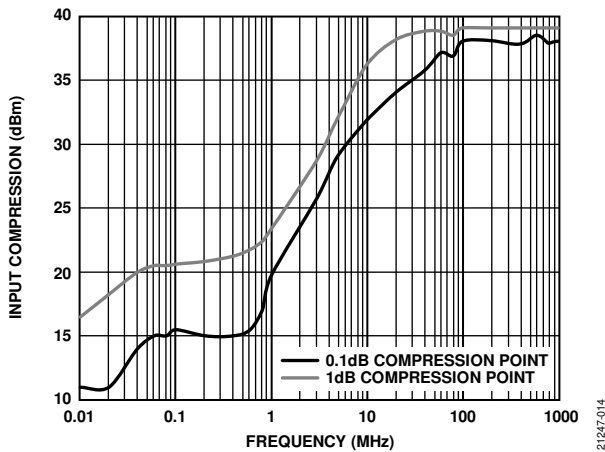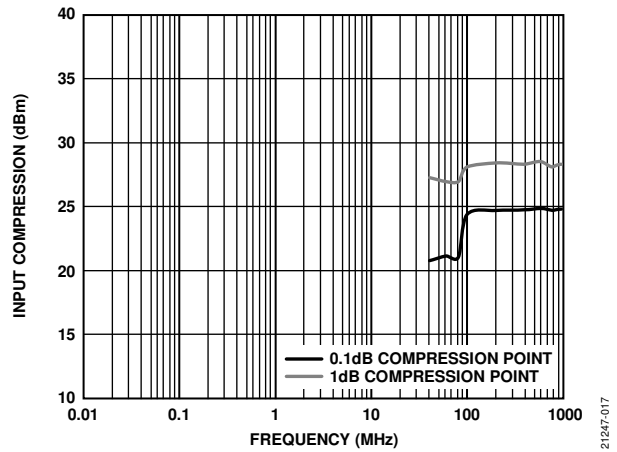*Figure 14. P0.1dB and P1dB Input Compression vs. Frequency (Low Frequency Detail), $V_{SS}$ = −2.5 V*



*Figure 17. P0.1dB and P1dB Input Compression vs. Frequency (Low Frequency Detail), $V_{SS}$ = 0 V*



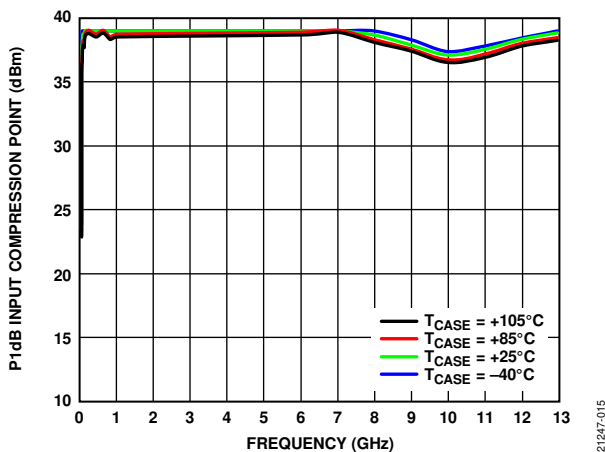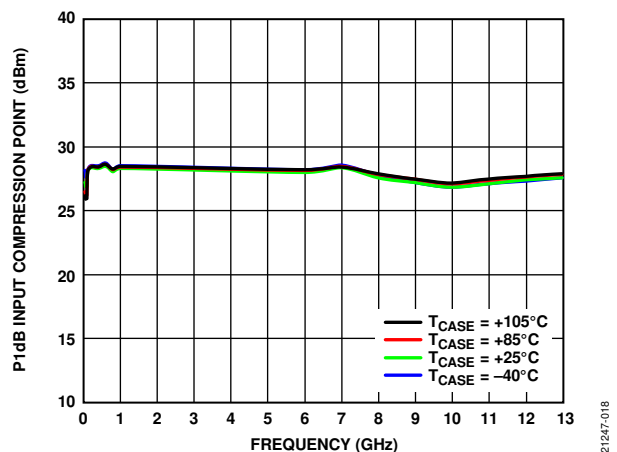*Figure 15. P1dB Input Compression Point vs. Frequency over Temperature, $V_{SS}$ = −2.5 V*



*Figure 18. P1dB Input Compression Point vs. Frequency over Temperature (Low Frequency Detail), $V_{SS}$ = 0 V*
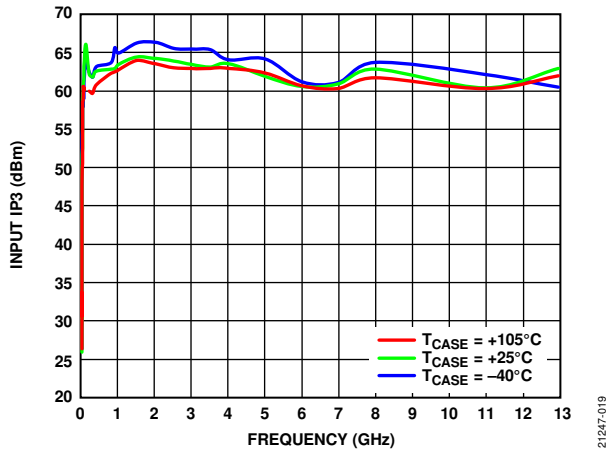
*Figure 19. Input IP3 vs. Frequency over Temperature, $V_{SS} = -2.5\,V$*
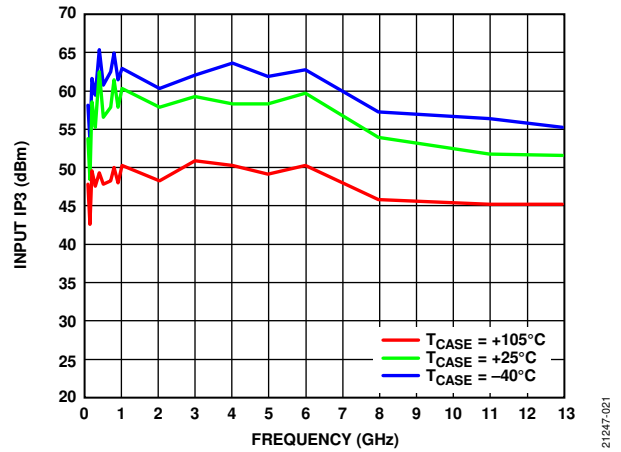


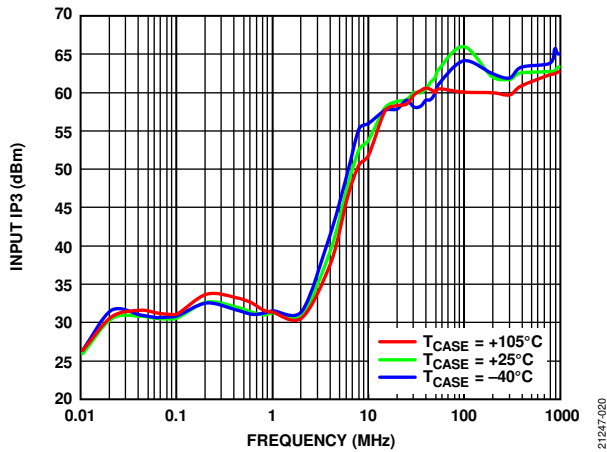*Figure 21. Input IP3 vs. Frequency over Temperature, $V_{SS} = 0\,V$*



*Figure 20. Input IP3 vs. Frequency over Temperature (Low Frequency Detail), $V_{SS} = -2.5\,V$*
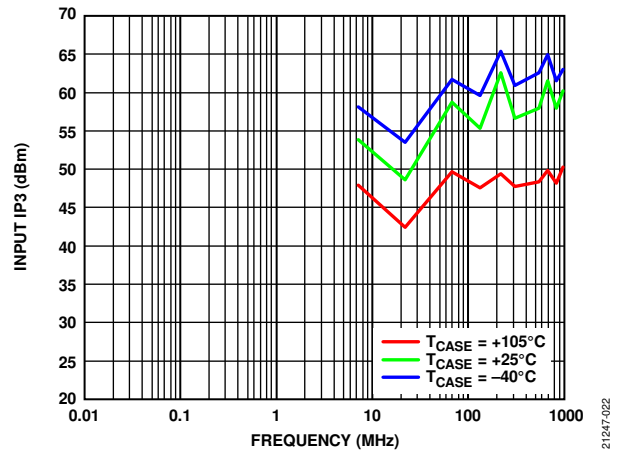


*Figure 22. Input IP3 vs. Frequency over Temperature (Low Frequency Detail), $V_{SS} = 0\,V$*

# THEORY OF OPERATION

The ADRF5019 integrates a driver to perform logic functions internally and to provide the user with the advantage of a simplified positive voltage control interface. The driver features two digital control input pins ($V_{CTRL}$ and LS) that control the state of the RF paths, determining which RF port is in the insertion loss state and which path is in the isolation state (see Table 5).

## RF INPUT AND OUTPUT

The RF ports (RFC, RF1, and RF2) are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The ADRF5019 is bidirectional with equal power handling capabilities. An RF input signal ($RF_{IN}$) can be applied to the RFC port or to the RF1 port or the RF2 port.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected RF throw port, which is nonreflective, by using an internal 50 Ω termination resistor.

## POWER SUPPLY

The ADRF5019 requires a positive supply voltage applied to the $V_{DD}$ pin and a negative supply voltage applied to the $V_{SS}$ pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The ideal power-up sequence is as follows:

1. Connect to GND.
2. Power up the $V_{DD}$ and $V_{SS}$ voltages. Power up $V_{SS}$ after $V_{DD}$ to avoid current transients on $V_{DD}$ during ramp up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the $V_{DD}$ voltage supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high impedance state after the $V_{DD}$ voltage is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal to RFC, RF1, or RF2.

The ideal power-down sequence is the reverse order of the power-up sequence.

### Single-Supply Operation

The ADRF5019 can operate with a single positive supply voltage applied to the $V_{DD}$ pin and $V_{SS}$ pin connected to ground. However, some performance degradations can occur in the input compression and input third-order intercept.

**Table 5. Control Voltage Truth Table**

| Digital Control Inputs | | RF Paths | |
|---|---|---|---|
| **LS** | **$V_{CTRL}$** | **RF1 to RFC** | **RF2 to RFC** |
| High | Low | Insertion loss (on) | Isolation (off) |
| High | High | Isolation (off) | Insertion loss (on) |
| Low | Low | Isolation (off) | Insertion loss (on) |
| Low | High | Insertion loss (on) | Isolation (off) |

# APPLICATIONS INFORMATION

## LAYOUT CONSIDERATIONS

All measurements in this data sheet are measured on the ADRF5019-EVALZ evaluation board. The design of the ADRF5019-EVALZ board serves as a layout recommendation for ADRF5019 application.

See the ADRF5019-EVALZ user guide for more information on using the evaluation board.

## BOARD LAYOUT

The ADRF5019-EVALZ is a 4-layer board. The outer copper (Cu) layers are 0.7 mil to 2.2 mil plated and are separated by dielectric materials. Figure 23 shows the ADRF5019-EVALZ board stack up.

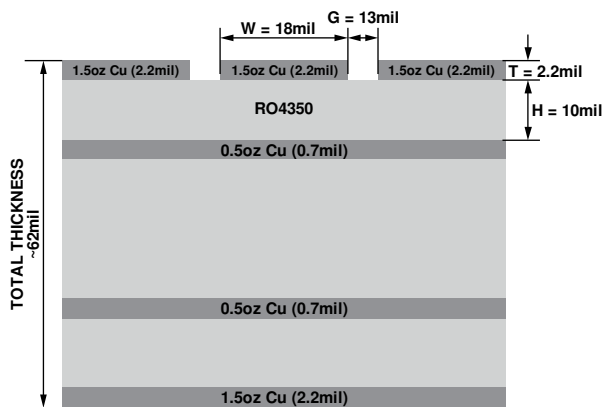The board layout and stackup shown in Figure 23 are used to make the measurements included in this data sheet.



Figure 23. *ADRF5019-EVALZ Stack Up*

All RF and dc traces are routed on the top copper layer. The inner and bottom layers are ground planes that provide a solid ground for the RF transmission lines. The top dielectric material (H) is 10 mil Rogers RO4350, which allows optimal RF performance. The middle and bottom dielectric layers provide mechanical strength. The overall evaluation board thickness is approximately 62 mil, which allows Subminiature Version A (SMA) connectors to be connected at the board edges.

## RF AND DIGITAL CONTROLS

The RF transmission lines use a coplanar waveguide (CPWG) model with a width of 18 mil and a ground spacing (G) of 13 mil and have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many plated through vias as possible are arranged around the transmission lines and under the exposed pad of the package.

The RF input and output ports (RFC, RF1, and RF2) are connected through 50 Ω transmission lines to the SMA launchers. On the $V_{DD}$ and $V_{SS}$ supply traces, a 100 pF bypass capacitor filters high frequency noise.

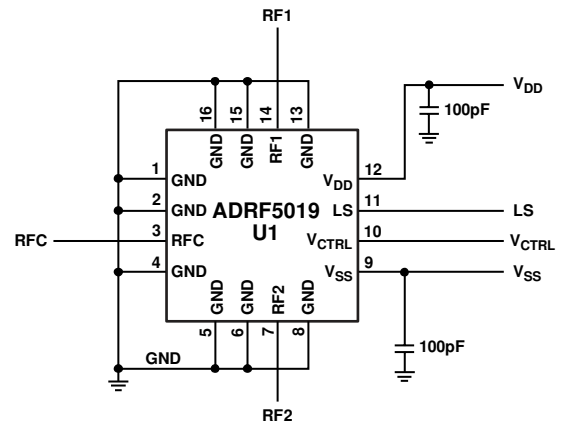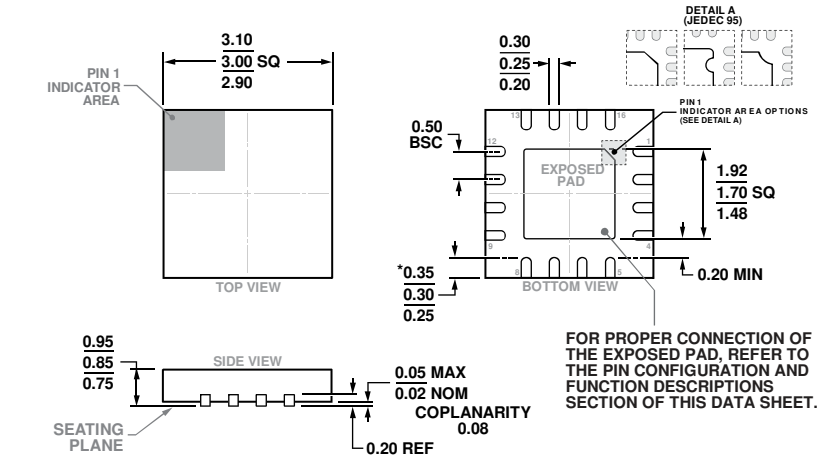Figure 24 shows the simplified application circuit for the ADRF5019.



Figure 24. *Simplified Application Circuit*

## OUTLINE DIMENSIONS



*COMPLIANT WITH JEDEC STANDARDS MO-220-VEED-4
WITH THE EXCEPTION OF PACKAGE EDGE TO LEAD EDGE.

*Figure 25. 16-Lead Lead Frame Chip Scale Package [LFCSP]*
*3 mm × 3 mm Body and 0.85 mm Package Height*
*(CP-16-38)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Marking Code |
|---|---|---|---|---|
| ADRF5019BCPZN | −40°C to +105°C | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-38 | S4Z |
| ADRF5019BCPZN-R7 | −40°C to +105°C | 16-Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-38 | S4Z |
| ADRF5019-EVALZ | | Evaluation Board | | |

[1] Z = RoHS Compliant Part.

www.analog.com