

# NB3Nxxxxx - VCXO Series

## 3.3V PureEdge™ VCXO Clock Generator with Differential LVPECL Outputs

### Description

The NB3NXXXXXX – series voltage–controlled crystal oscillator (VCXO) devices are designed to meet today’s requirements for 3.3 V LVPECL clock generation applications. These devices use an external high Q fundamental mode pullable crystal and Phase Locked Loop (PLL) multiplier to provide a wide range of frequencies from 60 MHz to 700 MHz (factory configurable per user specifications) with a pullable range of  $\pm 100$  ppm. The silicon–based PureEdge products provides users with exceptional frequency stability and reliability. They produce an ultra low jitter and phase noise LVPECL differential output. The NB3NXXXXXX – series are members of ON Semiconductor’s PureEdge clock family that provides accurate and precision clock generation solutions.

Available in the industry standard 4 mm x 4 mm QFN–20 package.

### Features

- LVPECL Differential Output
- Operating Range: 3.3 V  $\pm 10\%$
- Ultra Low Jitter and Phase Noise – 0.5 ps (12 kHz – 20 MHz)
- 245 ps Typical Rise and Fall Times
- Factory Configurable Frequencies from 60 MHz to 700 MHz (see Standard Frequencies in the Ordering Information Table in page 5)
- Pullable Range Minimum of  $\pm 100$  ppm
- Control Voltage with Positive Slope
- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  Ambient Operating Temperature
- These Devices are Pb–Free and are RoHS Compliant

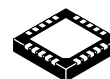
### Applications

- Networking
- SONET
- 10 Gigabit Ethernet
- Networking Base Stations
- Broadcasting



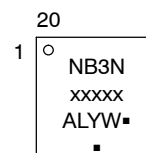
ON Semiconductor®

<http://onsemi.com>



QFN20  
MN SUFFIX  
CASE 485E

### MARKING DIAGRAM



XXXXX = Frequency XXX.XX  
A = Assembly Location  
L, WL = Wafer Lot  
Y = Year  
W, WW = Work Week  
G or ■ = Pb–Free Package

(\*Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

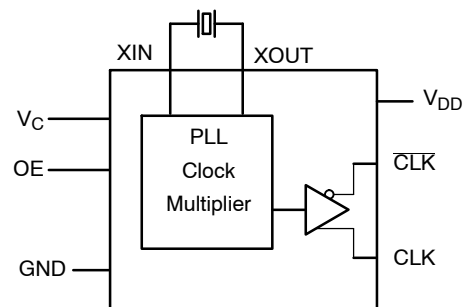


Figure 1. Simplified Block Diagram of NB3Nxxxxx

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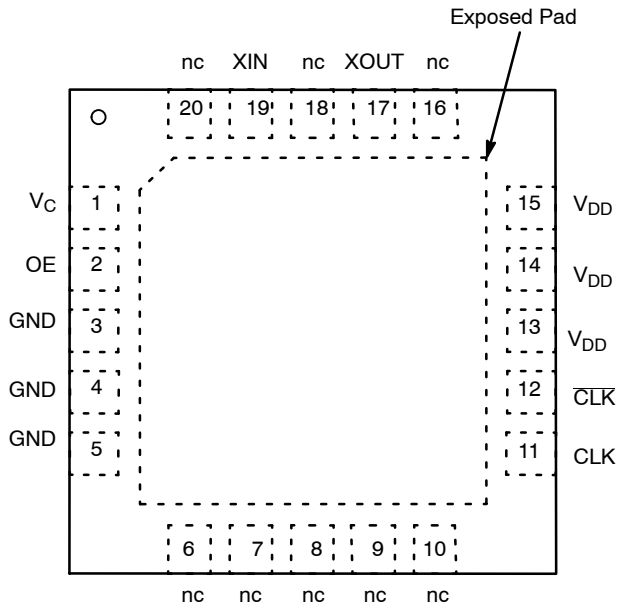


Figure 2. QFN-20 Pinout (Top View)

Table 1. OUTPUT ENABLE TRI-STATE FUNCTION

| OE   | Output Pins Function |
|------|----------------------|
| Open | Active               |
| High | Active               |
| Low  | High Z               |

Table 2. PIN DESCRIPTION

| Pin | Name    | I/O                    | Description   |
|-----|---------|------------------------|---|
| 1   | VC      | Analog Input           | Analog control voltage input pin that adjusts output oscillation frequency. $f_0 = V_C = 1.65 \text{ V}$ . Control voltage has a positive slope with a linearity of $\pm 10\%$ ; $V_C = 1.65 \text{ V} \pm 1 \text{ V}$ . |
| 2   | OE      | LVTTTL / LVC MOS Input | Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 1.  |
| 3   | GND     | Ground                 | Negative Supply Voltage   |
| 4   | GND     | Ground                 | Negative Supply Voltage   |
| 5   | GND     | Ground                 | Negative Supply Voltage   |
| 6   | nc      | No connect             |   |
| 7   | nc      | No connect             |   |
| 8   | nc      | No connect             |   |
| 9   | nc      | No connect             |   |
| 10  | nc      | No connect             |   |
| 11  | CLK     | LVPECL Output          | Non-inverted Differential Output. Typically Terminated with $50 \Omega$ Resistor to $V_{DD} - 2 \text{ V}$ .  |
| 12  | CLK-bar | LVPECL Output          | Inverted Differential Output. Typically Terminated with $50 \Omega$ Resistor to $V_{DD} - 2 \text{ V}$ .  |
| 13  | VDD     | Power Supply           | 3.3 V Positive Supply Voltage   |
| 14  | VDD     | Power Supply           | 3.3 V Positive Supply Voltage   |
| 15  | VDD     | Power Supply           | 3.3 V Positive Supply Voltage   |
| 16  | nc      | No connect             |   |
| 17  | XOUT    | Crystal                | Crystal Input. This pin forms an oscillator when connected to an external parallel-resonant crystal.  |
| 18  | nc      | No connect             |   |
| 19  | XIN     | Crystal                | Crystal Input. This pin forms an oscillator when connected to an external parallel-resonant crystal.  |

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**Table 2. PIN DESCRIPTION**

| Pin | Name | I/O        | Description   |
|-----|------|------------|---|
| 20  | nc   | No connect |   |
| –   | EP   |            | The Exposed Pad (EP) on the QFN-20 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board. |

1. All VDD and GND pins must be externally connected to a power supply for proper operation.

**Table 3. ATTRIBUTES**

| Characteristics   | Value                |
|---|----------------------|
| Internal Default State Resistor (OE)                          | 170 k $\Omega$       |
| ESD Protection Human Body Model                               | 2 kV                 |
| Machine Model   | 200 V                |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2) | Level 1              |
| Flammability Rating Oxygen Index: 28 to 34                    | UL 94 V-0 @ 0.125 in |
| Transistor Count  | 3510 Devices         |
| Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test    |                      |

2. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

| Symbol           | Parameter   | Condition 1        | Condition 1  | Rating      | Unit |
|------------------|---|--------------------|--|-------------|------|
| V <sub>DD</sub>  | Positive Power Supply                             | GND = 0 V          |  | 4.6         | V    |
| V <sub>IN</sub>  | Control Input (V <sub>C</sub> and OE)             |                    | V <sub>IN</sub> ≤ V <sub>DD</sub> + 200 mV<br>V <sub>IN</sub> ≥ GND – 200 mV |             | V    |
| I <sub>OUT</sub> | LVPECL Output Current                             | Continuous Surge   |  | 25<br>50    | mA   |
| T <sub>A</sub>   | Operating Temperature Range                       |                    |  | –40 to +85  | °C   |
| T <sub>stg</sub> | Storage Temperature Range                         |                    |  | –55 to +120 | °C   |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient)          | 0 lfpm<br>500 lfpm | QFN-20<br>QFN-20   | 47<br>33    | °C/W |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)<br>(Note 3) | Standard Board     | QFN-20   | 18          | °C/W |
| T <sub>sol</sub> | Wave Solder Pb-Free                               |                    |  | 265         | °C   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

**Table 5. RECOMMENDED CRYSTAL PARAMETERS**

|                                    |  |
|------------------------------------|--|
| Crystal Type                       | Fundamental AT-Cut                       |
| Frequency                          | Various – Device dependent; see AC Table |
| Load Capacitance                   | 16 pF                                    |
| Shunt Capacitance, C0              | 3.2 pF typical                           |
| Motional Capacitance (C1)          | 12 fF typical                            |
| Capacitance Ratio (C0/C1)          | 260 typical                              |
| ESR (Equivalent Series Resistance) | 25 $\Omega$ max; 5 $\Omega$ typical      |

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**Table 6. DC CHARACTERISTICS** ( $V_{DD} = 3.3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) (Note 4)

| Symbol | Characteristic           | Min             | Typ | Max             | Unit |
|--------|--------------------------|-----------------|-----|-----------------|------|
| IDD    | Power Supply Current     |                 | 90  | 110             | mA   |
| VIH    | Input HIGH Voltage, OE   | 2000            |     | $V_{DD}$        | mV   |
| VIL    | Input LOW Voltage, OE    | $GND - 200$     |     | 800             | mV   |
| IIH    | Input HIGH Current, OE   | -100            |     | +100            | uA   |
| IIL    | Input LOW Current, OE    | -100            |     | +100            | uA   |
| VOH    | Output HIGH Voltage      | $V_{DD} - 1195$ |     | $V_{DD} - 945$  | mV   |
| VOL    | Output LOW Voltage       | $V_{DD} - 1945$ |     | $V_{DD} - 1600$ | mV   |
| VOUTPP | Output Voltage Amplitude |                 | 700 |                 | mV   |

4. Measurement taken with outputs terminated with  $50\ \Omega$  to  $V_{DD} - 2.0\text{ V}$ . See Figure 3.

**Table 7. AC CHARACTERISTICS** ( $V_{DD} = 3.3 \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Symbol            | Characteristic                                    | Conditions                               | Min       | Typ | Max    | Unit |
|-------------------|---|--|-----------|-----|--------|------|
| $f_{CLKOUT}$      | Output Clock Frequency                            | Crystal $f_{ref} = 28.276363\text{ MHz}$ | NB3N15552 |     | 155.52 | MHz  |
|                   |   | Crystal $f_{ref} = 28.409090\text{ MHz}$ | NB3N15625 |     | 156.25 |      |
|                   |   | Crystal $f_{ref} = 30.703125\text{ MHz}$ | NB3N49152 |     | 491.52 |      |
|                   |   | Crystal $f_{ref} = 28.276363\text{ MHz}$ | NB3N62208 |     | 622.08 |      |
| $t_{jit(cp)}$     | RMS Phase Jitter                                  | 12 kHz to 20 MHz                         |           | 0.5 | 0.9    | ps   |
| $t_{jitter}$      | Cycle to Cycle, RMS                               | 1000 Cycles                              |           | 2   | 8      | ps   |
|                   | Cycle to Cycle, Peak-to-Peak                      | 1000 Cycles                              |           | 10  | 30     |      |
|                   | Period, RMS                                       | 10,000 Cycles                            |           | 1   | 4      |      |
|                   | Period, Peak-to-Peak                              | 10,000 Cycles                            |           | 6   | 20     |      |
| $t_{OE/OD}$       | Output Enable/Disable Time                        |  |           |     | 200    | ns   |
| $F_P$             | Crystal Pull ability (Note 5)                     | $0 \leq V_C \leq 3.3\text{ V}$           | $\pm 100$ |     |        | ppm  |
| $V_{C(bw)}$       | Control Voltage Bandwidth                         | -3 dB                                    | 20        |     |        | kHz  |
| $t_{DUTY\_CYCLE}$ | Output Clock Duty Cycle (Measured at Cross Point) |  | 45        | 50  | 55     | %    |
| $t_R$             | Output Rise Time (20% and 80%)                    |  |           | 245 | 400    | ps   |
| $t_F$             | Output Fall Time (80% and 20%)                    |  |           | 245 | 400    | ps   |
| $t_{start}$       | Start-up Time                                     |  |           | 1   | 5      | ms   |

5. Gain transfer is positive with a rate of 130 ppm/V.

**Table 8. PHASE NOISE PERFORMANCE**

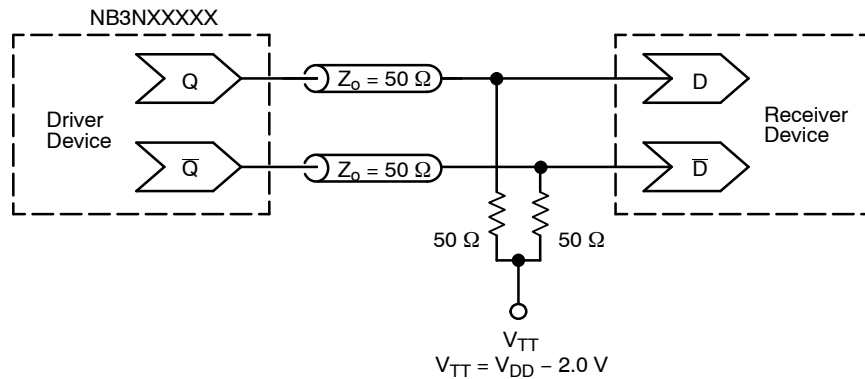
| Parameter        | Characteristic                 | Condition      | 155.52 MHz | 156.25 MHz | 491.52 MHz | 622.08 MHz | Unit   |
|------------------|--------------------------------|----------------|------------|------------|------------|------------|--------|
| $\theta_{NOISE}$ | Output Phase-Noise Performance | 100 Hz offset  | -82        | -82        | -72        | -70        | dBc/Hz |
|                  |                                | 1 kHz offset   | -106       | -106       | -96        | -94        | dBc/Hz |
|                  |                                | 10 kHz offset  | -126       | -126       | -116       | -114       | dBc/Hz |
|                  |                                | 100 kHz offset | -128       | -128       | -119       | -116       | dBc/Hz |
|                  |                                | 1 MHz offset   | -135       | -135       | -125       | -123       | dBc/Hz |
|                  |                                | 10 MHz offset  | -159       | -159       | -151       | -149       | dBc/Hz |

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## ORDERING INFORMATION

| Device         | Frequency (MHz) | Package             | Shipping†          |
|----------------|-----------------|---------------------|--------------------|
| NB3N15552MNG   | 155.52          | QFN-20<br>(Pb-Free) | 92 Units / Rail    |
| NB3N15552MNTXG | 155.52          | QFN-20<br>(Pb-Free) | 3000 / Tape & Reel |
| NB3N15625MNG   | 156.25          | QFN-20<br>(Pb-Free) | 92 Units / Rail    |
| NB3N15625MNTXG | 156.25          | QFN-20<br>(Pb-Free) | 3000 / Tape & Reel |
| NB3N49152MNG   | 491.52          | QFN-20<br>(Pb-Free) | 92 Units / Rail    |
| NB3N49152MNTXG | 491.52          | QFN-20<br>(Pb-Free) | 3000 / Tape & Reel |
| NB3N62208MNG   | 622.08          | QFN-20<br>(Pb-Free) | 92 Units / Rail    |
| NB3N62208MNTXG | 622.08          | QFN-20<br>(Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

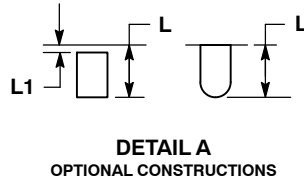
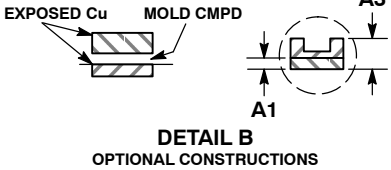
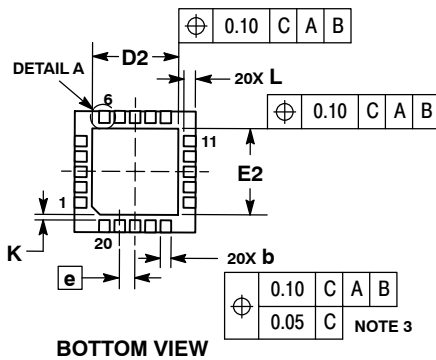
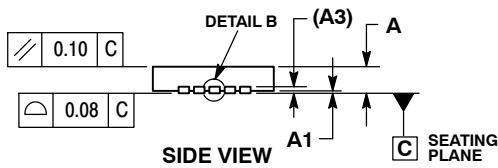
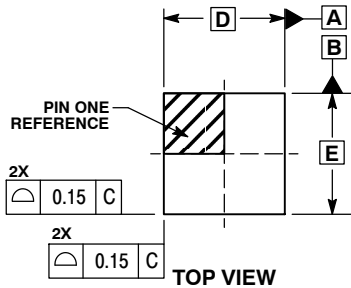


**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

# NB3Nxxxxx – VCXO Series

## PACKAGE DIMENSIONS

QFN20, 4x4, 0.5P  
CASE 485E-01  
ISSUE B

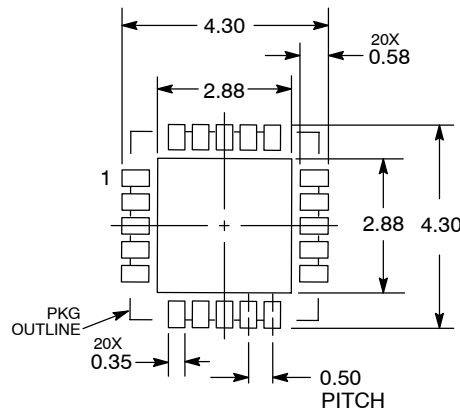


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS |      |      |
|-------------|------|------|
| DIM         | MIN  | MAX  |
| A           | 0.80 | 1.00 |
| A1          | ---  | 0.05 |
| A3          | 0.20 | REF  |
| b           | 0.20 | 0.30 |
| D           | 4.00 | BSC  |
| D2          | 2.60 | 2.90 |
| E           | 4.00 | BSC  |
| E2          | 2.60 | 2.90 |
| e           | 0.50 | BSC  |
| K           | 0.20 | REF  |
| L           | 0.35 | 0.45 |
| L1          | 0.00 | 0.15 |

**SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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