

74LVC16373A-Q100; 74LVCH16373A-Q100

16-bit D-type transparent latch with 5 V tolerant
inputs/outputs; 3-state

Rev. 5 — 1 August 2023

Product data sheet

1. General description

The 74LVC16373A-Q100 and 74LVCH16373A-Q100 are 16-bit D-type transparent latches with 3-state outputs. The devices can be used as two 8-bit transparent latches or a single 16-bit transparent latch. The devices feature two latch enables (1LE and 2LE) and two output enables (1OE and 2OE), each controlling 8-bits. When nLE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When nLE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of nLE. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. Operation of the nOE input does not affect the state of the latches. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

Bus hold on the data inputs eliminates the need for external pull-up resistors to hold unused inputs.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

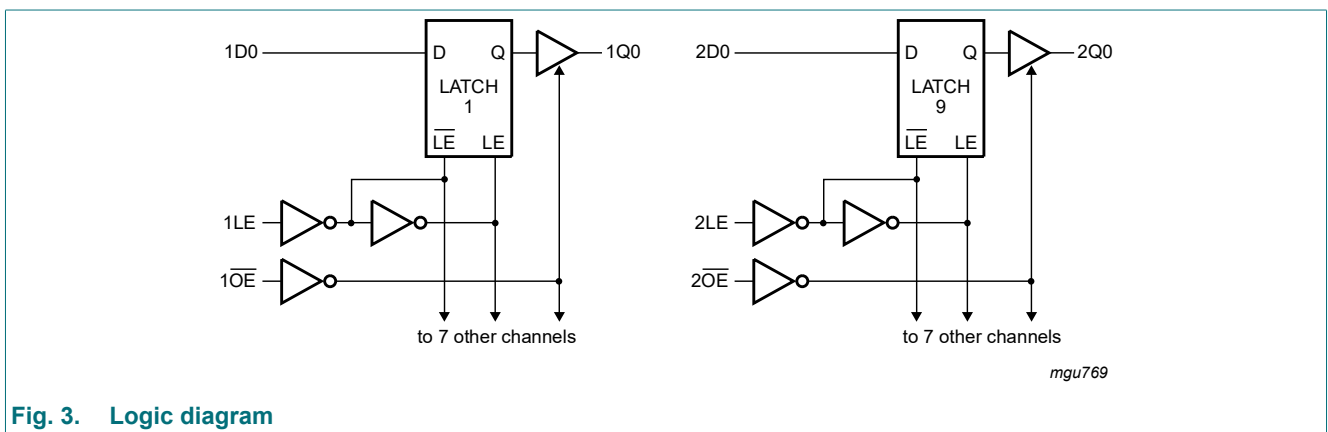
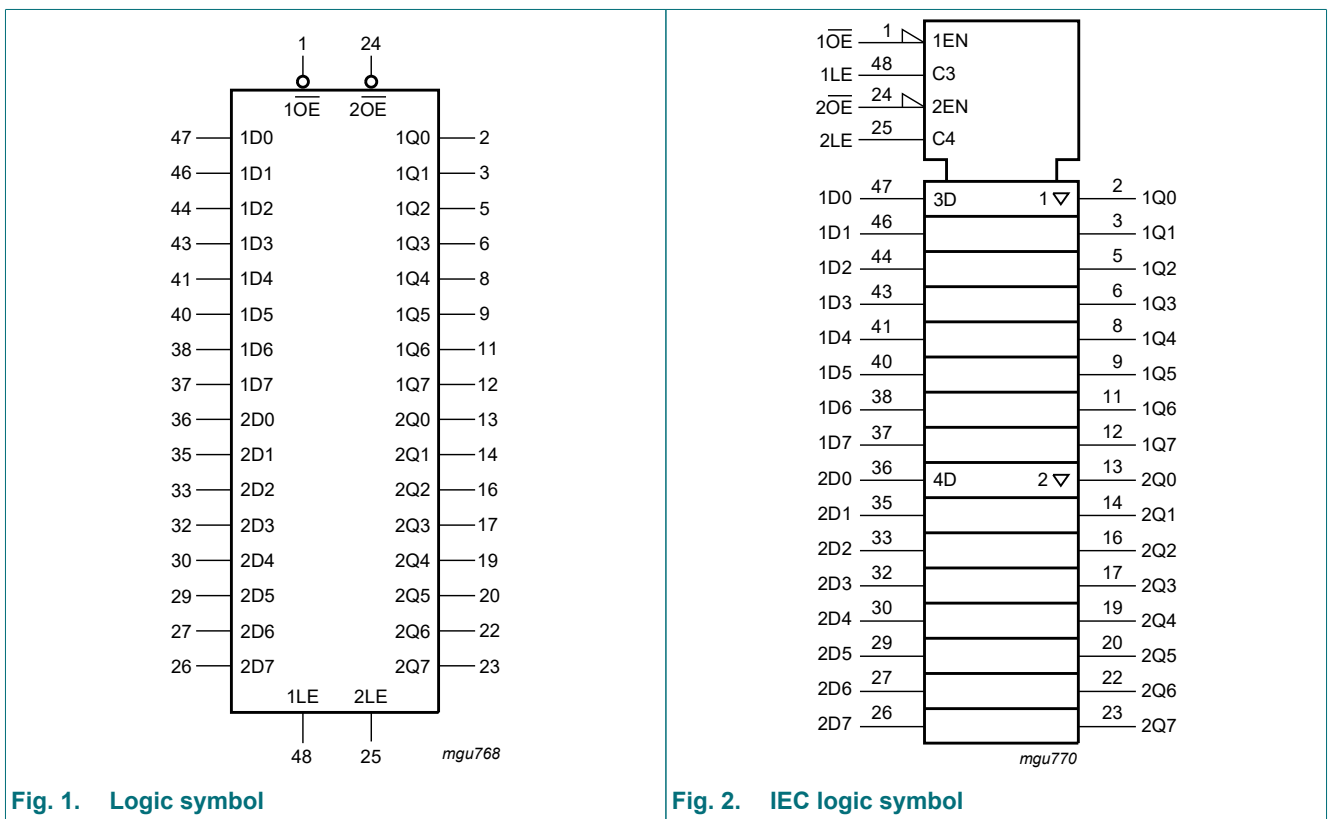
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power dissipation
- MULTIBYTE flow-through standard pinout architecture
- Multiple low inductance supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16373A-Q100 only)
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standards:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC16373ADGG-Q100	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVCH16373ADGG-Q100				
74LVC16373ADGV-Q100	-40 °C to +125 °C	TVSOP48	plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm	SOT480-1
74LVCH16373ADGV-Q100				

4. Functional diagram



16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

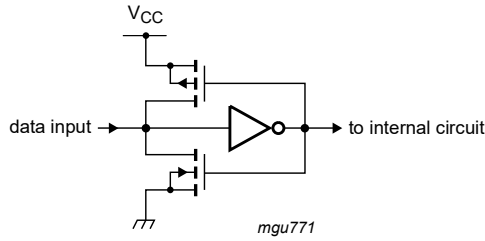


Fig. 4. Bus hold circuit

5. Pinning information

5.1. Pinning

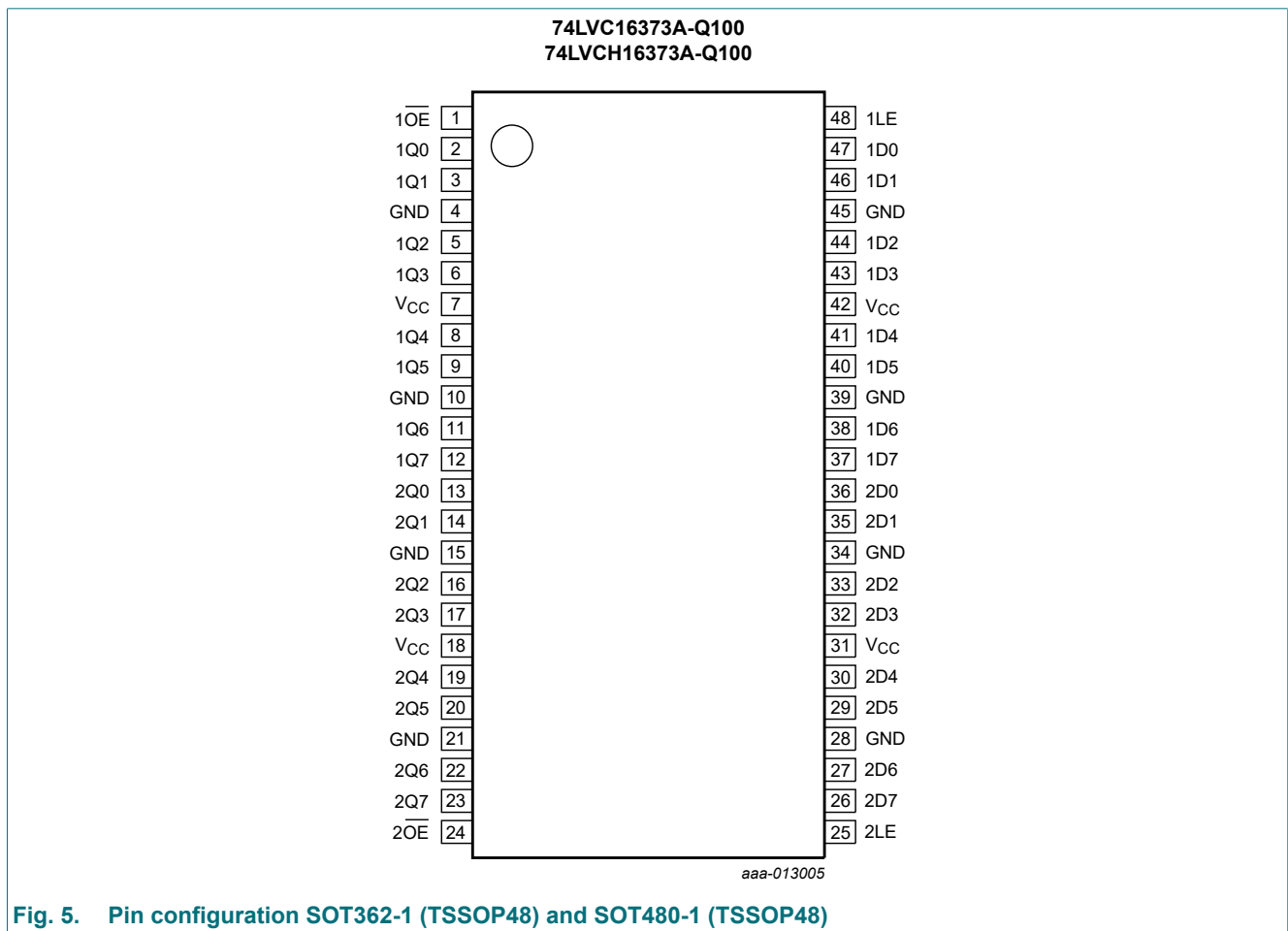


Fig. 5. Pin configuration SOT362-1 (TSSOP48) and SOT480-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 24	output enable input (active LOW)
1LE, 2LE	48, 25	latch enable input (active HIGH)
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC}	7, 18, 31, 42	supply voltage
1Q0 to 1Q7	2, 3, 5, 6, 8, 9, 11, 12	data output
2Q0 to 2Q7	13, 14, 16, 17, 19, 20, 22, 23	data output
1D0 to 1D7	47, 46, 44, 43, 41, 40, 38, 37	data input
2D0 to 2D7	36, 35, 33, 32, 30, 29, 27, 26	data input

6. Functional description

Table 3. Function table

Per section of eight bits.

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH to LOW LE transition

L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH to LOW LE transition

Z = high-impedance OFF-state

Operating modes	Input			Internal latch	Output nQ0 to nQ7
	nOE	nLE	nDn		
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
V_O	output voltage	output HIGH or LOW state	[2] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[2] -0.5	+6.5	V
I_O	output current	$V_O = 0\text{ V to }V_{CC}$	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT362-1 (TSSOP48) packages: P_{tot} derates linearly with 12.2 mW/K above 109 °C.

For SOT480-1 (TVSOP48) packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.2\text{ V to }2.7\text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	-	10	ns/V

16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ [1]	Max	Min	Max		
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V	
		V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V	
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V	
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V	
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V	
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V	
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V	
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}							
		I _O = -100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V	
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V	
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V	
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V	
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}							
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V	
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V	
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V	
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V	
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	[2]	-	±0.1	±5	-	±20	µA
		V _{CC} = 3.6 V; V _O = 5.5 V or GND	[2]	-	±0.1	±5	-	±20	µA
		V _{CC} = 0 V; V _I or V _O = 5.5 V		-	±0.1	±10	-	±20	µA
		V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A		-	0.1	20	-	80	µA
		per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A		-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF	

16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
I _{BHL}	bus hold LOW current	V _{CC} = 1.65; V _I = 0.58 V [3][4]	10	-	-	10	-	µA
		V _{CC} = 2.3; V _I = 0.7 V	30	-	-	25	-	µA
		V _{CC} = 3.0; V _I = 0.8 V	75	-	-	60	-	µA
I _{BHH}	bus hold HIGH current	V _{CC} = 1.65; V _I = 1.07 V [3][4]	-10	-	-	-10	-	µA
		V _{CC} = 2.3; V _I = 1.7 V	-30	-	-	-25	-	µA
		V _{CC} = 3.0; V _I = 2.0 V	-75	-	-	-60	-	µA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 1.95 V [3][5]	200	-	-	200	-	µA
		V _{CC} = 2.7 V	300	-	-	300	-	µA
		V _{CC} = 3.6 V	500	-	-	500	-	µA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 1.95 V [3][5]	-200	-	-	-200	-	µA
		V _{CC} = 2.7 V	-300	-	-	-300	-	µA
		V _{CC} = 3.6 V	-500	-	-	-500	-	µA

- [1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.
- [2] The bus hold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input pin.
- [3] Valid for data inputs (74LVCH16373A-Q100) only; control inputs do not have a bus hold circuit.
- [4] The specified sustaining current at the data inputs holds the input below the specified V_I level.
- [5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	Dn to Qn; see Fig. 6 [2]						
		V _{CC} = 1.2 V	-	12	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	5.4	11.4	1.5	13.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.9	5.7	1.0	6.6	ns
		V _{CC} = 2.7 V	1.5	2.9	4.9	1.5	6.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.4	4.4	1.0	5.5	ns
		LE to Qn; see Fig. 7						
		V _{CC} = 1.2 V	-	14	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	6.4	12.4	2.0	14.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	3.4	6.1	1.5	7.1	ns
		V _{CC} = 2.7 V	1.5	3.0	5.3	1.5	7.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	2.9	4.8	1.5	6.0	ns
t _{en}	enable time	OE to Qn; see Fig. 8 [2]						
		V _{CC} = 1.2 V	-	18	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	5.5	12.4	1.5	14.3	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.1	6.6	1.0	7.6	ns
		V _{CC} = 2.7 V	1.5	3.3	5.7	1.5	7.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.5	4.9	1.0	6.5	ns

16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{dis}	disable time	OE to Qn; see Fig. 8 [2]						
		V _{CC} = 1.2 V	-	11	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.8	4.5	9.1	2.8	10.5	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.5	5.1	1.0	6.0	ns
		V _{CC} = 2.7 V	1.5	3.3	6.3	1.5	8.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.1	5.4	1.5	7.0	ns
t _w	pulse width	LE HIGH; see Fig. 7						
		V _{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V _{CC} = 2.7 V	3.0	-	-	3.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	3.0	2.0	-	3.0	-	ns
t _{su}	set-up time	Dn to LE; see Fig. 9						
		V _{CC} = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns
		V _{CC} = 2.7 V	2.0	-	-	2.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	1.0	-	2.0	-	ns
t _h	hold time	Dn to LE; see Fig. 9						
		V _{CC} = 1.65 V to 1.95 V	2.5	-	-	2.5	-	ns
		V _{CC} = 2.3 V to 2.7 V	2.0	-	-	2.0	-	ns
		V _{CC} = 2.7 V	0.9	-	-	0.9	-	ns
		V _{CC} = 3.0 V to 3.6 V	+0.9	-1.0	-	+0.9	-	ns
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V [3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	per input; V _I = GND to V _{CC} [4]						
		V _{CC} = 1.65 V to 1.95 V	-	10.8	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	13.0	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	15.0	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

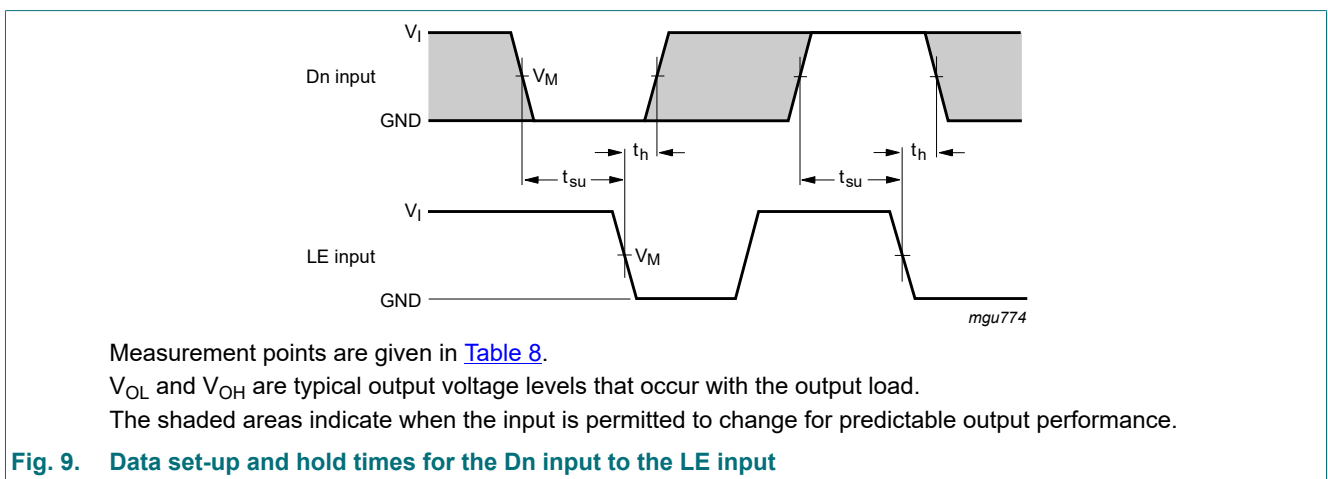
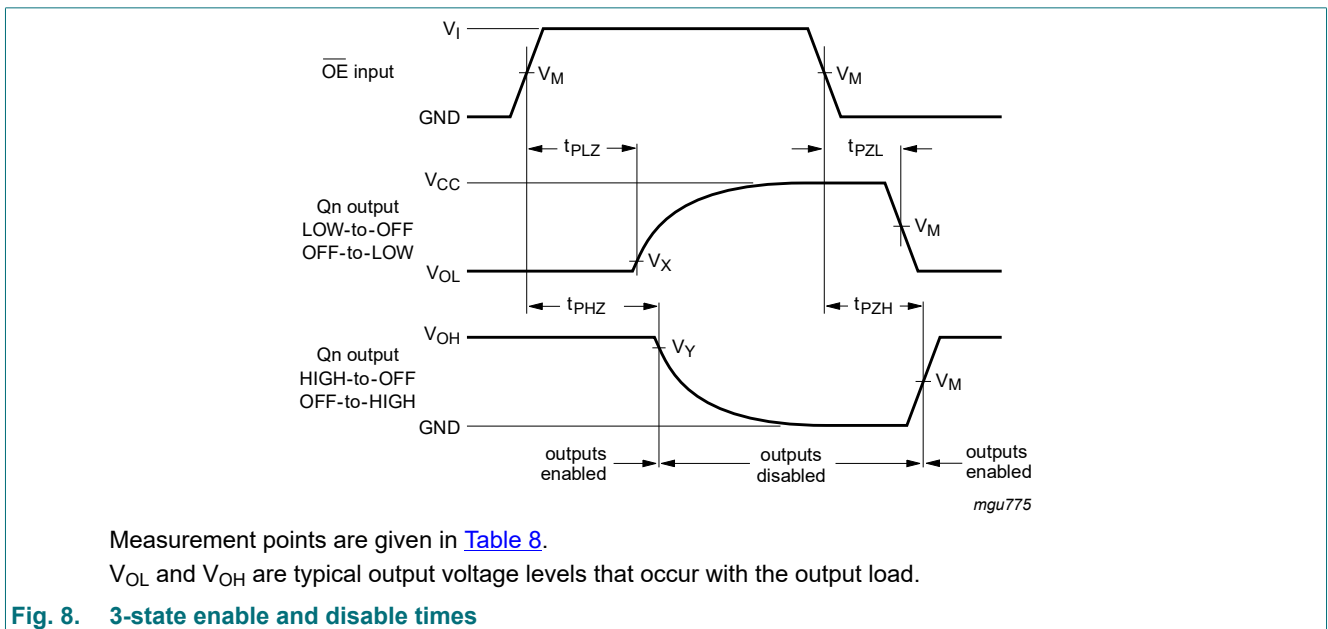
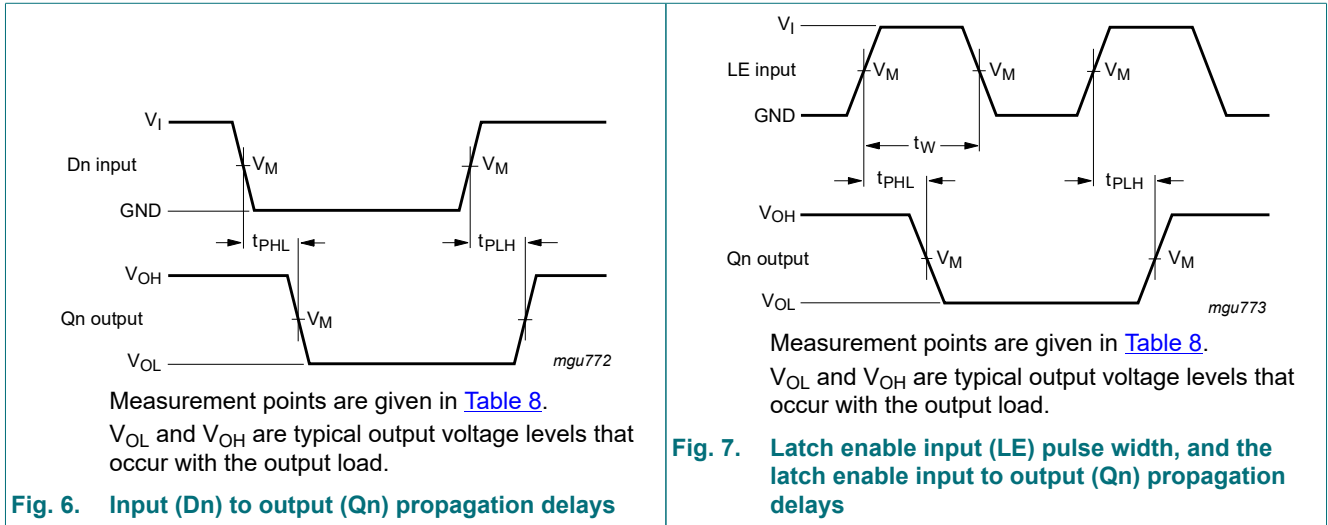
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

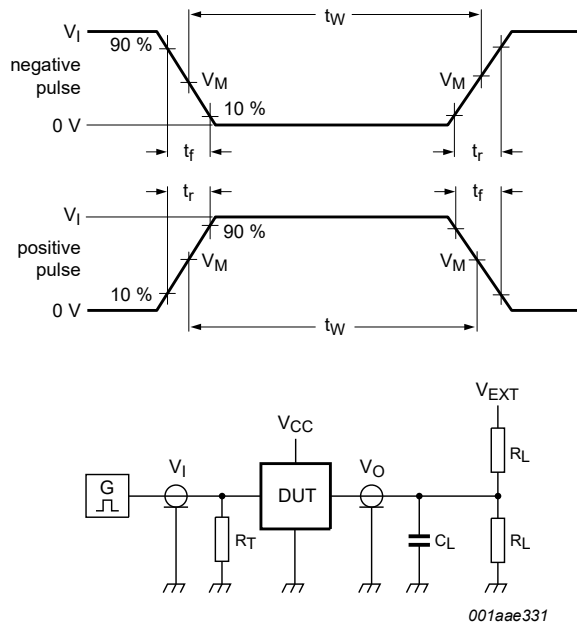
10.1. Waveforms and test circuit



16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

Table 8. Measurement points

Supply voltage	Input		Output		
V _{CC}	V _I	V _M	V _M	V _X	V _Y
1.2 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
1.65 V to 1.95 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
2.3 V to 2.7 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
V _{CC}	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V _{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

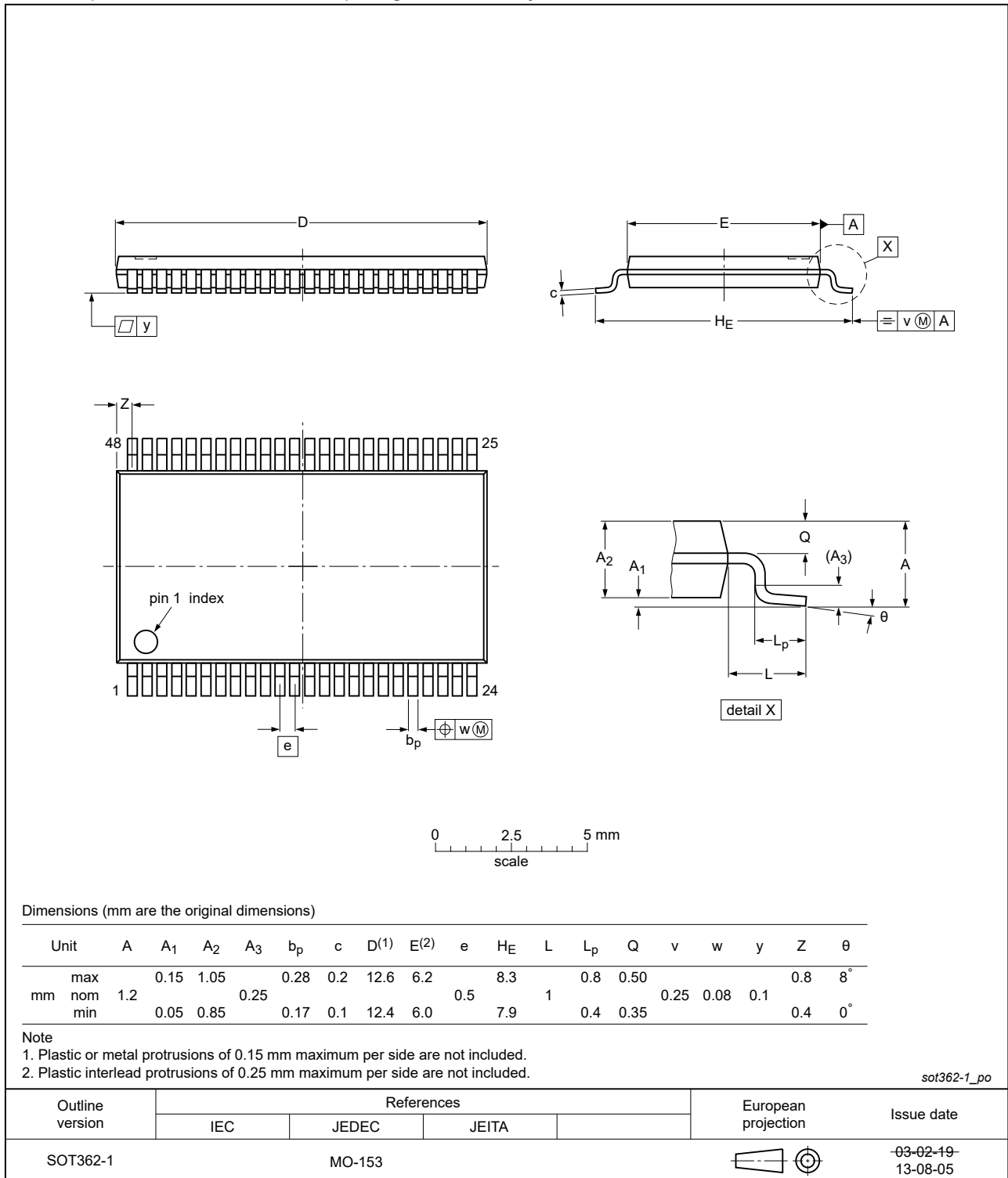


Fig. 11. Package outline SOT362-1 (TSSOP48)

16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

TVSOP48: plastic thin shrink small outline package; 48 leads;
body width 4.4 mm; lead pitch 0.4 mm

SOT480-1

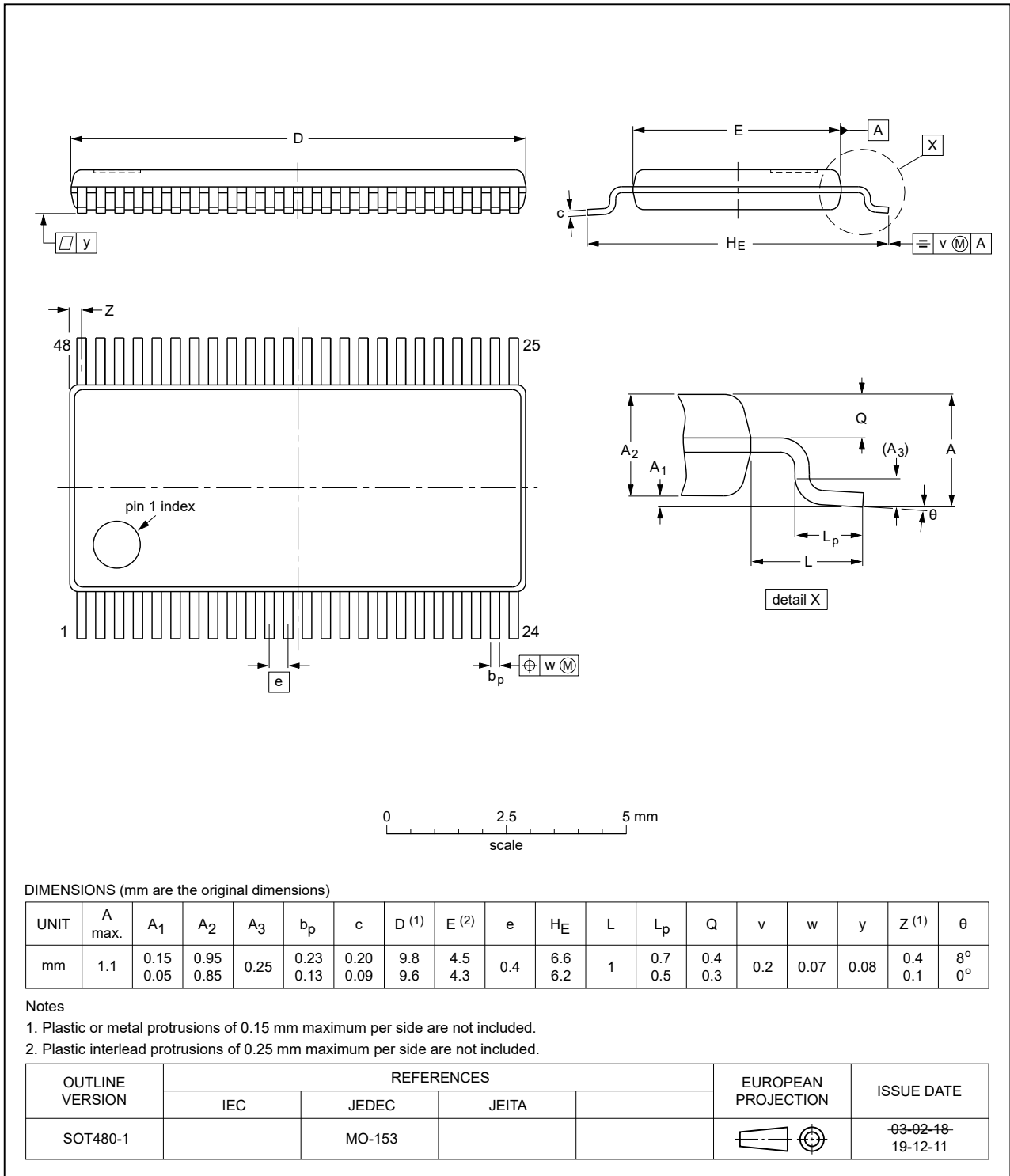


Fig. 12. Package outline SOT480-1 (TVSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16373A_Q100 v.5	20230801	Product data sheet	-	74LVC_LVCH16373A_Q100 v.4
Modifications:	<ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74LVC_LVCH16373A_Q100 v.4	20211001	Product data sheet	-	74LVC_LVCH16373A_Q100 v.3
Modifications:	<ul style="list-style-type: none"> • Section 1 and Section 2 updated. • Package outline drawing SOT480-1 updated. 			
74LVC_LVCH16373A_Q100 v.3	20190215	Product data sheet	-	74LVC_LVCH16373A_Q100 v.2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74LVC16373ADGV-Q100 and 74LVCH16373ADGV-Q100 added. 			
74LVC_LVCH16373A_Q100 v.2	20140710	Product data sheet	-	74LVC_LVCH16373A_Q100 v.1
Modifications:	<ul style="list-style-type: none"> • 74LVC16373ADL-Q100 and 74LVCH16373ADL-Q100 removed. 			
74LVC_LVCH16373A_Q100 v.1	20140624	Product data sheet	-	-

16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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