winbond

32Mb HyperRAM

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1. FEATURES

- Interface: HyperBus
- Power supply: 1.7V~1.95V
- Maximum clock rate: 166MHz
- Double-Data Rate (DDR) Up to 333 MT/s
- Differential clock (CK/CK#)
- Chip Select (CS#)
- 8-bit data bus (DQ[7:0])
- Hardware reset (RESET#)
- Read-Write Data Strobe (RWDS)
  - – Bidirectional Data Strobe / Mask
  - – Output at the start of all transactions to indicate refresh latency
  - – Output during read transactions as Read Data Strobe
  - – Input during write transactions as Write Data Mask

Performance and Power

- Configurable output drive strength
- Power Saving Modes
  - – Hybrid Sleep Mode
  - – Deep Power Down
- Configurable Burst Characteristics
  - – Wrapped burst lengths:
    - – 16 bytes (8 clocks)
    - – 32 bytes (16 clocks)
    - – 64 bytes (32 clocks)
    - – 128 bytes (64 clocks)
- Array Refresh Modes
  - – Full Array Refresh
  - – Partial Array Refresh
- Support package:
  24 balls TFBGA
- Operating temperature range:
  -40°C ≤ T_{CASE} ≤ 85°C

2. ORDER INFORMATION

Part Number	VCC/VCCQ	I/O Width	Package	Interface	Others
W955D8MBYA6I	1.8V	8	24 balls TFBGA	HyperBus	166MHz, -40°C~85°C

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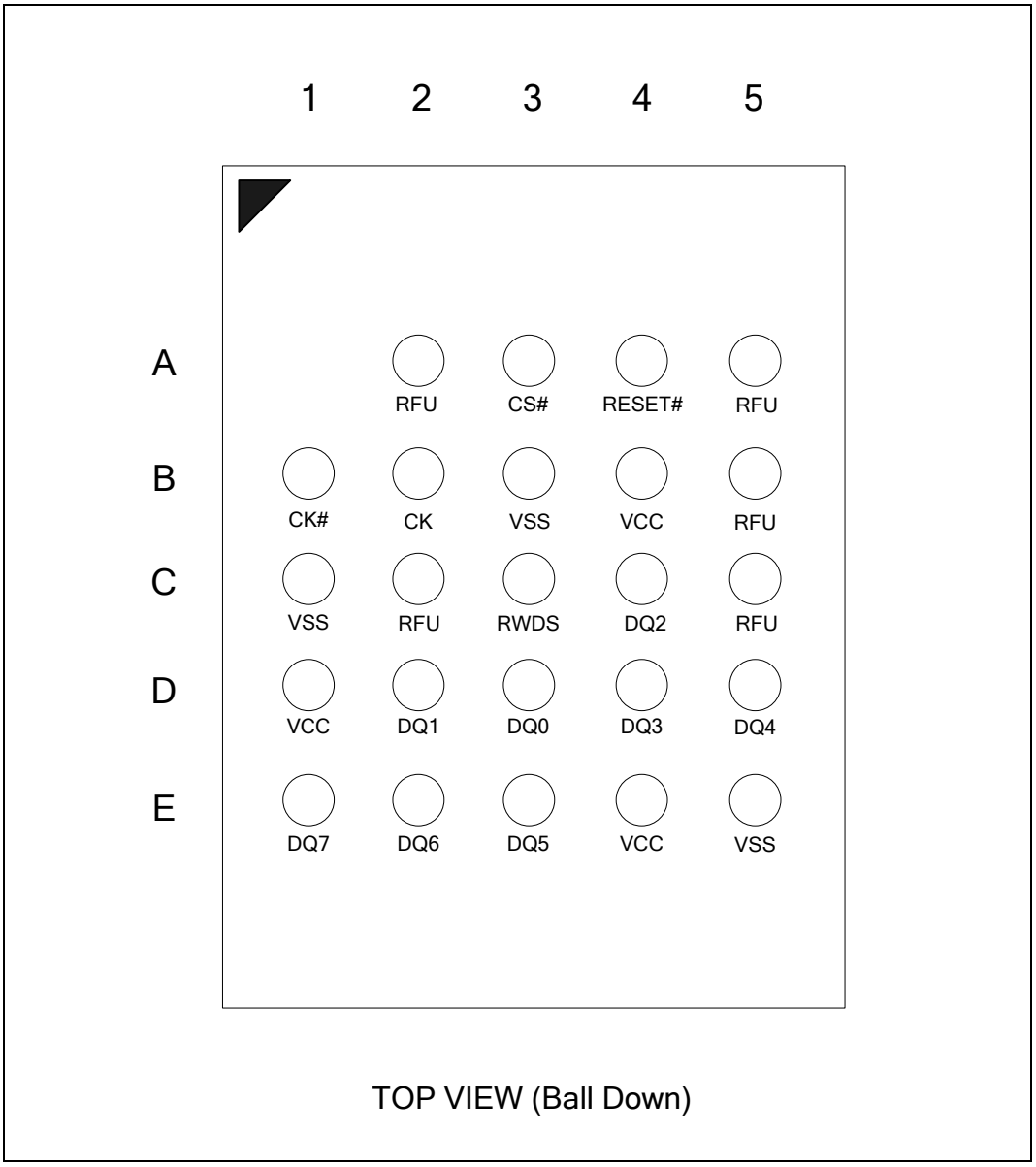
3. BALL ASSIGNMENT

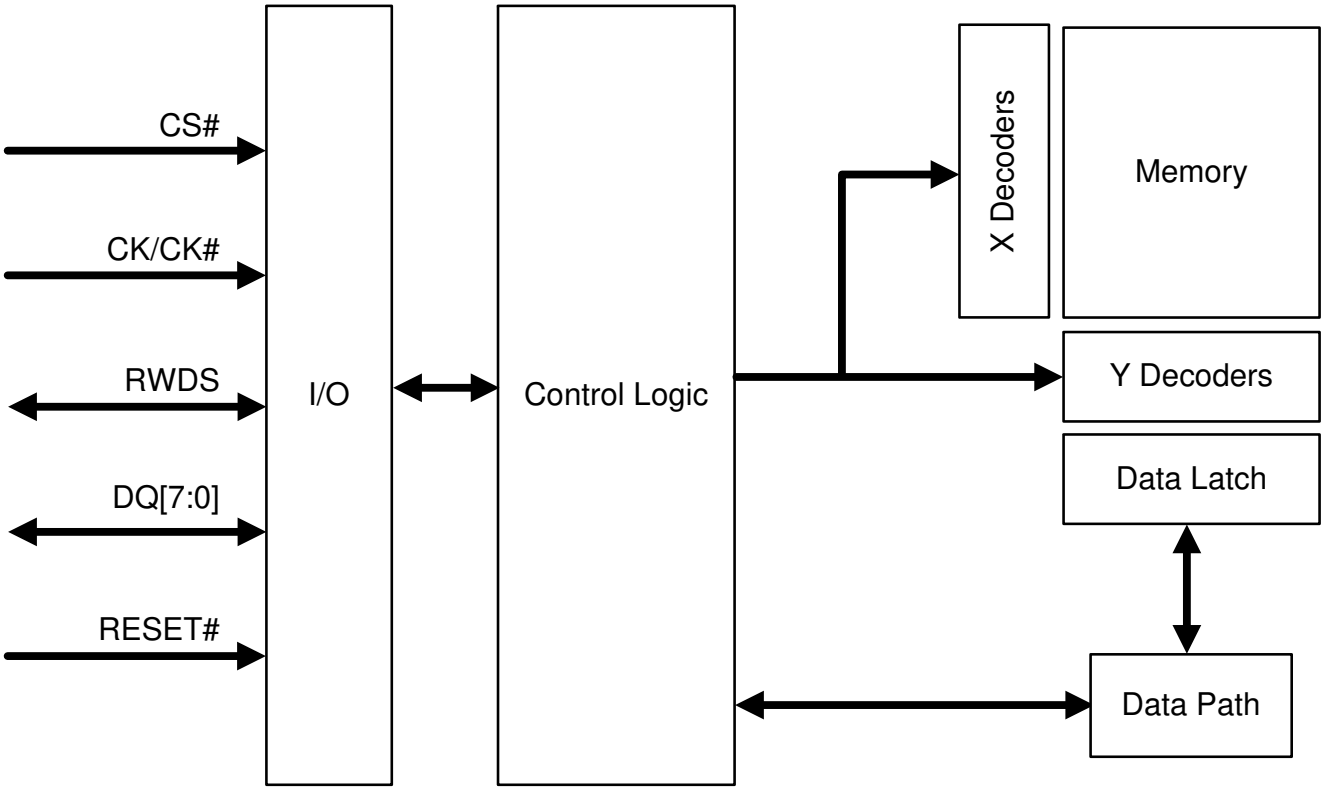


24 Balls TFBGA, 5x5-1 Ball Footprint, Top View

4. BALL DESCRIPTIONS

Signal Name	Type	Description
CS#	Input	**Chip Select:** Bus transactions are initiated with a High to Low transition. Bus transactions are terminated with a Low to High transition. The master device has a separate CS# for each slave.
CK, CK#	Input	**Differential Clock:** Command, address, and data information is output with respect to the crossing of the CK and CK# signals.
DQ[7:0]	Input / Output	**Data Input / Output:** Command, Address, and Data information is transferred on these signals during Read and Write transactions.
RWDS	Input / Output	**Read Write Data Strobe:** During the Command/Address portion of all bus transactions RWDS is a slave output and indicates whether additional initial latency is required. Slave output during read data transfer, data is edge aligned with RWDS. Slave input during data transfer in write transactions to function as a data mask. (High = additional latency, Low = no additional latency).
RESET#	Input, Internal Pull-up	**Hardware Reset:** When Low the slave device will self-initialize and return to the Standby state. RWDS and DQ[7:0] are placed into the High-Z state when RESET# is Low. The slave RESET# input includes a weak pull-up, if RESET# is left unconnected it will be pulled up to the High state. **Note:** The RESET# pad is maximum 4V tolerant.
VCC	Power Supply	**Power Supply**
VSS	Power Supply	**Ground**
RFU	No Connect	**Reserved for Future Use**: May or may not be connected internally, the signal/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The signal/ball may be used by a signal in the future.

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

6.1 HyperBus Interface

HyperBus is a low signal count, Double Data Rate (DDR) interface, that achieves high speed read and write throughput. The DDR protocol transfers two data bytes per clock cycle on the DQ input/output signals. A read or write transaction on HyperBus consists of a series of 16-bit wide, one clock cycle data transfers at the internal HyperRAM array with two corresponding 8-bit wide, one-half-clock-cycle data transfers on the DQ signals. All inputs and outputs are LV-CMOS compatible.

Command, address, and data information is transferred over the eight HyperBus DQ[7:0] signals. The clock (CK#, CK) is used for information capture by a HyperBus slave device when receiving command, address, or data on the DQ signals. Command or Address values are center aligned with clock transitions.

Every transaction begins with the assertion of CS# and Command-Address (CA) signals, followed by the start of clock transitions to transfer six CA bytes, followed by initial access latency and either read or write data transfers, until CS# is de-asserted.

Read and write transactions require two clock cycles to define the target row address and burst type, then an initial access latency of t_{ACC}. During the CA part of a transaction, the memory will indicate whether an additional latency for a required refresh time (t_{RFH}) is added to the initial latency; by driving the RWDS signal to the High state. During the CA period the third clock cycle will specify the target word address within the target row. During a read (or write) transaction, after the initial data value has been output (or input), additional data can be read from (or written to) the row on subsequent clock cycles in either a wrapped burst for memory data Read/Write or register Read/Write.

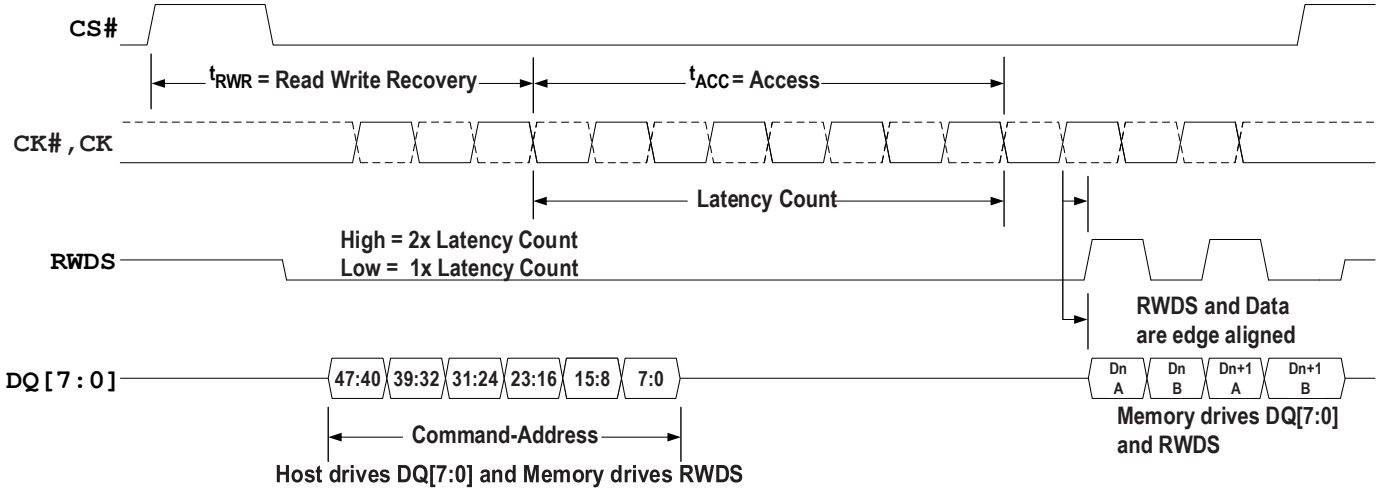


Figure 1 - Read Transaction, Single Initial Latency Count

The Read/Write Data Strobe (RWDS) is a bidirectional signal that indicates:

- When data will start to transfer from a HyperRAM device to the master device in read transactions (initial read latency)
- When data is being transferred from a HyperRAM device to the master device during read transactions (as a source synchronous read data strobe)
- When data may start to transfer from the master device to a HyperRAM device in write transactions (initial write latency)
- Data masking during write data transfers

During the CA transfer portion of a read or write transaction, RWDS acts as an output from a HyperRAM device to indicate whether additional initial access latency is needed in the transaction.

During read data transfers, RWDS is a read data strobe with data values edge aligned with the transitions of RWDS.

For register read, only the first two bytes of read data is valid.

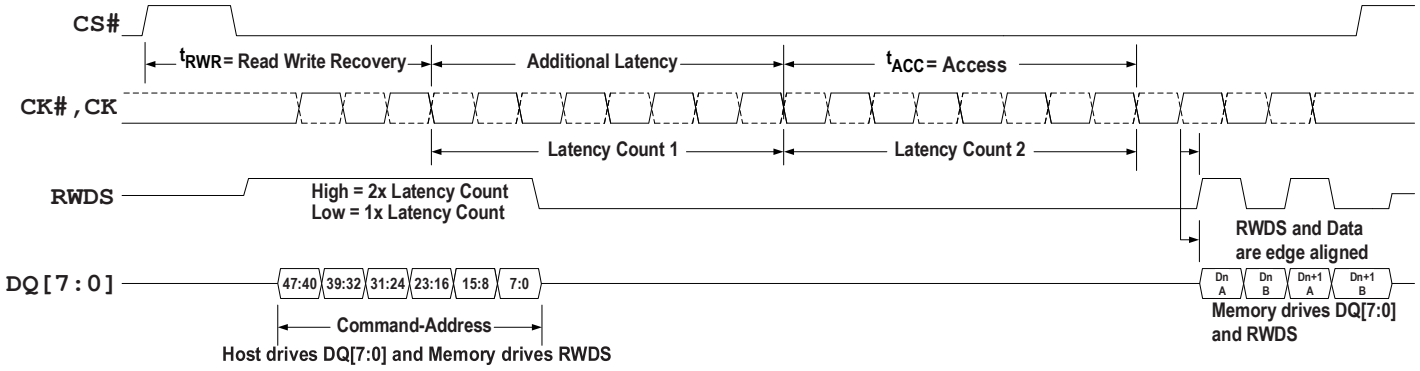


Figure 2 - Read Transaction, Additional Latency Count

During write data transfers, RWDS indicates whether each data byte transfer is masked with RWDS High (invalid and prevented from changing the byte location in a memory) or not masked with RWDS Low (valid and written to a memory). Data masking may be used by the host to byte align write data within a memory or to enable merging of multiple non-word aligned writes in a single burst write. During write transactions, data is center aligned with clock transitions.

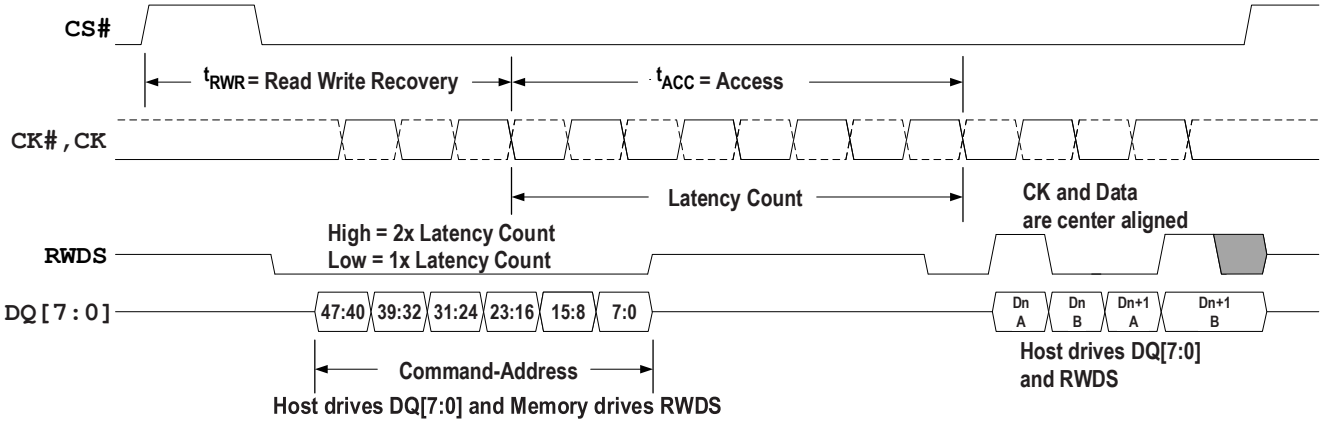


Figure3 - Write Transaction, Single Initial Latency Count

Note: The last write data can be masked or not masked.

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Read and write transactions are burst oriented, transferring the next sequential word during each clock cycle. Each individual read or write transaction can use a wrapped burst sequence.

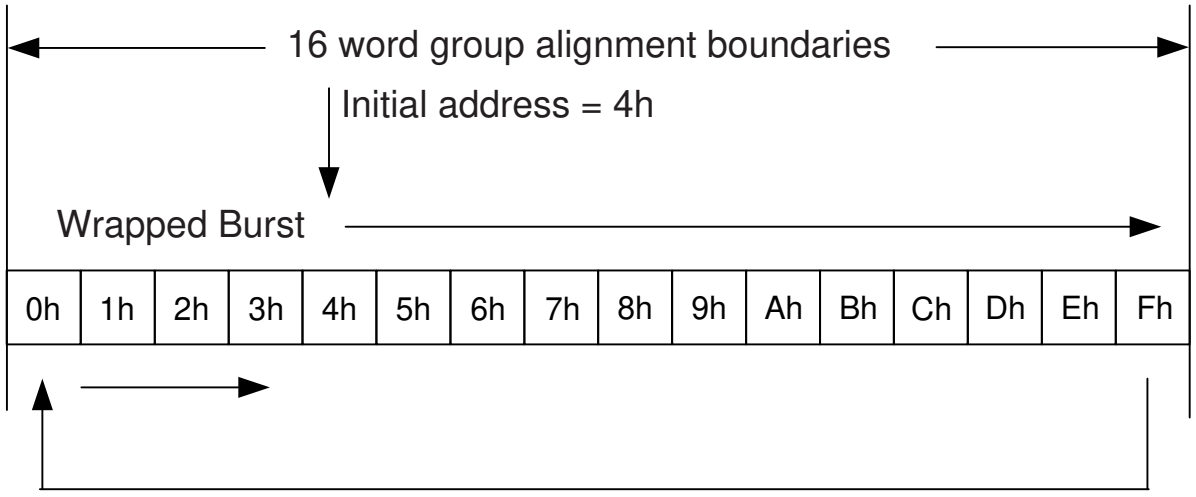

Figure 4 - Wrapped Burst Sequence (case of 16 words)

During wrapped transactions, accesses start at a selected location and continue to the end of a configured word group aligned boundary, then wrap to the beginning location in the group, then continue back to the starting location. Wrapped bursts are generally used for critical word first cache line fill read transactions.

7. HYPERBUS TRANSACTION DETAILS

7.1 Command/Address Bit Assignments

All HyperRAM bus transactions can be classified as either read or write. A bus transaction is started with CS# going Low with clock in idle state (CK=Low and CK#=High). The first three clock cycles transfer three words of Command/Address (CA0, CA1, CA2) information to define the transaction characteristics. The Command/Address words are presented with DDR timing, using the first six clock edges. The following characteristics are defined by the Command/Address information:

- Read or Write transaction
- Address Space: memory array space or register space
  - Register space is used to access Device Identification (ID) registers and Configuration Registers (CR) that identify the device characteristics and determine the slave specific behavior of read and write transfers on the HyperBus interface.
- Burst sequence type
- The target row (and half-page) address (upper order address)
- The target column (word within half-page) address (lower order address)

Once the transaction has been defined, a number of idle clock cycles are used to satisfy initial read or write access latency requirements before data is transferred. During the Command-Address portion of all transactions, RWDS is used by the memory to indicate whether additional initial access latency will be inserted for a required refresh of the memory array.

When data transfer begins, read data is edge aligned with RWDS transitions or write data is center aligned with clock transitions. During read data transfer, RWDS serves as a source synchronous data timing strobe.

During write data transfer, clock transitions provide the data timing reference and RWDS is used as a data mask. When RWDS is Low during a write data transfer, the data byte is written into memory; if RWDS is High during the transfer the byte is not written.

Data is transferred as 16-bit values with the first eight bits transferred on a High going CK (write data or CA bits) or RWDS edge (read data) and the second eight bits being transferred on the Low going CK or RWDS edge. Data transfers during read or write operations can be ended at any time by bringing CS# High when CK= Low and CK# = High.

The clock may stop in the idle state while CS# is High. The clock may also stop in the idle state for short periods while CS# is Low, as long as this does not cause a transaction to exceed the CS# maximum time low (t_{CSM}) limit.

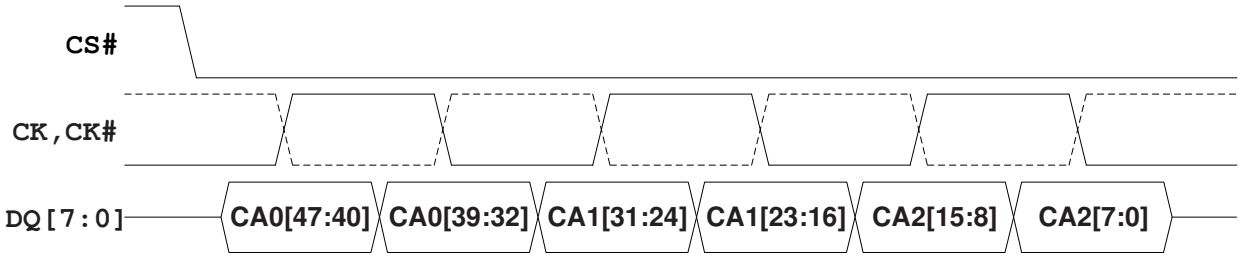

Figure 5 - Command-Address (CA) Sequence

Notes:

1. Figure shows the initial three clock cycles of all transactions on the HyperBus.
2. CK# of differential clock is shown as dashed line waveform.
3. CA information is “center aligned” with the clock during both Read and Write transactions.
4. Data bits in each byte are always in high to low order with bit 7 on DQ7 and bit 0 on DQ0.

Table 1 - CA Bit Assignment to DQ Signals

Signal	CA0[47:40]	CA0[39:32]	CA1[31:24]	CA1[23:16]	CA2[15:8]	CA2[7:0]
DQ[7]	CA[47]	CA[39]	CA[31]	CA[23]	CA[15]	CA[7]
DQ[6]	CA[46]	CA[38]	CA[30]	CA[22]	CA[14]	CA[6]
DQ[5]	CA[45]	CA[37]	CA[29]	CA[21]	CA[13]	CA[5]
DQ[4]	CA[44]	CA[36]	CA[28]	CA[20]	CA[12]	CA[4]
DQ[3]	CA[43]	CA[35]	CA[27]	CA[19]	CA[11]	CA[3]
DQ[2]	CA[42]	CA[34]	CA[26]	CA[18]	CA[10]	CA[2]
DQ[1]	CA[41]	CA[33]	CA[25]	CA[17]	CA[9]	CA[1]
DQ[0]	CA[40]	CA[32]	CA[24]	CA[16]	CA[8]	CA[0]

Table 2 - Command/Address Bit Assignments

CA Bit#	Bit Name	Bit Function
47	R/W#	Identifies the transaction as a read or write. R/W#=1 indicates a Read transaction R/W#=0 indicates a Write transaction
46	Address Space (AS)	Indicates whether the read or write transaction accesses the memory or register space. AS=0 indicates memory space AS=1 indicates the register space The register space is used to access device ID and Configuration registers.
45	Burst Type	Burst Type=0 Wrap burst for Memory data Read/Write Burst Type=1 Register Read/Write
44-34	Reserved	Reserved
33-22	Row Address	Row component of the target address: System word address bits A20-A9
21-16	Upper Column Address	Upper Column component of the target address: System word address bits A8-A3
15-3	Reserved	Reserved
2-0	Lower Column Address	Lower Column component of the target address: System word address bits A2-A0 selecting the starting word within a half-page.

Notes:

1. A Page is a 16-word (32-byte) length and aligned unit of device internal read or write access and additional latency may be inserted by RWDS when refresh is undergoing.
2. The Column address selects the burst transaction starting word location within a Row. The Column address is split into an upper and lower portion. The upper portion selects an 8-word (16-byte) Half-page and the lower portion selects the word within a Half-page where a read or write transaction burst starts.
3. The initial read access time starts when the Row and Upper Column (Half-page) address bits are captured by HyperBus interface.

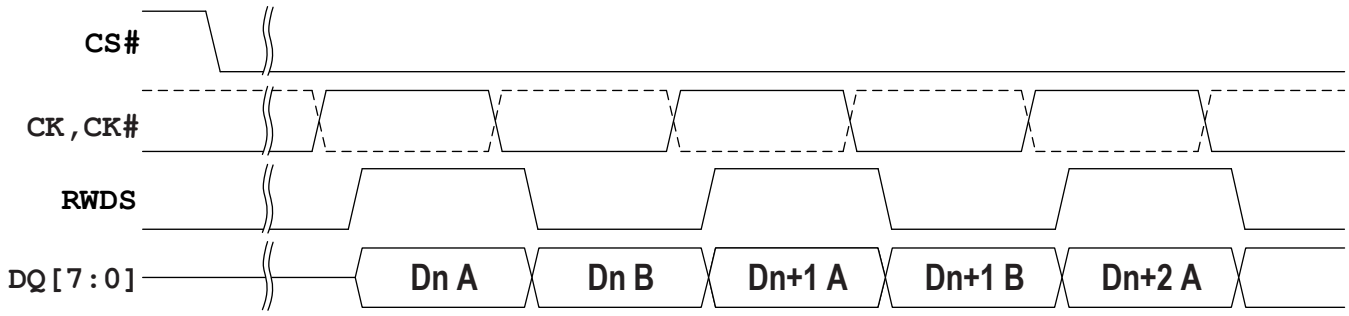

Figure 6 - Data Placement during a Read Transaction

Notes:

1. Figure shows a portion of a Read transaction on the HyperBus. CK# of differential clock is shown as dashed line waveform.
2. Data is “edge aligned” with the RWDS serving as a read data strobe during read transactions.
3. Data is always transferred in full word increments (word granularity transfers).
4. Word address increments in each clock cycle. Byte A is between RWDS rising and falling edges and is followed by byte B between RWDS falling and rising edges, of each word.
5. Data bits in each byte are always in high to low order with bit 7 on DQ7 and bit 0 on DQ0.

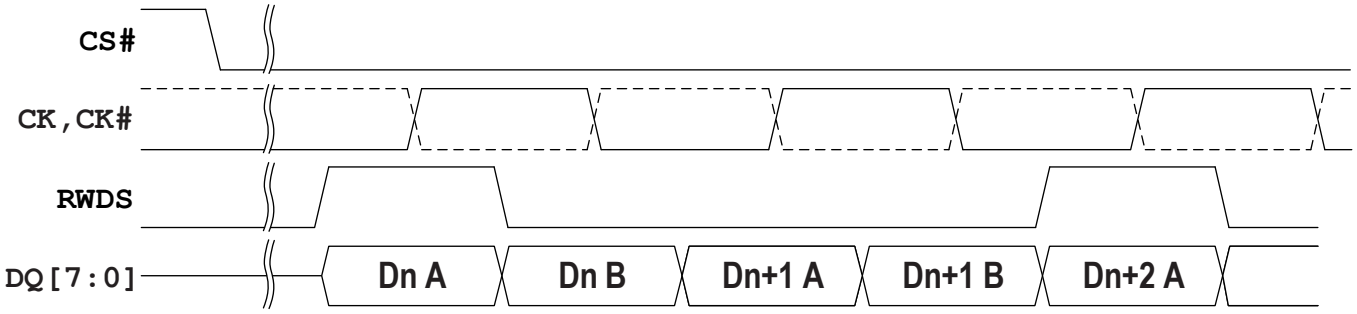

Figure 7 - Data Placement during a Write Transaction

Notes:

1. Figure shows a portion of a Write transaction on the HyperBus.
2. Data is “center aligned” with the clock during a Write transaction.
3. RWDS functions as a data mask during write data transfers with initial latency. Masking of the first and last byte is shown to illustrate an unaligned 3 byte write of data.
4. RWDS is not driven by the master during write data transfers with zero initial latency. Full data words are always written in this case. RWDS may be driven Low or left High-Z by the slave in this case.

7.2 Read Transactions

The HyperBus master begins a transaction by driving CS# Low while clock is idle. The clock then begins toggling while CA words are transferred.

In CA0, CA[47] = 1 indicates that a Read transaction is to be performed. CA[46] = 0 indicates the memory space is being read or CA[46] = 1 indicates the register space is being read. CA[45] indicates the burst type (wrap burst for memory data Read or register Read). Read transactions can begin the internal array access as soon as the row and upper column address has been presented in CA0 and CA1 (CA[47:16]). CA2 (CA(15:0]) identifies the target Word address within the chosen row.

The HyperBus master then continues clocking for a number of cycles defined by the latency count setting in Configuration Register 0. The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is Low during the CA cycles, one latency count is inserted. If RWDS is High during the CA cycles, an additional latency count is inserted. Once these latency clocks have been completed the memory starts to simultaneously transition the Read-Write Data Strobe (RWDS) and output the target data.

New data is output edge aligned with every transition of RWDS. Data will continue to be output as long as the host continues to transition the clock while CS# is Low. However, the HyperRAM device may stop RWDS transitions with RWDS Low, between the deliveries of words, in order to insert latency between words when crossing memory array boundaries.

The clock is not required to be free-running. The clock may remain idle while CS# is High.

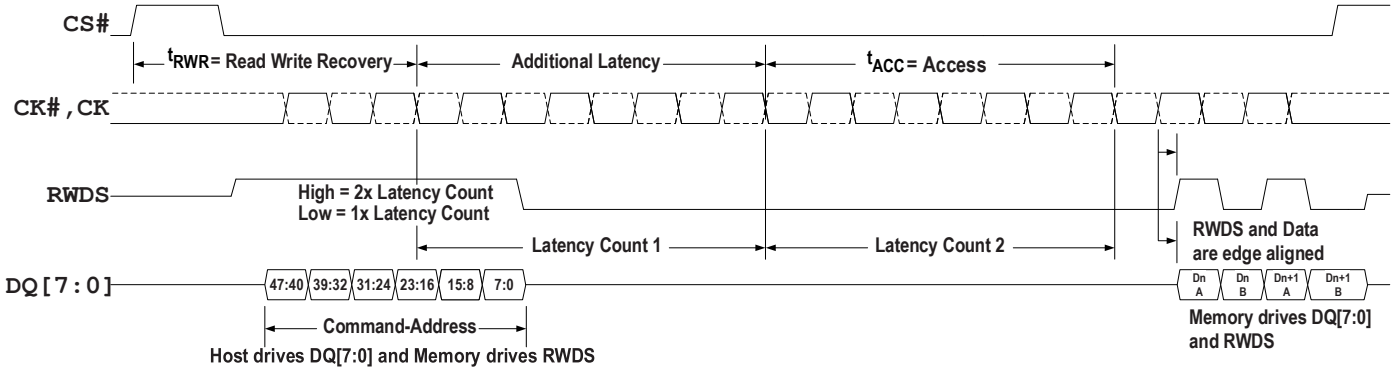

Figure 8 - Read Transaction with Additional Initial Latency

Notes:

1. Transactions are initiated with CS# falling while CK=Low and CK#=High.
2. CS# must return High before a new transaction is initiated.
3. CK# is the complement of the CK signal.CK# of a differential clock is shown as a dashed line waveform.
4. Read access array starts once CA[23:16] is captured.
5. The read latency is defined by the initial latency value in a configuration register.
6. In this read transaction example the initial latency count was set to four clocks.
7. In this read transaction a RWDS High indication during CA delays output of target data by an additional four clocks.
8. The memory device drives RWDS during read transactions.

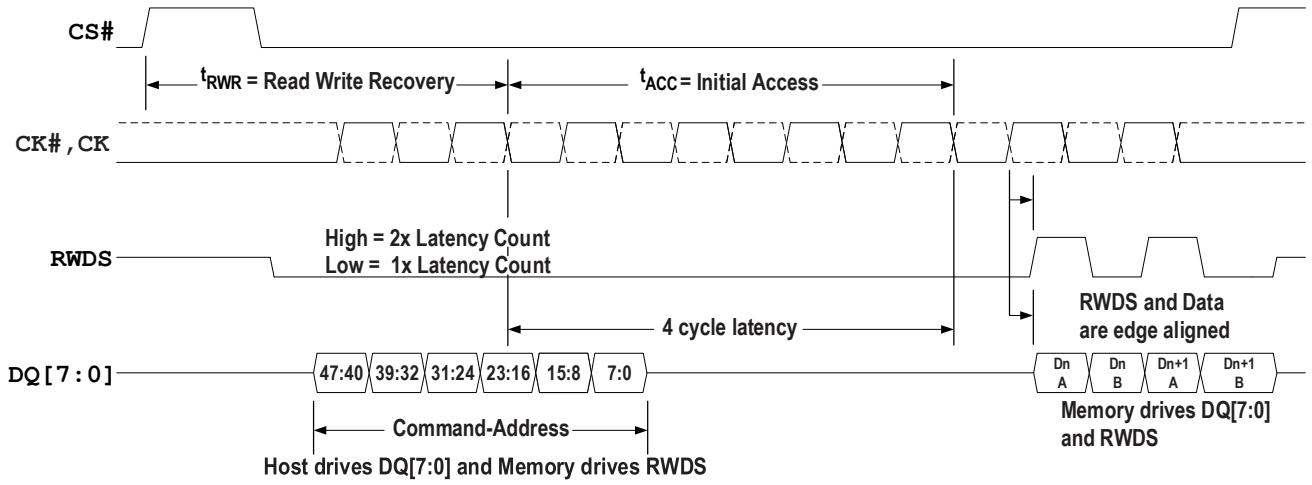

Figure 9 - Read Transaction without Additional Initial Latency

Note:

1. RWDS is Low during the CA cycles. In this Read Transaction there is a single initial latency count for read data access because, this read transaction does not begin at a time when additional latency is required by the slave.

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7.3 Write Transactions (Memory Array Write)

The HyperBus master begins a transaction by driving CS# Low while clock is idle. Then the clock begins toggling while CA words are transferred.

In CA0, CA[47] = 0 indicates that a Write transaction is to be performed. CA[46] = 0 indicates the memory space is being written. CA[45] indicates wrap burst for memory data Write. Write transactions can begin the internal array access as soon as the row and upper column address has been presented in CA0 and CA1 (CA[47:16]). CA2 (CA(15:0]) identifies the target word address within the chosen row.

The HyperBus master then continues clocking for a number of cycles defined by the latency count setting in configuration register 0. The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is Low during the CA cycles, one latency count is inserted. If RWDS is High during the CA cycles, an additional latency count is inserted.

Once these latency clocks have been completed the HyperBus master starts to output the target data. Write data is center aligned with the clock edges. The first byte of data in each word is captured by the memory on the rising edge of CK and the second byte is captured on the falling edge of CK.

During the CA clock cycles, RWDS is driven by the memory.

During the write data transfers, RWDS is driven by the host master interface as a data mask. When data is being written and RWDS is High the byte will be masked and the array will not be altered. When data is being written and RWDS is Low the data will be placed into the array. Because the master is driving RWDS during write data transfers, neither the master nor the HyperRAM device is able to indicate a need for latency within the data transfer portion of a write transaction. The acceptable write data burst length setting is also shown in configuration register 0.

Data will continue to be transferred as long as the HyperBus master continues to transition the clock while CS# is Low. Legacy format wrapped bursts will continue to wrap within the burst length. Write transfers can be ended at any time by bringing CS# High when the clock is idle.

The clock is not required to be free-running. The clock may remain idle while CS# is High.

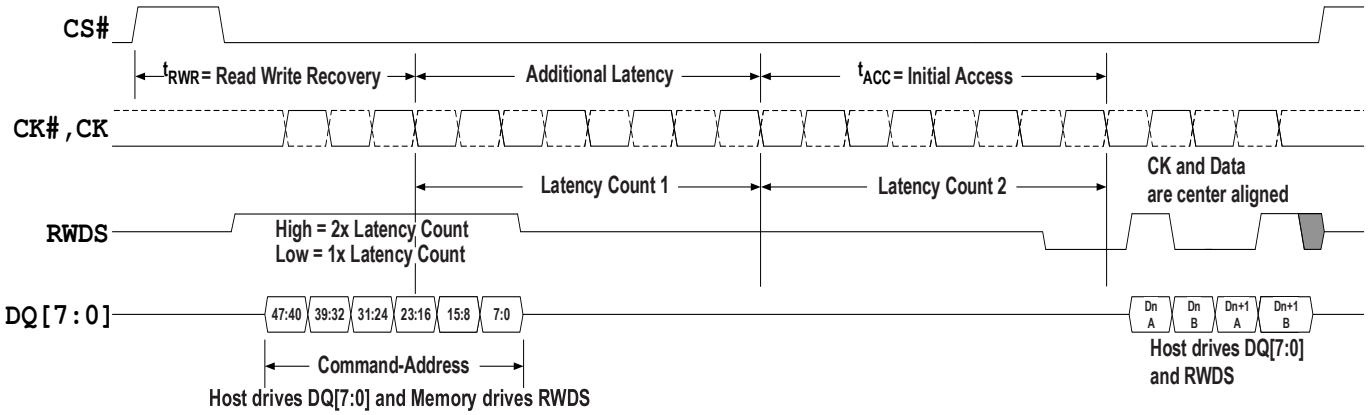

Figure 10 - Write Transaction with Additional Initial Latency

Notes:

1. Transactions must be initiated with CK=Low and CK#=High.
2. CS# must return High before a new transaction is initiated.
3. During CA, RWDS is driven by the memory and indicates whether additional latency cycles are required.
4. In this example, RWDS indicates that additional initial latency cycles are required.
5. At the end of CA cycles the memory stops driving RWDS to allow the host HyperBus master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave.
6. During data transfer, RWDS is driven by the host to indicate which bytes of data should be either masked or loaded into the array.
7. The figure shows RWDS masking byte Dn A and byte Dn+1 B to perform an unaligned word write to bytes Dn B and Dn+1 A.

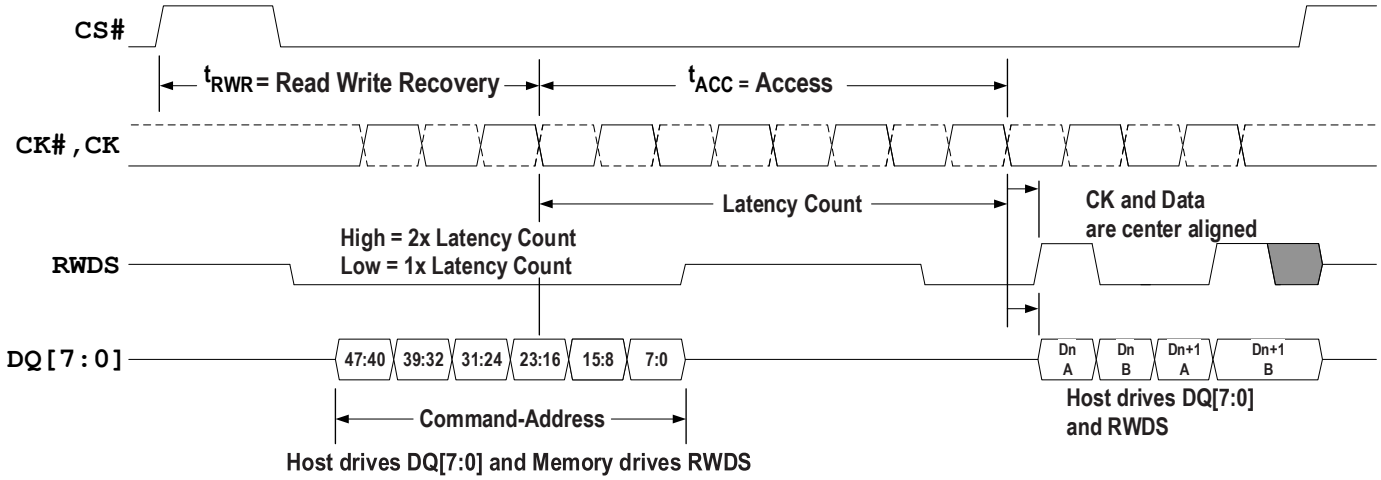

Figure 11 - Write Transaction without Additional Initial Latency

Notes:

1. During CA, RWDS is driven by the memory and indicates whether additional latency cycles are required.
2. In this example, RWDS indicates that there is no additional latency required.
3. At the end of CA cycles the memory stops driving RWDS to allow the host HyperBus master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave.
4. During data transfer, RWDS is driven by the host to indicate which bytes of data should be either masked or loaded into the array.
5. The figure shows RWDS masking byte Dn A and byte Dn+1 B to perform an unaligned word write to bytes Dn B and Dn+1 A.

7.4 Write Transactions without Initial Latency (Register Write)

A Write transaction starts with the first three clock cycles providing the Command/Address information indicating the transaction characteristics. CA0 may indicate that a Write transaction is to be performed and also indicates the address space and register Write.

Writes without initial latency are used for register space writes. HyperRAM device write transactions with zero latency mean that the CA cycles are followed by write data transfers. Writes with zero initial latency, do not have a turnaround period for RWDS. The HyperRAM device will always drive RWDS during the CA period to indicate whether extended latency is required for a transaction that has initial latency. However, the RWDS is driven before the HyperRAM devices has received the first byte of CA i.e. before the HyperRAM device knows whether the transaction is a read or write to register space. In the case of a write with zero latency, the RWDS state during the CA period does not affect the initial latency of zero. Since master write data immediately follows the CA period in this case, the HyperRAM device may continue to drive RWDS Low or may take RWDS to High-Z during write data transfer. The master must not drive RWDS during Writes with zero latency. Writes with zero latency do not use RWDS as a data mask function. All bytes of write data are written (full word writes).

The first byte of data in each word is presented on the rising edge of CK and the second byte is presented on the falling edge of CK. Write data is center aligned with the clock inputs. Write transfers can be ended at any time by bringing CS# High when clock is idle. The clock is not required to be free-running.

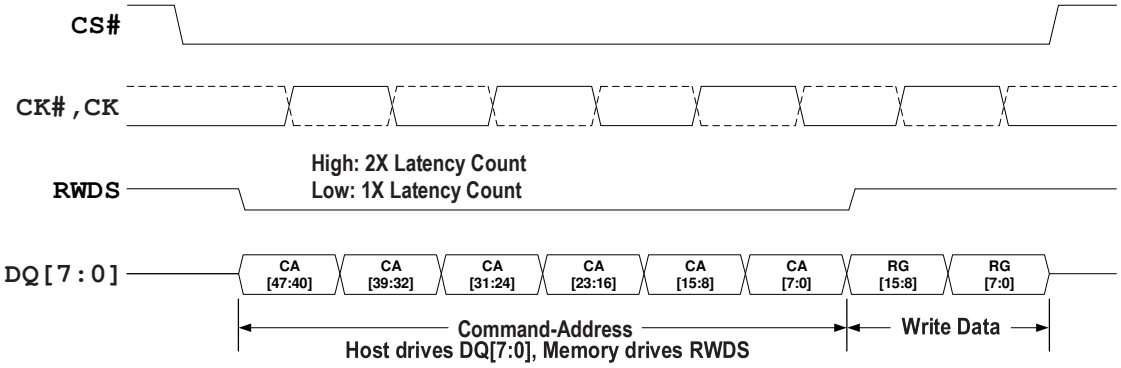

Figure 12 - Write Operation without Initial Latency

8. MEMORY SPACE

8.1 HyperBus Interface Memory Space addressing

Table 3 - Memory Space Address Map (word based - 16 bits)

Unit Type	Count	System Word Address Bits	CA Bits	Notes
Rows within 32 Mb pSRAM	4096 (Rows)	A20~A9	33~22	
Row	1 (row)	A8~A3	21~16	512 (word addresses) 1K bytes
Half-Page	8 (word addresses)	A2~A0	2~0	8 words (16 bytes)

Table 4 - Memory Space Address Map (word based - 16 bits)

		32Mb
Row Address	System Word Address Bits	A20~A9
	CA Bits	33~22
Column Address	System Word Address Bits	A8~A0
	CA Bits	21~16; 2~0
Half-Page (HP) Address	System Word Address Bits	A8~A3
	CA Bits	21~16
Word of HP Address	System Word Address Bits	A2~A0
	CA Bits	2~0

Notes:

1. A Page is a 16-word (32-byte) length and aligned unit of device internal read or write access and additional latency may be inserted by RWDS when crossing Page boundaries.
2. The Column address selects the burst transaction starting word location within a Row. The Column address is split into an upper and lower portion. The upper portion selects an 8-word (16-byte) half-page and the lower portion selects the word within a half-page where a read or write transaction burst starts.

8.1.1 Density and Row Boundaries

The DRAM array size (density) of the device can be determined from the total number of system address bits used for the row and column addresses as indicated by the Row Address Bit Count and Column Address Bit Count fields in the ID0 register. For example: a 32-Mbit HyperRAM device has 9 column address bits and 12 row address bits for a total of 21 word address bits = 2^{21}= 2M words = 4M bytes. The 9 column address bits indicate that each row holds 2^9 = 512 words = 1K bytes. The row address bit count indicates there are 4096 rows to be refreshed within each array refresh interval. The row count is used in calculating the refresh interval.

9. REGISTER SPACE

9.1 HyperBus Interface Register Addressing

When CA[46] is 1 a read or write transaction accesses the Register Space.

Table 5 - Register Space Address Map

Register	System Address	—	—	—	31~27	26~19	18~11	10~3	—	2~0
	CA Bits	47	46	45	44~40	39~32	31~24	23~16	15~8	7~0
Identification Register 0 (read only)		E0h				00h	00h	00h	00h	00h
Identification Register 1 (read only)		E0h				00h	00h	00h	00h	01h
Configuration Register 0 Read		E0h				00h	01h	00h	00h	00h
Configuration Register 0 Write		60h				00h	01h	00h	00h	00h
Configuration Register 1 Read		E0h				00h	01h	00h	00h	01h
Configuration Register 1 Write		60h				00h	01h	00h	00h	01h

9.2 Register Space Access

Register default values are loaded upon power-up or hardware reset. The registers can be altered at any time while the device is in the standby state.

Loading a register is accomplished with write transaction without initial latency using a single 16-bit word write transaction.

Each register is written with a separate single word write transaction. Register write transactions have zero latency, the single word of data immediately follows the CA. RWDS is not driven by the host during the write because RWDS is always driven by the memory during the CA cycles to indicate whether a memory array refresh is in progress. Because a register space write goes directly to a register, rather than the memory array, there is no initial write latency, related to an array refresh that may be in progress. In a register write, RWDS is also not used as a data mask because both bytes of a register are always written and never masked.

Reserved register fields must be written with their default value. Writing reserved fields with other than default values may produce undefined results.

Note: The host must not drive RWDS during a write to register space.

Note: The RWDS signal is driven by the memory during the CA period based on whether the memory array is being refreshed. This refresh indication does not affect the writing of register data.

Note: The RWDS signal returns to high impedance after the CA period. Register data is never masked. Both data bytes of the register data are loaded into the selected register.

Reading of a register is accomplished with read transaction with single or double initial latency using a single 16 bit read transaction. If more than one word is read, the same register value is repeated in each word read. The contents of the register is returned in the same manner as reading array data, with one or two latency counts, based on the state of RWDS during the CA period. The latency count is defined in the Configuration Register 0 Read Latency field (CR0[7:4]).

9.3 Device Identification Registers

There are two read only, non-volatile, word registers, that provide information on the device selected when CS# is low. The device information fields identify:

- Manufacture
- Type
- Density

Table 6 - ID Register 0 Bit Assignments

Bits	Function	Settings (Binary)
[15:7]	Reserved	Reserved
[6:4]	Density	101b - 32 Mb
[3:0]	Manufacturer	0000b - Reserved **1111b – Winbond** 0010b to 1111b - Reserved

Table 7 - ID Register 1 Bit Assignments

Bits	Function	Settings (Binary)
[15:4]	Reserved	0000_0000_0000b (default)
[3:0]	Device Type	1111b – HyperRAM 0000b to 1110b - Reserved

9.4 Configuration Register 0

Configuration Register 0 (CR0) is used to define the power state and access protocol operating conditions for the HyperRAM device. Configurable characteristics include:

- Wrapped Burst Length (16, 32, 64, or 128 byte aligned and length data group)
- Wrapped Burst Type
  – Legacy wrap (sequential access with wrap around within a selected length and aligned group)
- Initial Latency
- Variable Latency
  – Whether an array read or write transaction will use fixed or variable latency. If fixed latency is selected the memory will always indicate a refresh latency and delay the read data transfer accordingly. If variable latency is selected, latency for a refresh is only added when a refresh is required at the same time a new transaction is starting.
- Output Drive Strength
- Deep Power Down Mode

Table 8 - Configuration Register 0 Bit Assignments

CR0 Bit	Function	Settings (Binary)
[15]	Deep Power Down Enable	0b - Writing 0 to CR0[15] causes the device to enter Deep Power Down (DPD) 1b - Normal operation (default) Note: 1: HyperRAM will automatically set the value of CR0[15] to “1” after exit DPD.
[14:12]	Drive Strength	000b - 50 ohms (default) 001b - 35 ohms 010b - 100 ohms 011b - 200 ohms Others - Reserved
[11:8]	Reserved	1111b - Reserved (default) Reserved for Future Use. When writing this register, these bits should be set to 1 for future compatibility.
[7:4]	Initial Latency	0000b - 5 Clock Latency @ 133MHz Max Frequency 0001b - 6 Clock Latency @ 166MHz Max Frequency (default) 1110b - 3 Clock Latency @ 83MHz Max Frequency 1111b - 4 Clock Latency @ 104MHz Max Frequency Others - Reserved
[3]	Fixed Latency Enable	0b – Variable Initial Latency – 1 or 2 times Initial Latency depending on RWDS during CA cycles. 1b - Fixed 2 times Initial Latency (default)
[2]	Burst Type	0b: Reserved 1b: Wrapped burst sequences in legacy wrapped burst manner (default)
[1:0]	Burst Length	00b - 128 bytes 01b - 64 bytes 10b - 16 bytes 11b - 32 bytes (default)

9.4.1 Wrapped Burst

A wrapped burst transaction accesses memory within a group of words aligned on a word boundary matching the length of the configured group. Wrapped access groups can be configured as 16, 32, 64, or 128 bytes alignment and length.

During wrapped transactions, access starts at the CA selected location within the group, continues to the end of the configured word group aligned boundary, then wraps around to the beginning location in the group, then continues back to the starting location. Wrapped bursts are generally used for critical word first instruction or data cache line fill read accesses.

Table 9 - Example Wrapped Burst Sequences (HyperBus Addressing)

CA[45]	CR[2:0]	Burst Type	Wrap Boundary (Bytes)	Start Address (Hex)	Address Sequence (Hex) (Words)
0	100	Wrap 128	128	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, ...
0	101	Wrap 64	64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, ...
0	101	Wrap 64	64	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, ...
0	110	Wrap 16	16	XXXXXX02	02, 03, 04, 05, 06, 07, 00, 01, ...
0	110	Wrap 16	16	XXXXXX0C	0C, 0D, 0E, 0F, 08, 09, 0A, 0B, ...
0	111	Wrap 32	32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, ...
0	111	Wrap 32	32	XXXXXX1E	1E, 1F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, ...

9.4.2 Initial Latency

Register Space write transactions always have zero initial latency. RWDS may be High or Low during the CA period. The level of RWDS during the CA period does not affect the placement of register data immediately after the CA, as there is no initial latency needed to capture the register data. A refresh operation may be performed in the memory array in parallel with the capture of register data.

In the event a distributed refresh is required at the time a Memory Space read or writes transaction or Register Space read transaction begins, the RWDS signal goes high during the CA to indicate that an additional initial latency is being inserted to allow a refresh operation to complete before opening the selected row.

Memory Space read and writes transactions or Register Space read transactions require some initial latency to open the row selected by the CA. This initial latency is t_{ACC}. The number of latency clocks needed to satisfy t_{ACC} depends on the HyperBus frequency and can vary from 3 to 6 clocks. The value in CR0[7:4] selects the number of clocks for initial latency. The default value is 6 clocks, allowing for operation up to a maximum frequency of 166MHz prior to the host system setting a lower initial latency value that may be more optimal for the system.

9.4.3 Fixed Latency

A configuration register option bit CR0[3] is provided to make all Memory Space read and write transactions or Register Space read transactions require the same initial latency by always driving RWDS High during the CA to indicate that two initial latency periods are required. This fixed initial latency is independent of any need for a distributed refresh; it simply provides a fixed (deterministic) initial latency for all of these transaction types. The fixed latency option may simplify the design of some HyperBus memory controllers or ensure deterministic transaction performance. Fixed latency is the default POR or reset configuration. The system may clear this configuration bit to disable fixed latency and allow variable initial latency with RWDS driven high only when additional latency for a refresh is required.

9.4.4 Drive Strength

DQ and RWDS signal line loading, length, and impedance vary depending on each system design. Configuration register bits CR0[14:12] provide a means to adjust the DQ[7:0] and RWDS signal output impedance to customize the DQ and RWDS signal impedance to the system conditions to minimize high speed signal behaviors such as overshoot, undershoot, and ringing. The default POR or reset configuration value is 000b select to 50 ohms output impedance.

The HyperRAM support nominal impedance of 35, 50, 100 and 200 Ohms at VCC/2. The impedance values may vary from the typical values depending on the Process, Voltage, and Temperature (PVT) conditions. Impedance will increase with slower process, lower voltage, or higher temperature. Impedance will decrease with faster process, higher voltage, or lower temperature.

Each system design should evaluate the data signal integrity across the operating voltage and temperature ranges to select the best drive strength settings for the operating conditions.

9.4.5 Deep Power Down

When the HyperRAM device is not needed for system operation, it may be placed in a very low power consuming state called Deep Power Down (DPD), by writing 0 to CR0[15]. When CR0[15] is cleared to 0, the device enters the DPD state within t_{DPDIN} time and all refresh operations stop. The data in RAM is lost, (becomes invalid without refresh) during DPD state. Exiting DPD requires driving CS# Low then High, POR, or a reset. Only CS# and RESET# signals are monitored during DPD mode. All register content might lost in Deep Power Down State and the device powers-up in its default state.

9.5 Configuration Register 1

Configuration Register 1 (CR1) is used to define the refresh array size, refresh rate and Hybrid Sleep for the HyperRAM device. Configurable characteristics include:

- Partial Array Refresh
- Hybrid Sleep State
- Refresh Rate

Table 10 - Configuration Register 1 Bit Assignments

CR1 Bit	Function	Settings (Binary)
[15-7]	Reserved	000000000b - Reserved (default) When writing this register, these bits should keep 000000000b for future compatibility.
[6]	Refresh Rate	0b - The HyperRAM refresh the internal cell array using faster rate 1b - The HyperRAM refresh the internal cell array using normal rate
[5]	Hybrid Sleep	0b - Normal operation (default) 1b - Writing 1 to CR1[5] causes the device to enter Hybrid Sleep (HS) State
[4:3]	Reserved	00b – Reserved When writing this register, these bits should keep 00b
[2:0]	Partial Array Refresh	000b - Full Array (default) 001b - Bottom 1/2 Array 010b - Bottom 1/4 Array 011b - Bottom 1/8 Array 100b - None 101b - Top 1/2 Array 110b - Top 1/4 Array 111b - Top 1/8 Array Note: The array means default 32Mb density.

9.5.1 Partial Array Refresh

The partial array refresh configuration restricts the refresh operation in HyperRAM to a portion of the memory array specified by CR1[2:0]. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

CR1[2:0]	System Word Address Space	Refresh Range
000	000000h – 1FFFFFh	Full array
001	000000h – 0FFFFFh	Bottom 1/2 array
010	000000h – 07FFFFh	Bottom 1/4 array
011	000000h – 03FFFFh	Bottom 1/8 array
100	None	None
101	100000h – 1FFFFFh	Top 1/2 array
110	180000h – 1FFFFFh	Top 1/4 array
111	1C0000h – 1FFFFFh	Top 1/8 array

9.5.2 Hybrid Sleep

When the HyperRAM is not needed for system operation, it may be placed in Hybrid Sleep state if data in the device needs to be retained. Enter Hybrid Sleep state by writing 1 to CR1[5]. Bringing CS# Low will cause the device to exit HS state and set CR1[5] to 0. Also, POR, or a hardware reset will cause the device to exit Hybrid Sleep state. Note that a POR or a hardware reset disables refresh where the memory core data can potentially get lost.

Hybrid Sleep Mode: CR1[5], Default = Disabled

- 1: HyperRAM is entering at Hybrid Sleep Mode

- 0: Normal operation (default)

Write “1” into CR1[5] will force HyperRAM entering Hybrid Sleep Mode.

CR1[5] will be self-cleared to “0” after Hybrid Sleep Mode exited.

9.5.3 Refresh Multiplier Indicator

CR1[6]: Refresh multiplier indicator, read only. Write operation will not affect this bit.

0: The HyperRAM refresh the intern cell array using faster rate.

1: The HyperRAM refresh the internal cell array using normal rate.

10. INTERFACE STATES

10.1 Power Conservation Modes

10.1.1 Interface Standby

Standby is the default, low power, state for the interface while the device is not selected by the host for data transfer (CS#= High). All inputs and outputs other than CS# and RESET# are ignored in this state.

10.1.2 Hybrid Sleep

The HyperRAM will significantly decrease internal power consumption when staying at Hybrid Sleep Mode with keeping maintaining data stored in cell array, but, will not respond any data read/write command or status register read/write commands, also, allow without clock signal input.

Write “1” into CR1[5] will force HyperRAM entering Hybrid Sleep Mode. HyperRAM will enter Hybrid Sleep Mode after received the register write command on CR1[5] for entering Hybrid Sleep Mode.

To assert CE# to logic LOW level for at least 60nS time will force HyperRAM exiting Hybrid Sleep Mode. The HyperRAM will take at least 70µS, t_{HSMX}, to leave Hybrid Sleep Mode after recognizing the exiting signal (asserting CE# to logic LOW level for at least 60nS, t_{HSMXC}).

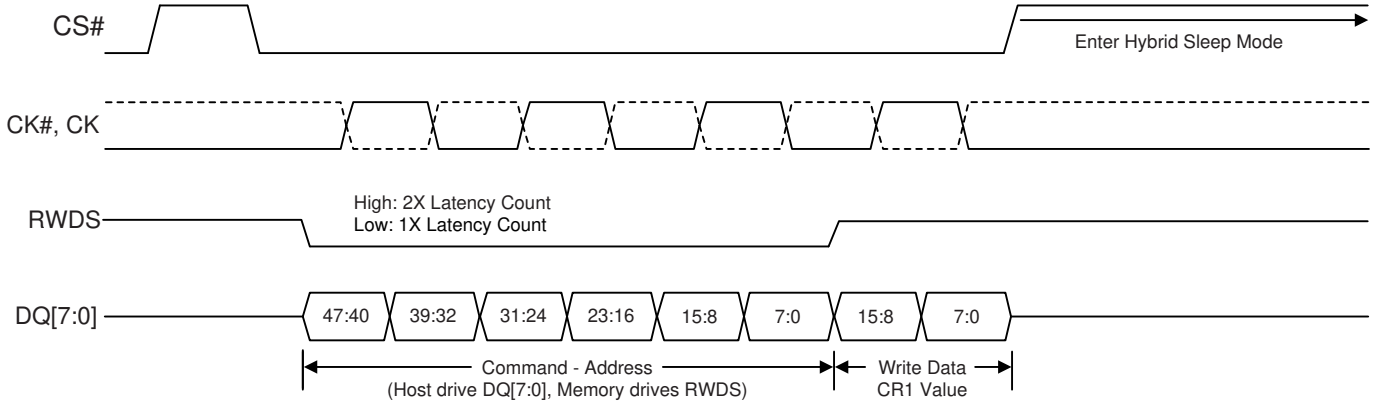

Figure 13 - Enter Hybrid Sleep Transaction

Figure 14 - Exit Hybrid Sleep Transaction

10.1.3 Deep Power Down

In the Deep Power down (DPD) state, current consumption is driven to the lowest possible level (I_{DPD}). DPD state is entered by writing a 0 to CR0[15]. The device reduces power within t_{DPDIN} time and all refresh operations stop. The data in Memory Space is lost, (becomes invalid without refresh) during DPD state. Driving CS# Low then High will cause the device to exit DPD state. Also, POR, or a hardware reset will cause the device to exit DPD state. Returning to Standby state requires t_{DPDOUT} time. Returning to Standby state following a POR requires t_{VCS} time, as with any other POR. Following the exit from DPD due to any of these events, the device is in the same state as following POR.

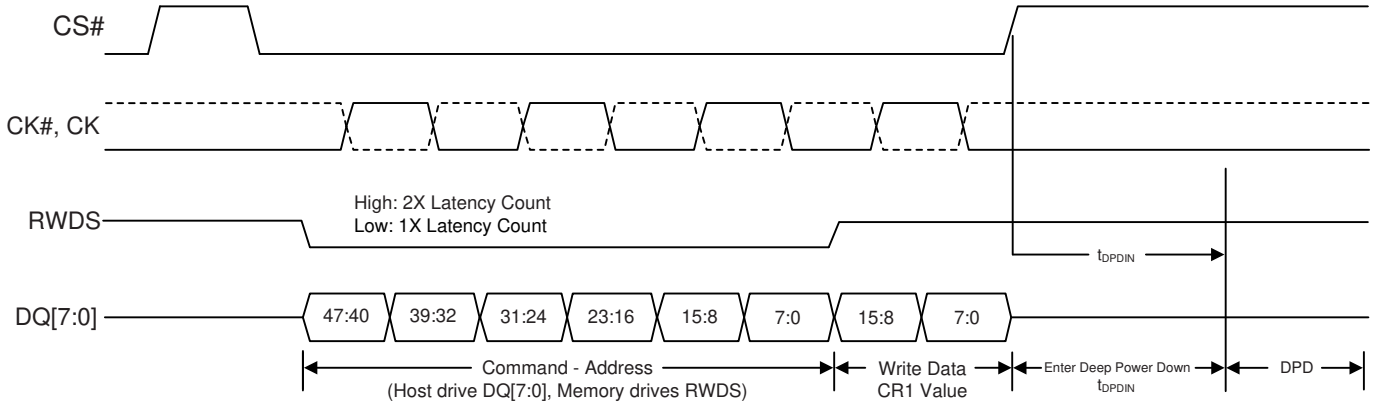

Figure 15 - Enter DPD Transaction

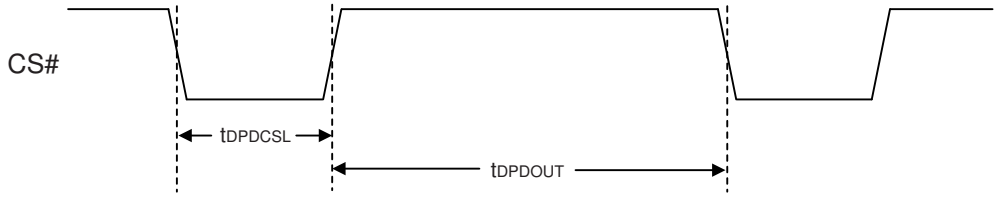

Figure 16 - Exit DPD Transaction

11. ELECTRICAL SPECIFICATIONS

11.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Voltage on V_{CC} supply relative to V_{SS}	-0.2	+2.45	V	1
Voltage to any pad except V_{CC} relative to V_{SS}	-0.3	V_{CC} +0.3	V	1
Storage temperature (plastic)	-55	+150	°C	1

Note:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

11.2 Operating Ranges

11.2.1 Electrical Characteristics and Operating Conditions

Parameter	Description	Test Conditions	Min	Max	Unit
V_{CC}	Power Supply Voltage		1.7	1.95	V
V_{CC}	I/O Power Supply Voltage		1.7	1.95	V
V_{IL}	Input Low Voltage		–0.5	0.3 x V_{CC}	V
V_{IH}	Input High Voltage		0.7 x V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = +0.1mA		0.15 x V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –0.1mA	0.85 x V_{CC}		V
V_{IX}	AC Differential Crossing voltage		V_{CC} x 0.4	V_{CC} x 0.6	V
I_{LI}	Input Leakage Current	V_{IN} = 0 to V_{CC}		2	µA
I_{LO}	Output Leakage Current	Chip disabled		1	µA

Note:

1. All parts list in section 2 order information table will not guarantee to meet functional and AC specification if the V_{CC} operation condition out of range mentioned in above table.

11.2.2 Operating Temperature

Parameter	Symbol	Range	Unit	Notes
Operating Temperature	TCASE	-40~85	°C	1

Note:

1. All parts list in section 2 order information table will not guarantee to meet functional and AC specification if the operation temperature range out of range mentioned in above table.

11.2.3 IDD Characteristics

Parameter	Description	Test Conditions	25°C	85°C	Unit	Notes
			Typ.	Max.		
I_{CC2}	Initial access, burst Read/Write	V_{IN} = V_{CC} or 0V, chip enabled, I_{OUT} = 0	15	18	mA	4, 5
I_{CC3R}	Continuous burst Read	V_{IN} = V_{CC} or 0V, chip enabled, I_{OUT} = 0	10	12	mA	4, 5
I_{CC3W}	Continuous burst Write	V_{IN} = V_{CC} or 0V, chip enabled, I_{OUT} = 0	10	12	mA	4, 5
I_{RST}	Reset Current	CS# = V_{IH}, RESET# = V_{SS} ± 0.3V, V_{CC} = V_{CC} max	1	1	mA	
I_{DPD}	Deep Power Down Current	V_{IN} = V_{CC} or 0V, V_{CC} = 1.95V; +85°C		10	µA	

Idle Standby and Hybrid Sleep Current

Parameter	Description	Test Conditions		25°C Typ.	85°C Max.	Unit	Notes
IDLE-ISB	Idle Standby Current	CS# = V_{CC}, V_{IN} = V_{CC} or 0V	Full Array	80	250	µA	6, 7
			Bottom 1/2 Array	70	200		
			Bottom 1/4 Array	60	150		
			Bottom 1/8 Array	50	100		
			Top 1/2 Array	70	200		
			Top 1/4 Array	60	150		
			Top 1/8 Array	50	100		
HSM-ISB	Hybrid Sleep Current Standby	CS# = V_{CC}, V_{IN} = V_{CC} or 0V	Full Array	20		µA	6, 7
			Bottom 1/2 Array	18			
			Bottom 1/4 Array	16			
			Bottom 1/8 Array	15			
			Top 1/2 Array	18			
			Top 1/4 Array	16			
			Top 1/8 Array	15			

Notes:

1. Input signals may overshoot to V_{CC} + 1.0V for periods less than 2nS during transitions.
2. Input signals may undershoot to V_{SS} – 1.0V for periods less than 2nS during transitions.
3. Drive strength is set as 35 ohms.
4. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
5. I_{CC3R}(typ) and I_{CC3W}(typ) are the average value measured with Full Array and at 25°C.this is data for reference only.
6. IDLE-ISB (typ) and HSM-ISB (typ) are the average value measured at 25°C. In order to achieve low standby current, all inputs must be driven to either V_{CC} or V_{SS}. HSM-ISB is measured after 150 mS after entering Hybrid Sleep Mode. The instant peak current should not be over 15mA.
7. IDLE-ISB (max) is measured at allowed maximum operating temperature. In order to achieve low standby current, all inputs must be driven to either V_{CC} or V_{SS}. IDLE-ISB is measured after 500mS after power-up or when entering standby mode.

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11.2.4 Power-Up Initialization

HyperRAM products include an on-chip voltage sensor used to launch the power-up initialization process. VCC must be applied simultaneously. When the power supply reaches a stable level at or above VCC (min), the device will require t_{VCS} time to complete its self-initialization process.

The device must not be selected during power-up. CS# must follow the voltage applied until VCC (min) is reached during power-up, and then CS# must remain high for a further delay of t_{VCS}. A simple pull-up resistor from VCC to Chip Select (CS#) can be used to insure safe and proper power-up.

If RESET# is Low during power up, the device delays start of the t_{VCS} period until RESET# is High. The t_{VCS} period is used primarily to perform refresh operations on the DRAM array to initialize it.

When initialization is complete, the device is ready for normal operation.

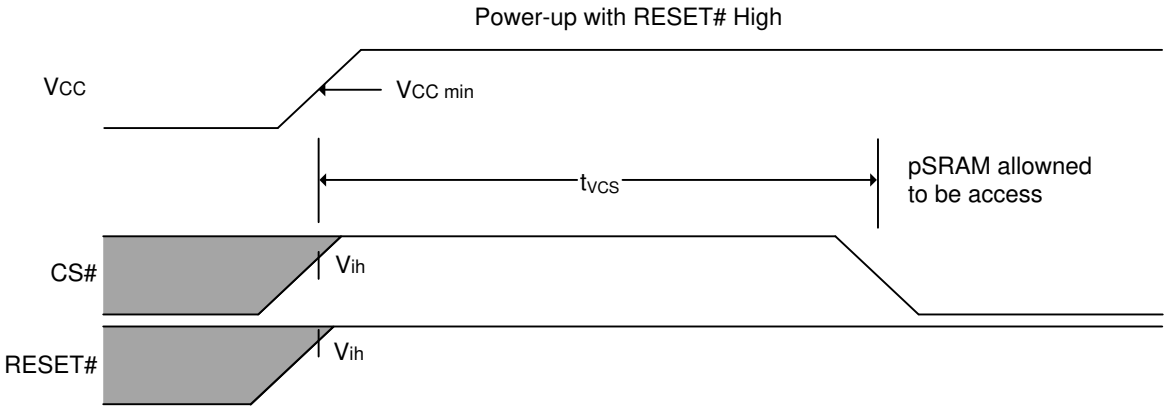


Figure 17 - Power-up with RESET# High

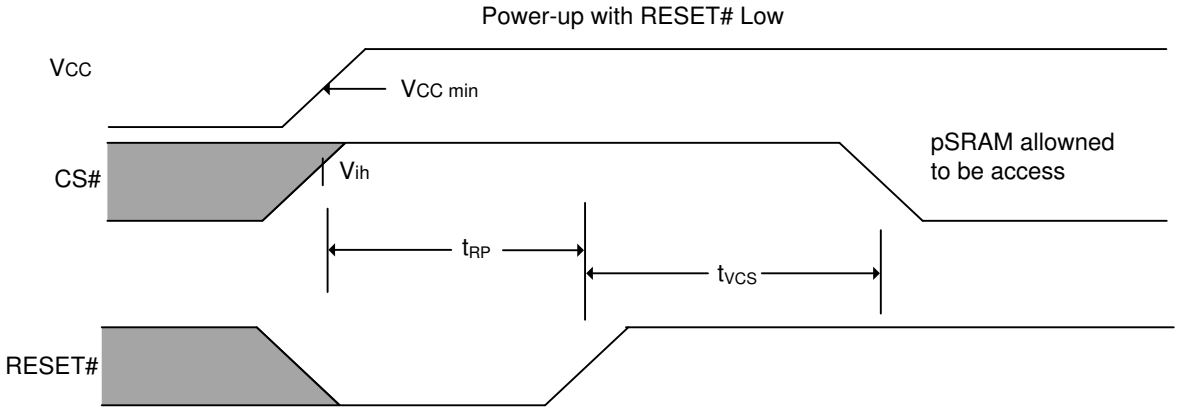


Figure 18 - Power-up with RESET# Low

Table 11 - Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
VCC	VCC Power Supply	1.7	1.95	V
t_{VCS}	VCC ≥ minimum and RESET# High to first access	–	150	µS

Notes:

1. Bus transactions (read and write) are not allowed during the power-up reset time (t_{VCS}).
2. VCC ramp rate may be non-linear.

11.2.5 Hardware Reset

The RESET# input provides a hardware method of returning the device to the standby state.

During t_{RPH} the device will draw I_{RST} current. If RESET# continues to be held Low beyond t_{RPH}, the device draws CMOS standby current (IDLE-ISB). While RESET# is Low (during t_{RP}), and during t_{RPH}, bus transactions are not allowed.

A hardware reset will:

- Cause the configuration registers to return to their default values
- Halt self-refresh operation while RESET# is low - memory array data is considered as invalid
- Force the device to exit the Hybrid Sleep state
- Force the device to exit the Deep Power Down state

After RESET# returns high, the self-refresh operation will resume. Because self-refresh operation is stopped during RESET# Low, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh. This may result in the loss of pSRAM array data during or immediately following a hardware reset. The host system should assume pSRAM array data is lost after hardware reset and reload any required data.

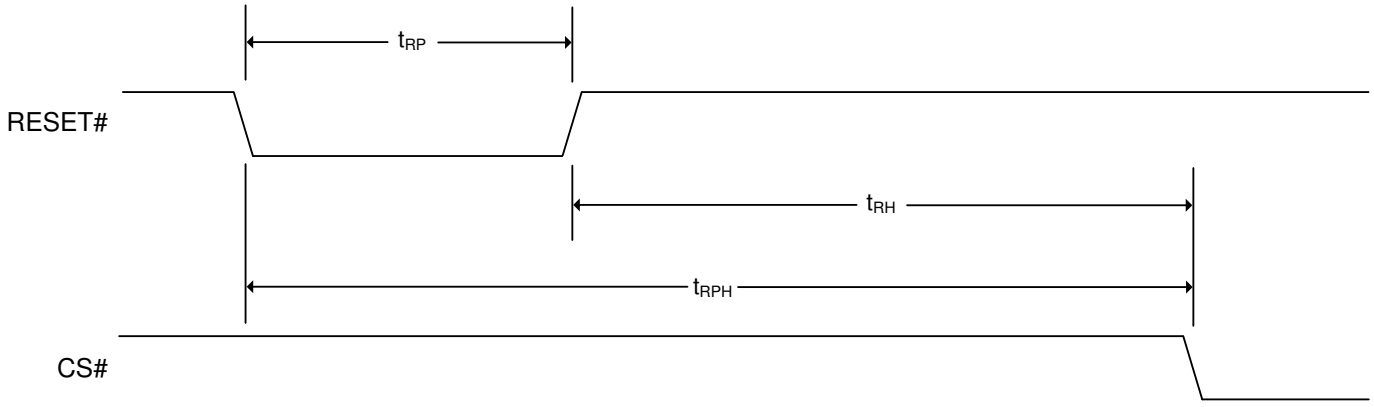


Figure 19 - Hardware Reset Timing Diagram

Table 12 - Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
t_{RP}	RESET# Pulse Width	200	–	nS
t_{RH}	Time between RESET# (High) and CS# (Low)	200	–	nS
t_{RPH}	RESET# Low to CS# Low	400	–	nS

Note: The RESET# pad is 4V tolerant.

11.2.6 Capacitance Characteristics

Table 13 - Capacitive Characteristics

Parameter	Description	Min	Max	Unit	Notes
C_{IN}	Input Capacitance	0.2	2.5	pF	1, 2
C_{IO}	Input / Output Capacitance (DQ)	0.3	3.5	pF	1

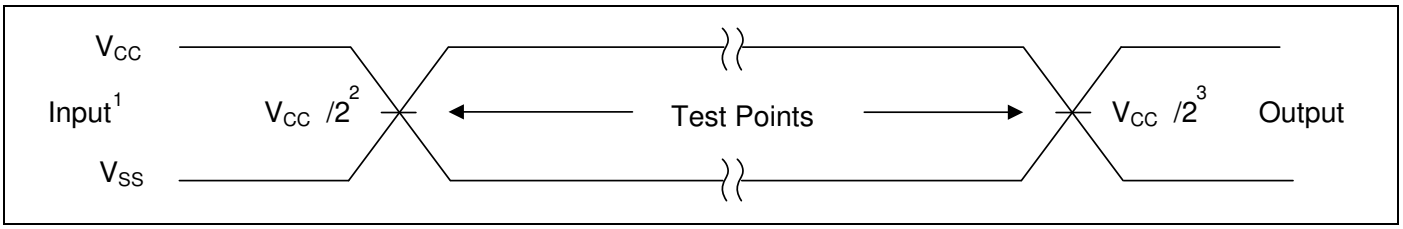
Notes:

1. These parameters are verified in die device (does not include package capacitance).
2. C_{IN} includes CK, CK# and CS# only.

12. TIMING SPECIFICATIONS

The following section describes HyperRAM device dependent aspects of timing specifications.

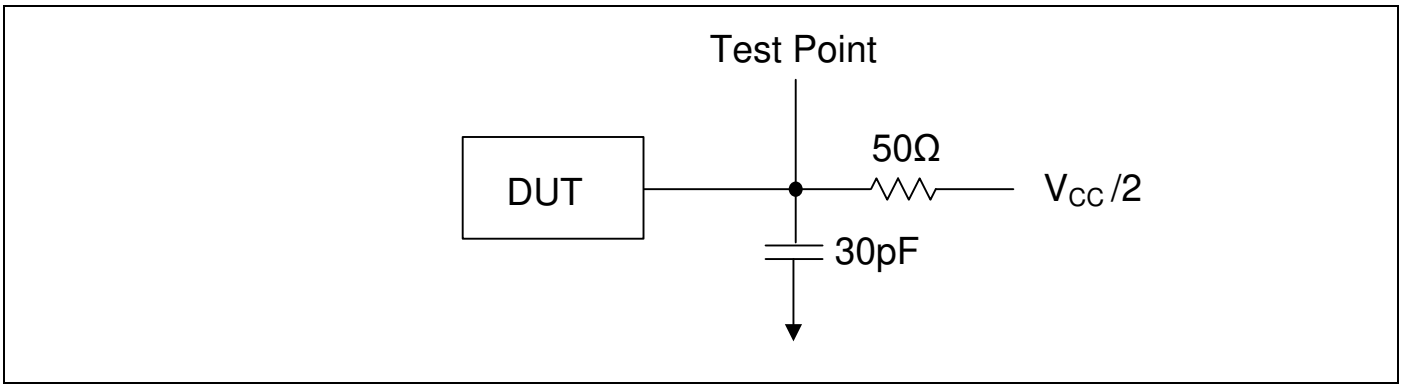
12.1 AC Input-Output Reference Waveform



Notes:

1. AC test inputs are driven at VCC for a logic 1 and VSS for a logic 0. Input rise and fall times (10% to 90%) < 1.6nS.
2. Input timing begins at VCC/2.
3. Output timing ends at VCC/2.

12.2 AC Test Conditions



Note:

All tests are performed with the outputs configured for default setting of half drive strength

Figure 20 - Test load reference

12.3 AC Characteristics

12.3.1 Read Transactions

Table 14 - HyperRAM Specific Read Timing Parameters

Parameter	Symbol	166 MHz		Unit	Notes
		Min	Max		
Clock Period	t_{CK}	6	1000	nS	Note4
Clock high-level width	t_{CH}	0.45	0.55	t_{CK}	Note4
Clock low-level width	t_{CL}	0.45	0.55	t_{CK}	Note4
Chip Select High Between Transactions	t_{CSHI}	6	–	nS	
HyperRAM Read-Write Recovery Time	t_{RWR}	36	-	nS	
Chip Select Setup to next CK Rising Edge	t_{CSS}	2	-	nS	Note1
Data Strobe Valid	t_{DSV}	–	8	nS	
Input Setup Time	t_{IS}	0.9	–	nS	
Input Hold Time	t_{IH}	0.9	–	nS	
HyperRAM Read Initial Access Time	t_{ACC}	36	-	nS	
Clock to DQs Low Z	t_{DQLZ}	0	–	nS	
CK transition to DQ Valid	t_{CKD}	1	5.5	nS	Note2
CK transition to DQ Invalid	t_{CKDI}	0	4.6	nS	
Data Valid (t_{DV} min = the lesser of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or t_{CKHP} min - t_{CKD} min + t_{CKDI} min)	t_{DV}	1.25	–	nS	
CK transition to RWDS Valid	t_{CKDS}	1	5.5	nS	Note2
CK transition to RWDS valid (with additional latency	t_{CKDSR}	1	8	nS	
RWDS transition to DQ Valid	t_{DSS}	-0.4	0.4	nS	
RWDS transition to DQ Invalid	t_{DSH}	-0.4	0.4	nS	
Chip Select Hold After CK Falling Edge	t_{CSH}	0	–	nS	Note1,2,3
Chip Select Inactive to RWDS High-Z	t_{DSZ}	–	6	nS	
Chip Select Inactive to DQ High-Z	t_{OZ}	–	6	nS	

Notes:

1. t_{CSS} and t_{CSH} are the timing requirement for HyperBus device to correctly latch the input signal of CS# using CK/CK# clock input for internal circuit controller. For the HyperBus device correctly latch the status of input signal of CS# using CK/CK# clock input, t_{CSS} must be larger than 2nS and t_{CSH} must be larger than 0nS.
2. For Read Transaction, at the end of transaction, CS# is able to be pull HIGH after the falling edge of last clock. The RWDS will transit to valid state after t_{CKDS} and the DQ data will to valid state after t_{CKD}. However, the output buffer of HyperBus device will be disabled when CS# is HIGH and the output data will be go to Hi-Z in a time of t_{OZ}. t_{DSZ} after CS# transit to HIGH.
3. For the controller to correctly latch the desired last output data, CS# must remain driven low for one or more additional clock periods, so that data remains valid long enough to cover t_{CKD}, t_{CKDS}, and the controller interface phase shift of RWDS.
4. All parts list in section 2 order information table will not guarantee to meet functional and AC specification if the t_{CK}, t_{CH} and t_{CL} out of range mentioned in above table.

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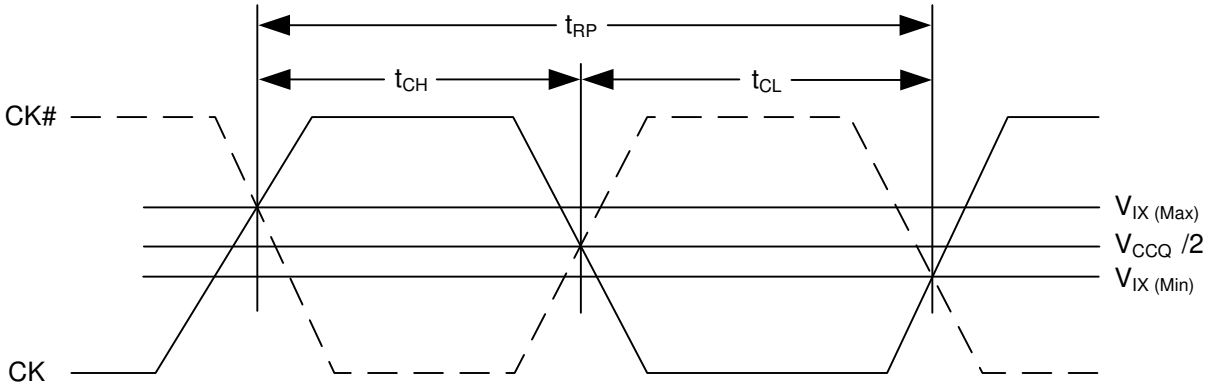

Figure 21 - Clock Characteristics

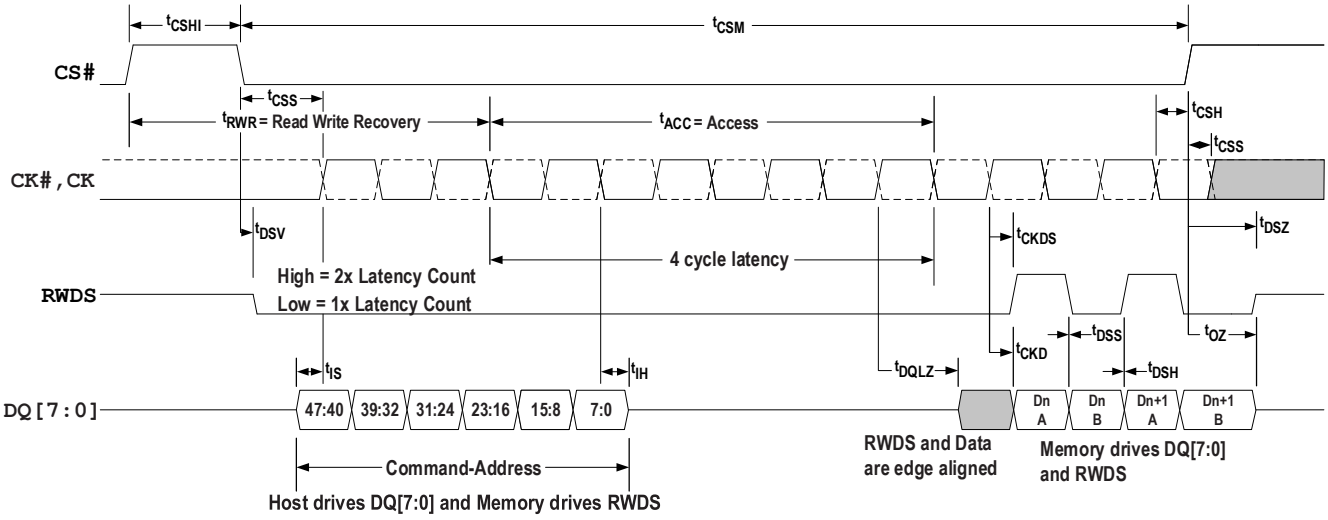

Figure 22 - Read Timing Diagram — No Additional Latency Required

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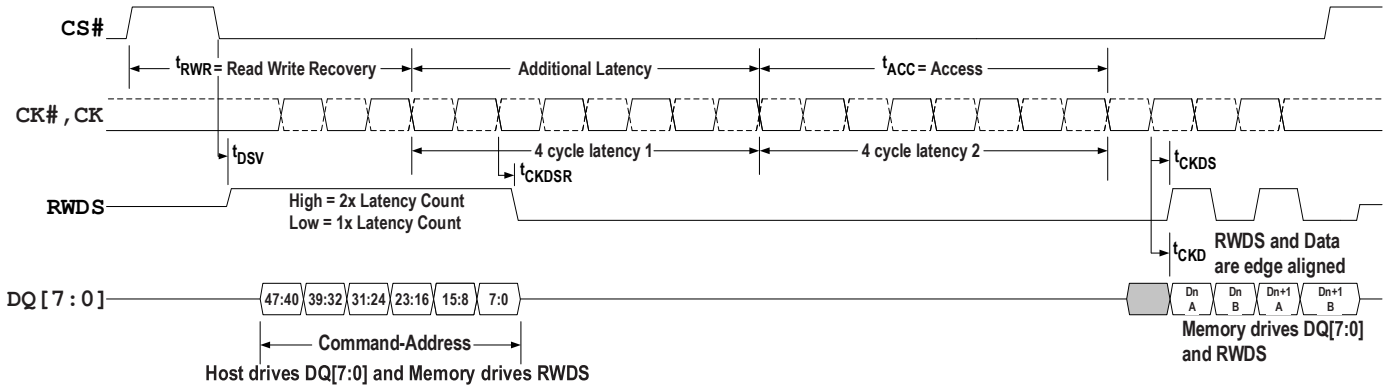

Figure 23 - Read Timing Diagram — With Additional Latency

Notes:

1. Timing parameters applicable to HyperBus interfaces.
2. Transactions must be initiated with CK = Low and CK# = High.
3. CS# must return High before a new transaction is initiated.
4. The memory drives RWDS during the entire Read transaction.
5. Transactions without additional latency count have RWDS Low during CA cycles. Transactions with additional latency count have RWDS High during CA cycles and RWDS returns low at t_{DSH}. All other timing relationships are the same for both figures although they are not shown in the second figure. A four cycle latency is used for illustration purposes only. The required latency count is device and clock frequency dependent.
6. These parameters are required by HyperRAM.

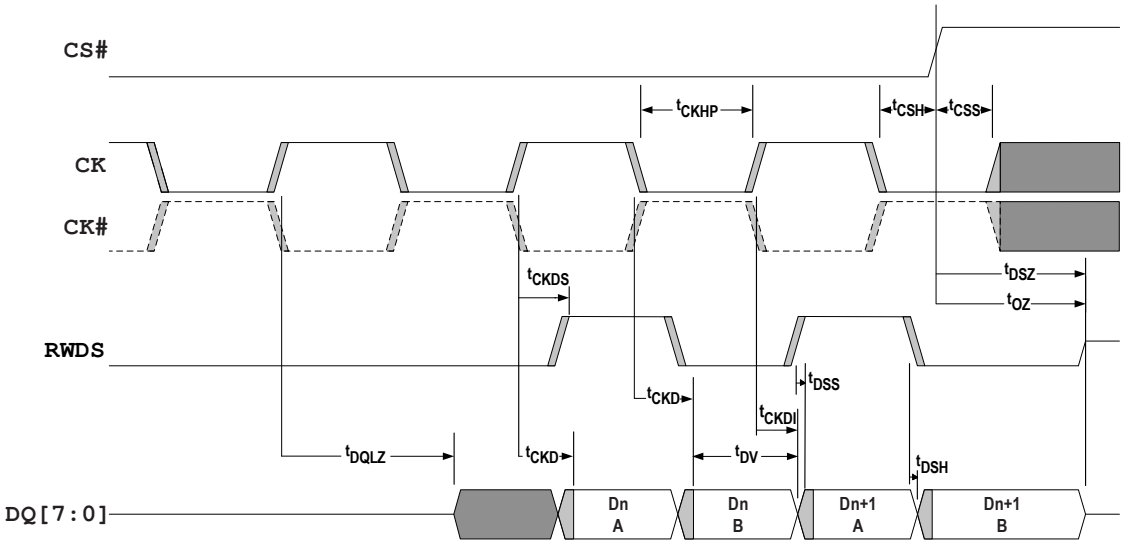

Figure 24 - Data Valid Timing

Notes:

1. This figure shows a closer view of the data transfer portion of read transaction diagrams to more clearly show the Data Valid period as affected by clock jitter and clock to output delay uncertainty.
2. The t_{CKD} and t_{CKDI} timing parameters define the beginning and end position of the data valid period.
3. The t_{DSS} and t_{DSH} timing parameters define how early or late RWDS may transition relative to the transition of data. This is the potential skew between the clock to data delay t_{CKD}, and clock to data strobe delay t_{CKDS}. Aside from this skew, the t_{CKD}, t_{CKDI}, and t_{CKDS} values track together (vary by the same ratio) because RWDS and Data are outputs from the same device under the same voltage and temperature conditions.

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12.3.2 Write Transactions

Table 15 - Write Timing Parameters

Description	Type	Parameter	166 MHz		Unit
			Min	Max	
Read-Write Recovery Time	R/W	t_{RWR}	36	–	nS
Access Time	R/W	t_{ACC}	36	–	nS
Chip Select Maximum Low Time (TCASE < 85°C)	R/W	t_{CSM}	–	4	µS
Data Mask Valid (RWDS setup to end of initial latency)	W	t_{DMV}	0	–	µS

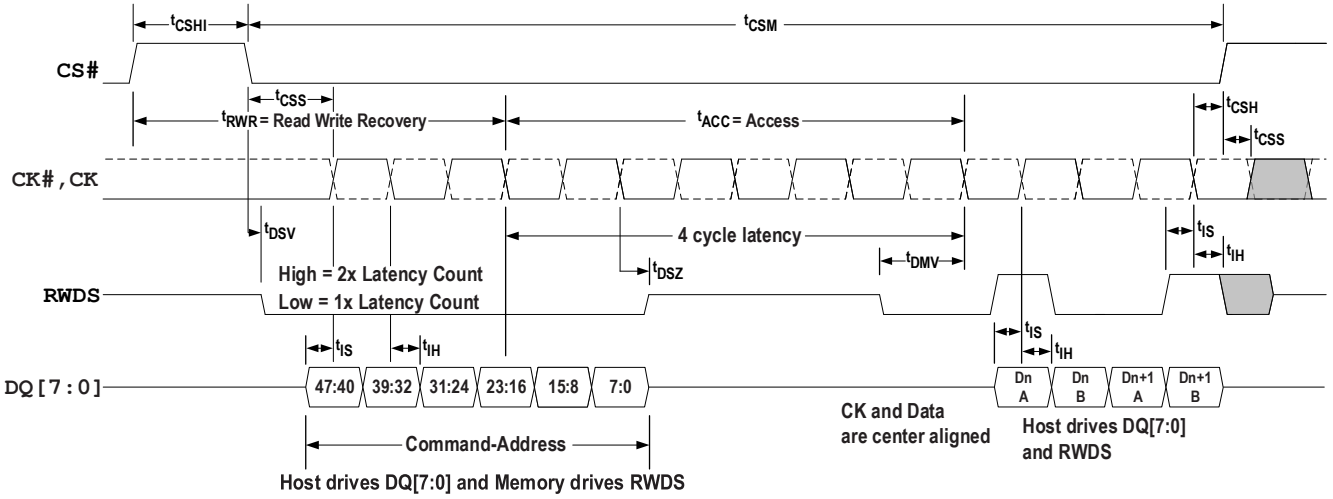

Figure 25 - Write Timing Diagram — No Additional Latency

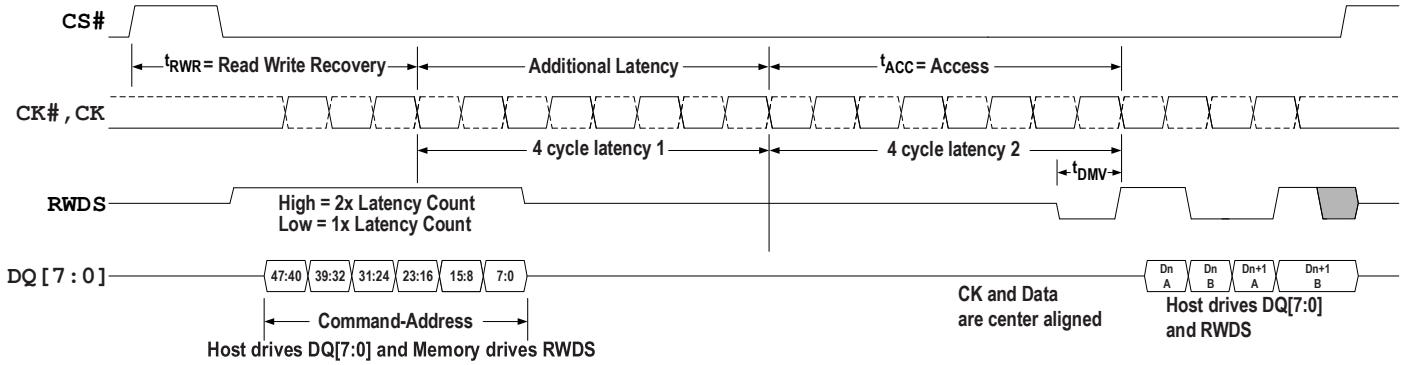

Figure 26 - Write Timing Diagram — With Additional Latency

Notes:

1. Timing parameters applicable to HyperBus interfaces.
2. Transactions must be initiated with CK=Low and CK#=High. CS# must return High before a new transaction is initiated.
3. During write transactions with latency, RWDS is used as an additional latency indicator initially and is then used as a data mask during data transfer.
4. Transactions without additional latency count have RWDS Low during CA cycles. Transactions with additional latency count have RWDS High during CA cycles and RWDS returns low at t_{DSH}. All other timing relationships are the same for both figures although they are not shown in the second figure. A four cycle latency is used for illustration purposes only. The required latency count is device and clock frequency dependent.
5. At the end of Command-Address cycles the memory stops driving RWDS to allow the host HyperBus master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave. This can be done during the last cycle of the initial latency.
6. The write transaction shown demonstrates the Dn A byte and the Dn+1 B byte being masked. Only Dn B byte and Dn+1 A byte are modified in the array. Dn A byte and Dn+1 B byte remain unchanged.

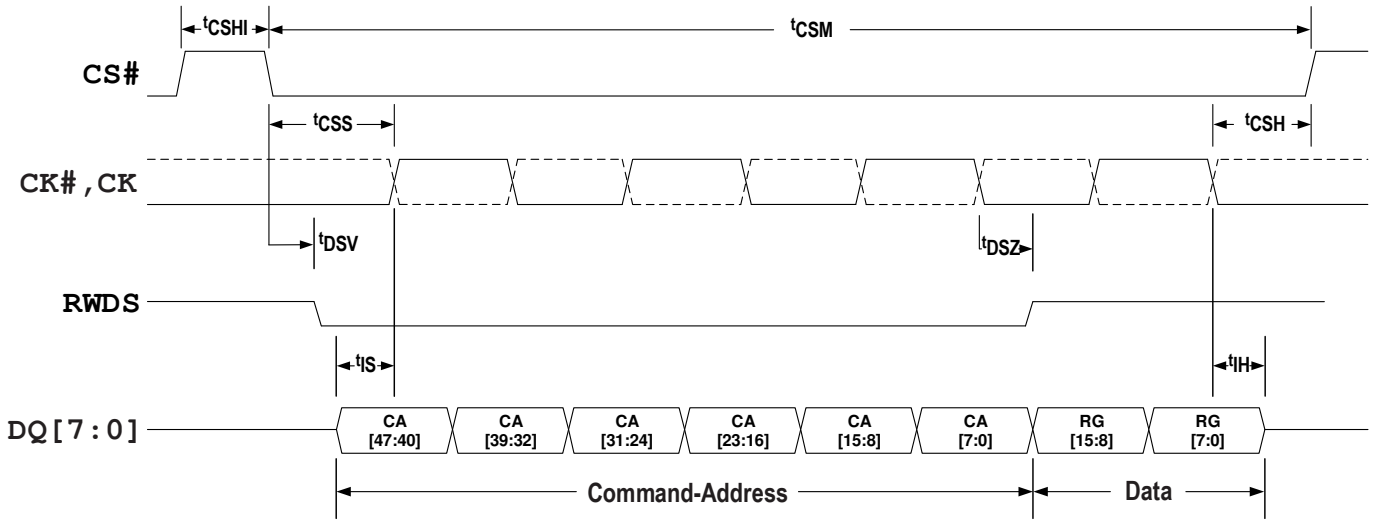

Figure 27 - Write Operation without Initial Latency (Register Write)

Notes:

1. Transactions must be initiated with CK=Low and CK#=High. CS# must return High before a new transaction is initiated.
2. Writes with zero initial latency, do not have a turnaround period for RWDS. The slave device will always drive RWDS during the Command-Address period to indicate whether extended latency is required for a transaction that has initial latency. However, the RWDS is driven before the slave device has received the first byte of CA, that is, before the slave knows whether the transaction is a read or write, to memory space or register space. In the case of a write with zero latency, the RWDS state during the CA period does not affect the initial latency of zero. Since master write data immediately follows the Command-Address period in this case, the slave may continue to drive RWDS Low or may take RWDS to High-Z during write data transfer. The master must not drive RWDS during Writes with zero latency. Writes with zero latency do not use RWDS as a data mask function. All bytes of write data are written (full word writes).

12.3.3 Hybrid Sleep Timings

Table 16 - Hybrid Sleep Timing Parameters

Description	Parameter	Min	Max	Unit
Hybrid Sleep Mode exiting command time (time for CE# low)	t_{HSMXC}	60		nS
Hybrid Sleep Mode exiting time	t_{HSMX}	–	70	µS

12.3.4 Deep Power down Timings

Table 17 - Deep Power down Timing Parameters

Description	Parameter	Min	Max	Unit
DPD register write to DPD power level	t_{DPDIN}	10	–	µS
CS# Low period to cause an exit from DPD	t_{DPDCSL}	200	–	nS
CS# Low then High to Standby wakeup time	t_{DPDOUT}	–	150	µS

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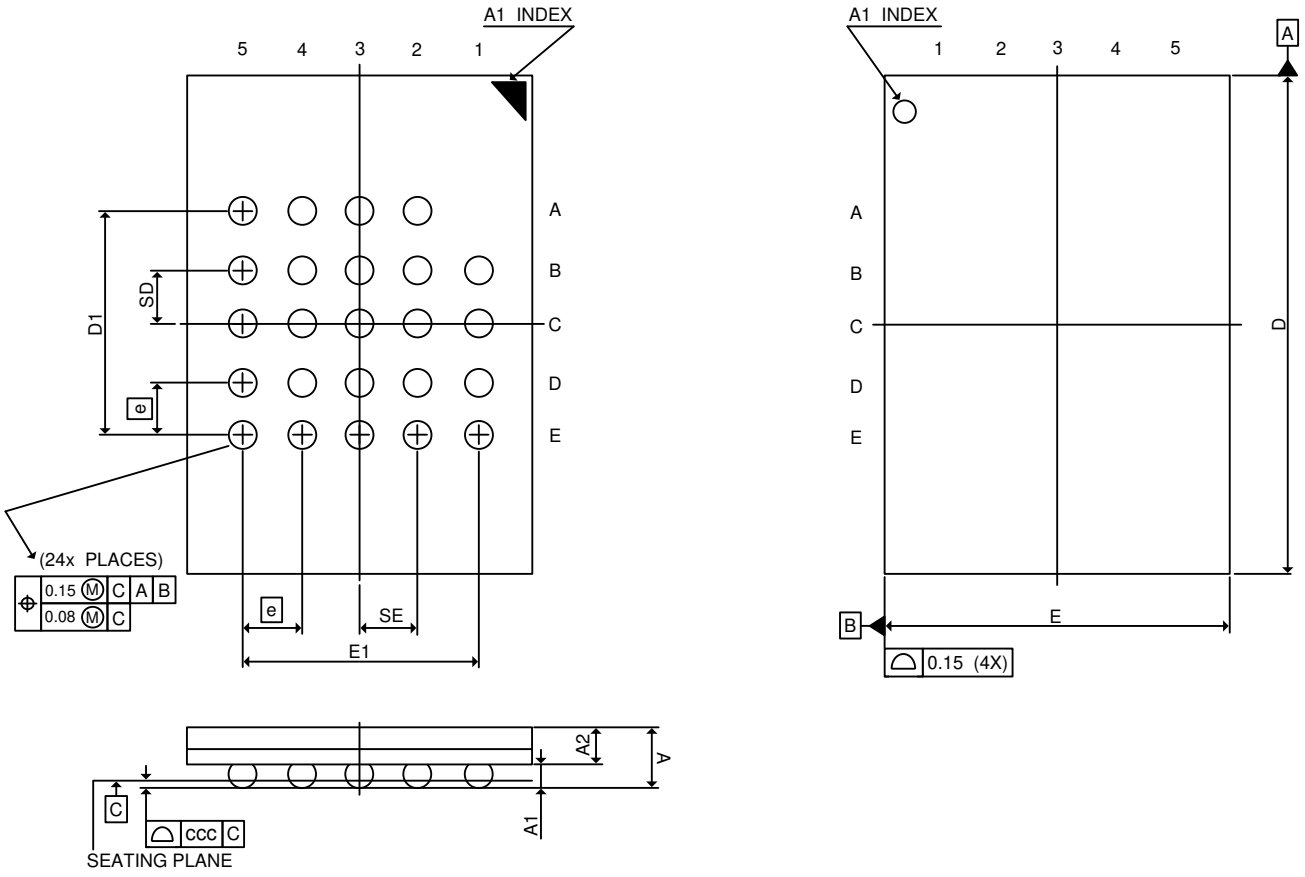
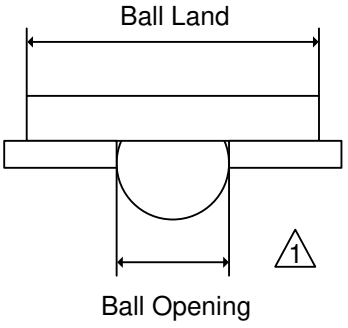
13. PACKAGE SPECIFICATION

Package Outline TFBGA24 Ball (6x8 mm² (5x5-1 ball arrays), Ball pitch: 1.00mm, Ø=0.40mm)



Controlling Dimensions are in milmeters

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	0.047
A1	0.26	0.31	0.36	0.010	0.012	0.014
A2	---	0.85	---	---	0.033	---
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	4.00 BSC			0.157 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.00 BSC			0.157 BSC		
SE	1.00 TYP			0.039 TYP		
SD	1.00 TYP			0.039 TYP		
e	1.00 BSC			0.039 TBSC		
ccc	---	---	0.10	---	---	0.0039



Note:
1. Ball land: 0.45mm. Ball opening: 0.35mm
   PCB Ball land suggested ≤ 0.35mm

14. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01-001	Jun. 05, 2019	All	Initial formal datasheet

Note: The content of this document is subject to change without notice.