HA5351

64ns Sample and Hold Amplifier

FN3690
Rev 11.00
April 25, 2013

The HA5351 is a fast acquisition, wide bandwidth sample and hold amplifier, built with the Intersil HBC-10 BiCMOS process. This sample and hold amplifier offers a combination of desirable features; fast acquisition time (70ns to 0.01% maximum), excellent DC precision and extremely low power dissipation, making it ideal for use in systems that sample multiple signals and require low power.

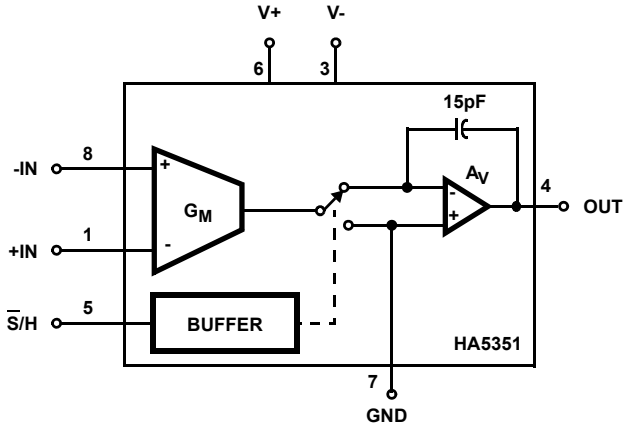
The HA5351 is in an open loop configuration with fully differential inputs providing flexibility for user defined feedback. In unity gain the HA5351 is completely self-contained and requires no external components. The on-chip 15pF hold capacitor is completely isolated to minimizing droop rate and reducing sensitivity to pedestal error. The HA5351 is available in 8 lead SOIC package for minimizing board space and ease of layout.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
HA5351IBZ	5351 IBZ	-40 to +85	8 Ld SOIC	M8.15

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Functional Diagram



Features

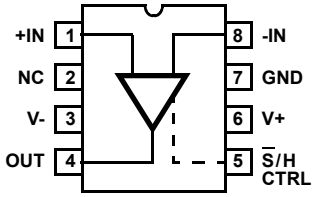
- Fast Acquisition to 0.01%. . . . . 70ns (Max)
- Low Offset Error . . . . . ±2mV (Max)
- Low Pedestal Error. . . . . ±10mV (Max)
- Low Droop Rate . . . . . 2µV/µs (Max)
- Wide Unity Gain Bandwidth 40MHz
- Low Power Dissipation . . . . . .220mW (Max)
- Total Harmonic Distortion (Hold Mode) . . . . . -72dBc - (V_{IN} = $5V_{P-P}$ at 1MHz)
- Fully Differential Inputs
- On Chip Hold Capacitor
- Pb-Free (RoHS Compliant)

Applications

- Synchronous Sampling
- Wide Bandwidth A/D Conversion
- Deglitching
- Peak Detection
- High Speed DC Restore

Pinout

HA5351
(8 LD SOIC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals . . . . . +11V
Differential Input Voltage 6V
Voltage Between Sample and Hold Control and Ground . . . . . +5.5V
Output Current, Continuous . . . . . ±37mA

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	160

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profilesee link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = 0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Voltage Range		Full	-2.5	-	+2.5	V
Input Resistance (Note 2)		+25	100	500	-	kΩ
Input Capacitance		+25	-	-	5	pF
Input Offset Voltage		+25	-2	-	2	mV
		Full	-3.0	-	3.0	mV
Offset Voltage Temperature Coefficient		Full	-	15	-	µV/°C
Bias Current		Full	-	2.5	5	µA
Offset Current		Full	-1.5	-	+1.5	µA
Common Mode Range		Full	-2.5	-	+2.5	V
Common Mode Rejection Ratio	±2.5V, Note 3	Full	60	80	-	dB
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	V_{OUT} = ±2.5V	+25	95	108	-	dB
		Full	85	-	-	dB
Unity Gain -3dB Bandwidth		25	-	40	-	MHz
TRANSIENT RESPONSE						
Rise Time	200mV Step	+25	-	8.5	-	ns
Overshoot	200mV Step	+25	0	-	30	%
Slew Rate	5V Step	Full	88	105	-	V/µs
DIGITAL INPUT CHARACTERISTICS						
Input Voltage	V_{IH}	+25, +85	2.1	-	5.0	V
		-40	2.4	-	5.0	V
	V_{IL}	Full	0	-	0.8	V
Input Current	V_{IL} = 0V	Full	-1.0	-	1.0	µA
	V_{IH} = 5V	Full	-1.0	-	1.0	µA
OUTPUT CHARACTERISTICS						
Output Voltage	R_L = 510Ω	Full	-3.0	-	+3.0	V
Output Current	R_L = 100Ω	+25, +85	20	25	-	mA
		-40	15	-	-	mA
Full Power Bandwidth	$5V_{P-P}$, A_V = +1, -3dB	Full	-	13	-	MHz
Output Resistance	Hold Mode	+25	-	0.02	-	Ω
Total Output Noise (DC to 10MHz)	Sample Mode	+25	-	325	-	μV_{RMS}
	Hold Mode	+25	-	325	-	μV_{RMS}

Electrical Specifications Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = 0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
DISTORTION CHARACTERISTICS						
SAMPLE MODE						
Total Harmonic Distortion	V_{IN} = 4.5V_{P-P}, f_{IN} = 100kHz	+25	-	-80	-	dBc
	V_{IN} = 5V_{P-P}, f_{IN} = 1MHz	+25	-	-74	-	dBc
	V_{IN} = 1V_{P-P}, f_{IN} = 10MHz	+25	-	-57	-	dBc
Signal to Noise Ratio (RMS Signal to RMS Noise)	V_{IN} = 4.5V_{P-P}, f_{IN} = 100kHz	+25	-	73	-	dB
HOLD MODE (50% Duty Cycle S/H)						
Total Harmonic Distortion	V_{IN} = 4.5V_{P-P}, f_{IN} = 100kHz, $f_S \cong$ 100kHz	+25	-	-78	-	dBc
	V_{IN} = 5V_{P-P}, f_{IN} = 1MHz, $f_S \cong$ 1MHz	+25	-	-72	-	dBc
	V_{IN} = 1V_{P-P}, f_{IN} = 10MHz, $f_S \cong$ 1MHz	+25	-	-51	-	dBc
Signal to Noise Ratio (RMS Signal to RMS Noise)	V_{IN} = 4.5V_{P-P}, f_{IN} = 100kHz, $f_S \cong$ 100kHz	+25	-	70	-	dB
SAMPLE AND HOLD CHARACTERISTICS						
Acquisition Time	0V to 2.0V Step to ±1mV	+25	-	53	-	ns
	0V to 2.0V Step to 0.01% (±200µV)	+25	-	64	70	ns
	-2.5V to +2.5V Step to 0.01% (±500µV)	+25	-	90	100	ns
Droop Rate		+25	-	0.3	-	µV/µs
		Full	-2	-	2	µV/µs
Hold Step Error	V_{IL} = 0V, V_{IH} = 4.0V, t_R = 5ns	Full	-10	-	+10	mV
Hold Mode Settling Time	To ±1mV	+25	-	50	-	ns
Hold Mode Feedthrough	5V_{P-P}, 500kHz, Sine	+25	-	72	-	dB
EADT (Effective Aperture Delay Time)		+25	-	+1	-	ns
Aperture Time (Note 2)		+25	-	10	-	ns
Aperture Uncertainty		+25	-	10	20	ps
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current		Full	-	20	22	mA
Negative Supply Current		Full	-	20	22	mA
PSRR	10% Delta	Full	60	74	-	dB

NOTES:

2. Derived from Computer Simulation only, not tested.
3. +CMRR is measured from 0V to +2.5V, -CMRR is measured from 0V to -2.5V.

Typical Performance Curves

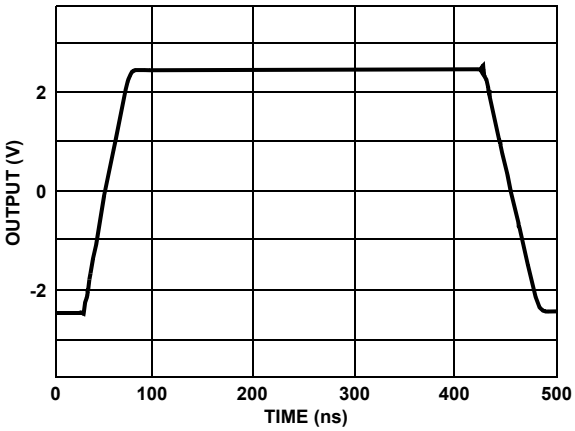


FIGURE 1. LARGE SIGNAL RESPONSE

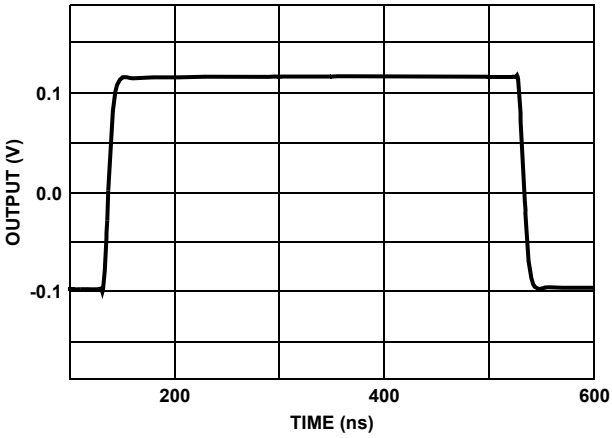


FIGURE 2. SMALL SIGNAL RESPONSE

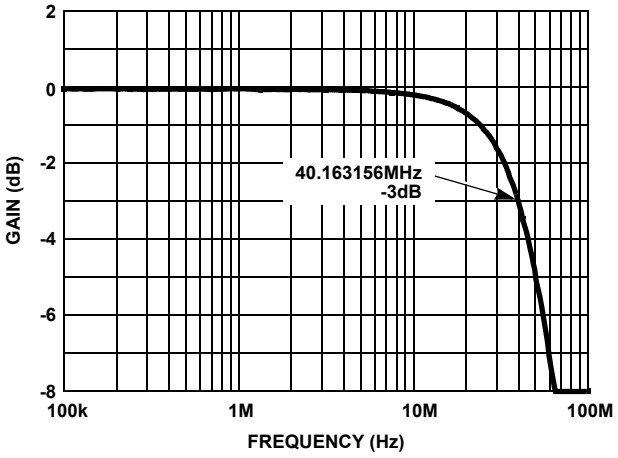


FIGURE 3. UNITY GAIN FREQUENCY RESPONSE

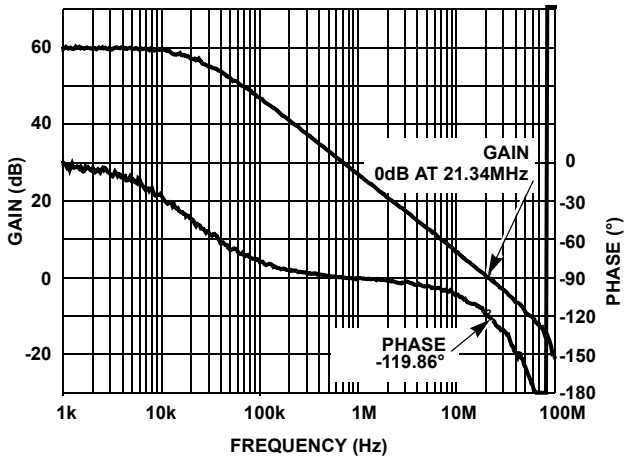


FIGURE 4. CLOSED LOOP GAIN/PHASE A_V = +1000

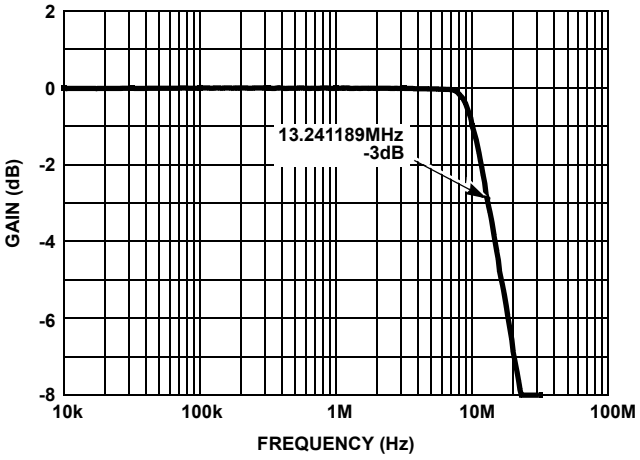


FIGURE 5. $5V_{P-P}$ FULL POWER FREQUENCY RESPONSE

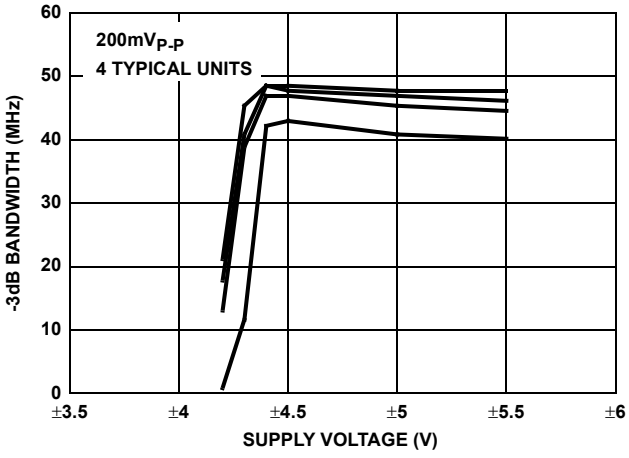


FIGURE 6. -3dB BANDWIDTH vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

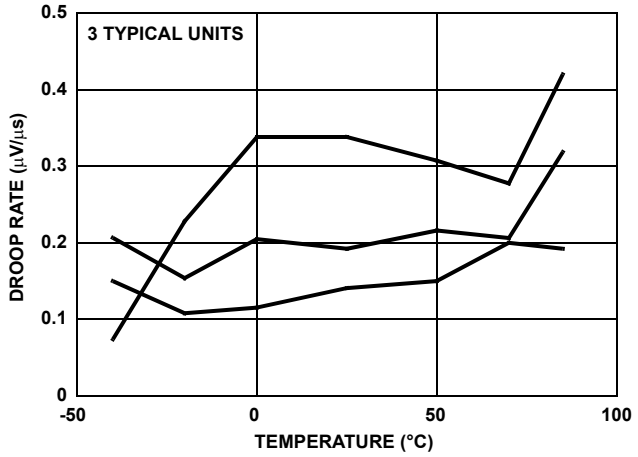


FIGURE 7. DROOP RATE vs TEMPERATURE

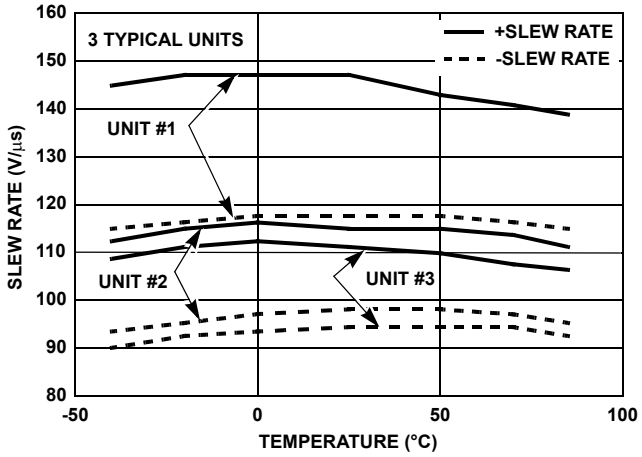


FIGURE 8. SLEW RATE vs TEMPERATURE

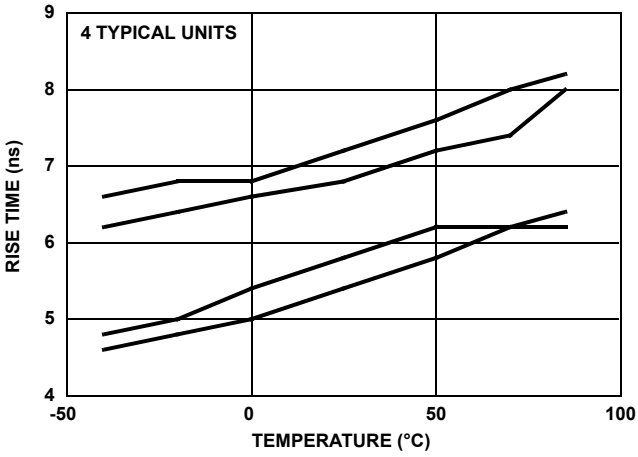


FIGURE 9. RISE TIME vs TEMPERATURE

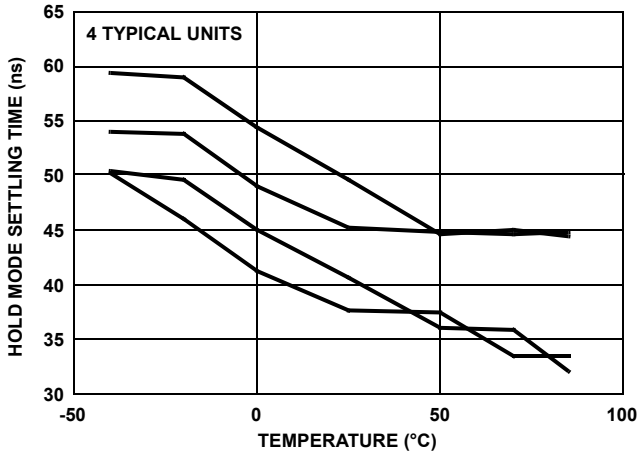


FIGURE 10. HOLD MODE SETTLING vs TEMPERATURE

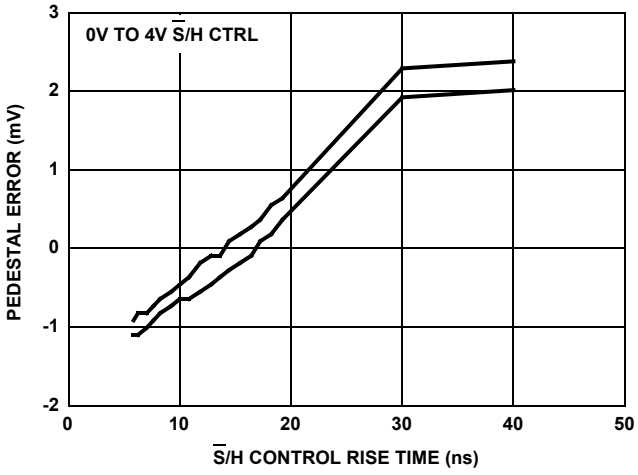


FIGURE 11. PEDESTAL vs S/H CONTROL RISE TIME

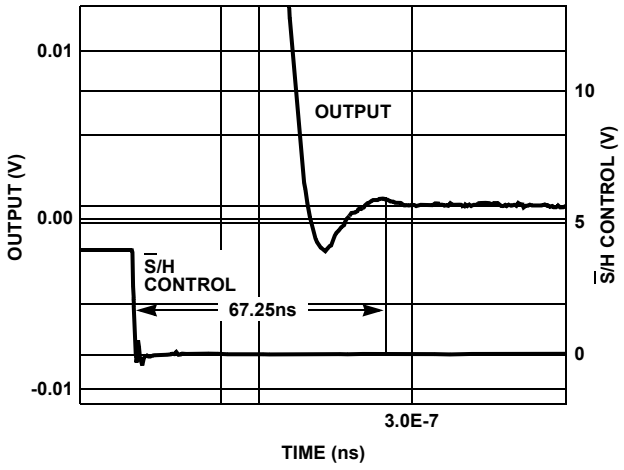


FIGURE 12. ACQUISITION TIME (0.01%, 0V TO 2V STEP)

Typical Performance Curves (Continued)

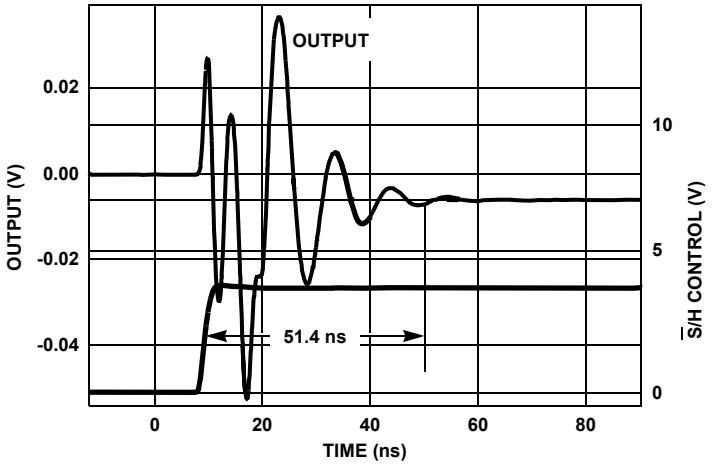


FIGURE 13. HOLD MODE SETTLING TIME (±200μV)

Die Characteristics

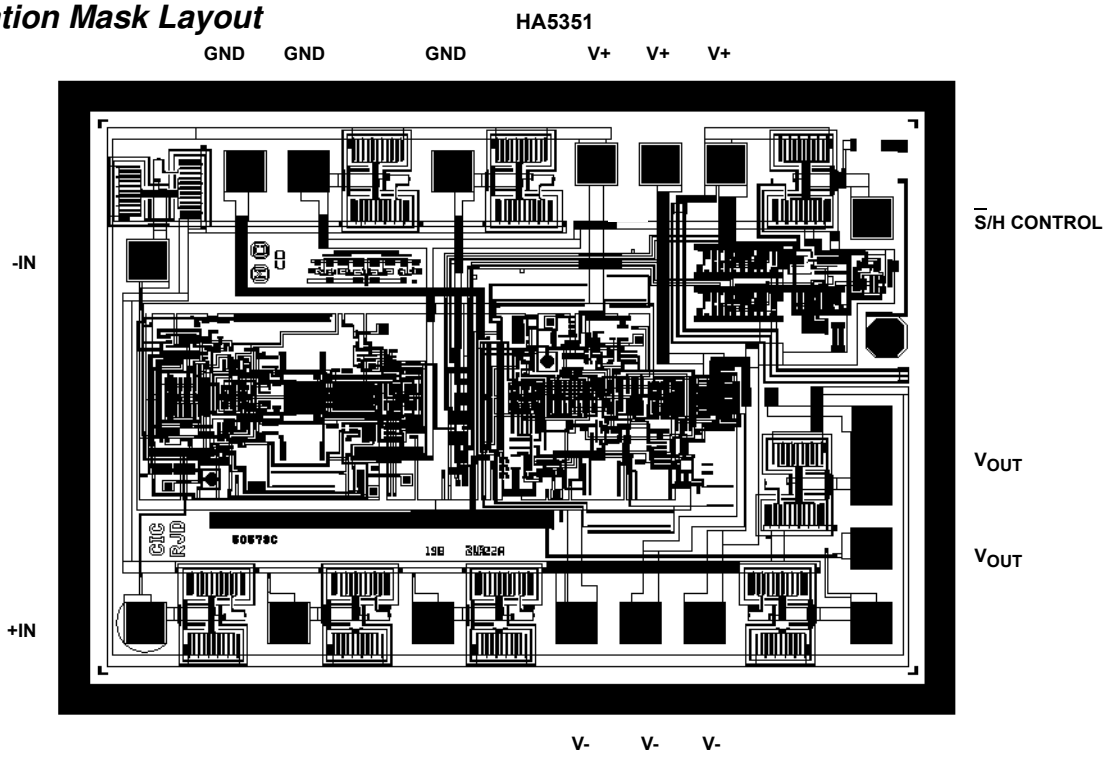
SUBSTRATE POTENTIAL:

V-

TRANSISTOR COUNT:

156

Metallization Mask Layout

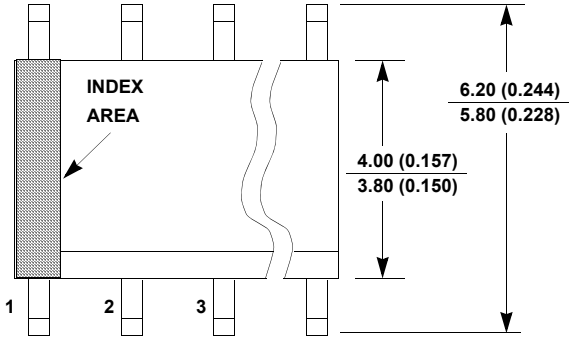


Package Outline Drawing

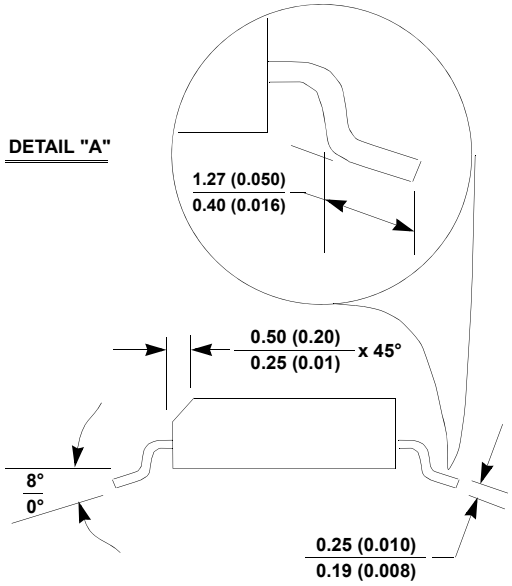
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

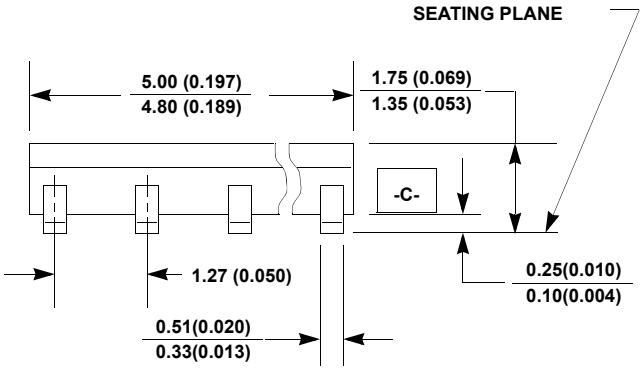
Rev 4, 1/12



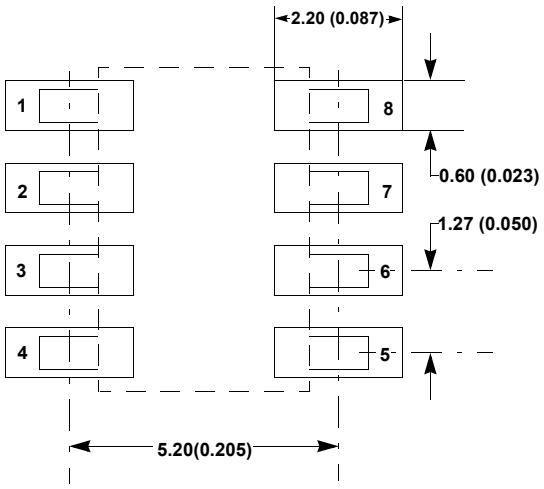
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.