



GAN140-650FBE

650 V, 140 mOhm Gallium Nitride (GaN) FET in a DFN
5 mm x 6 mm package

19 April 2023

Product data sheet

1. General description

The GAN140-650FBE is a general purpose 650 V, 140 m Ω Gallium Nitride (GaN) FET in a DFN 5 mm x 6 mm surface mount package. It is a normally-off e-mode device offering superior performance.

2. Features and benefits

- Enhancement mode - normally-off power switch
- Ultra high frequency switching capability
- No body diode
- Low gate charge, low output charge
- Qualified for standard applications
- ESD protection
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density
- Low package inductance and low package resistance

3. Applications

- High power density and high efficiency power conversion
- AC-to-DC converters, totem pole PFC
- DC-to-DC converters
- Fast battery charging, mobile phone, laptop, tablet and USB type-C chargers
- Datacom and telecom (AC-to-DC and DC-to-DC) converters
- Motor drives
- Solar (PV) inverters
- Class D audio amplifiers, TV PSU and LED drivers

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$-55\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$	-	-	650	V
V_{TDS}	transient drain to source voltage	pulsed; $t_p = 1\text{ }\mu\text{s}$; $\delta_{factor} = 0.01$	-	-	800	V
I_D	drain current	$V_{GS} = 6\text{ V}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$	[1]	-	17	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 1	-	-	113	W
T_j	junction temperature		-55	-	150	$^{\circ}\text{C}$
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 6\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 11 ; Fig. 12 ; Fig. 13	-	106	140	m Ω
		$V_{GS} = 6\text{ V}$; $I_D = 5\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$; Fig. 11 ; Fig. 14	-	230	-	m Ω

650 V, 140 mOhm Gallium Nitride (GaN) FET in a DFN 5 mm x 6 mm package

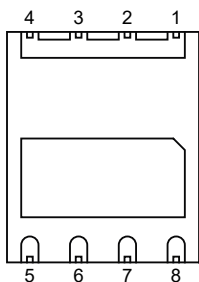
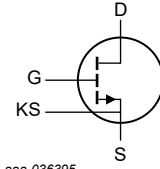
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _G	gate resistance	f = 5 MHz; T _j = 25 °C; open drain	-	3.5	-	Ω
Dynamic characteristics						
Q _{GD}	gate-drain charge	I _D = 5 A; V _{DS} = 400 V; V _{GS} = 6 V; T _j = 25 °C; Fig. 15 ; Fig. 16	-	1.2	-	nC
Q _{G(tot)}	total gate charge		-	3.5	-	nC
Q _{oss}	output charge	V _{GS} = 0 V; V _{DS} = 400 V; T _j = 25 °C	[2]	33	-	nC

[1] Limited by device saturation

[2] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since Q_r = Q_{oss} + Q_D, and Q_D = 0. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN5060-5 (SOT8075-1)</p>	 <p>aaa-036395</p>
2	D	drain		
3	D	drain		
4	D	drain		
5	S	source		
6	S	source		
7	KS	kelvin source		
8	G	gate		
mb	S	mounting base; connected to source		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
GAN140-650FBE	DFN5060-5	plastic thermal enhanced small outline package; no leads; 5 terminals; body: 5 × 6 × 0.9 mm	SOT8075-1

7. Marking

Table 4. Marking codes

Type number	Marking code
GAN140-650FBE	140IFBE

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	-55 °C ≤ T _j ≤ 150 °C	-	650	V

650 V, 140 mOhm Gallium Nitride (GaN) FET in a DFN 5 mm x 6 mm package

Symbol	Parameter	Conditions	Min	Max	Unit
V _{TDS}	transient drain to source voltage	pulsed; t _p = 1 μs; δ _{factor} = 0.01	-	800	V
V _{GS}	gate-source voltage		-1.4	7	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	113	W
I _D	drain current	V _{GS} = 6 V; T _{mb} = 25 °C	[1]	17	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 2	[1]	32	A
T _{stg}	storage temperature		-55	150	°C
T _j	junction temperature		-55	150	°C
T _{slid(M)}	peak soldering temperature		-	260	°C

[1] Limited by device saturation

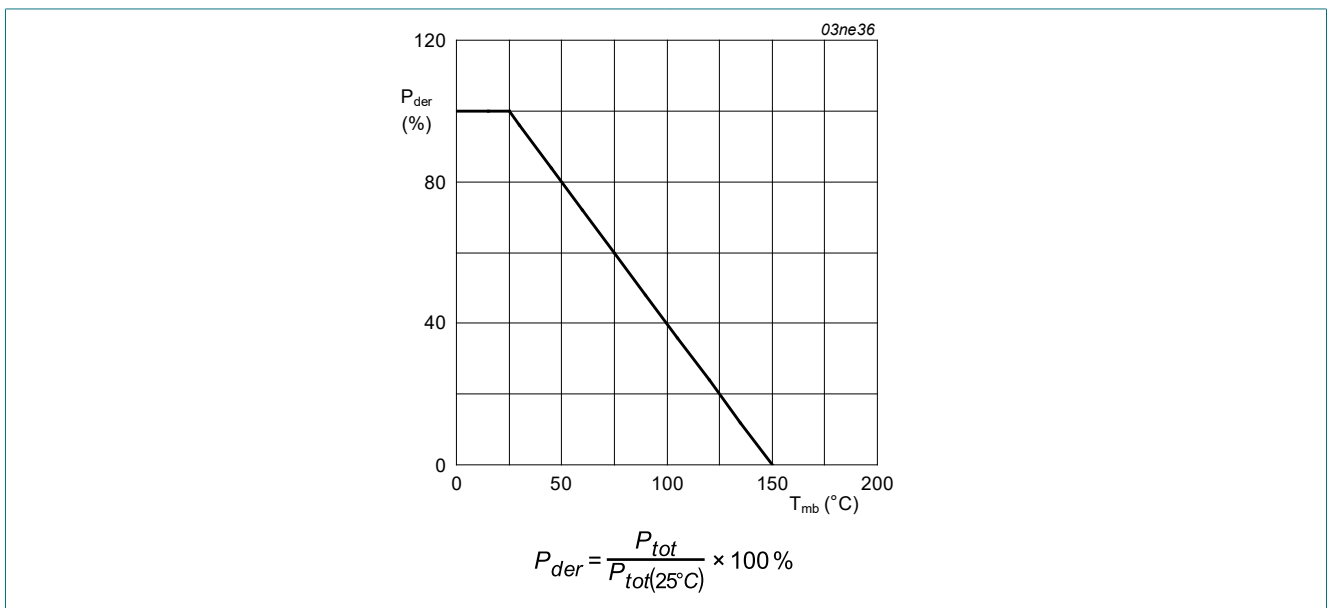


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

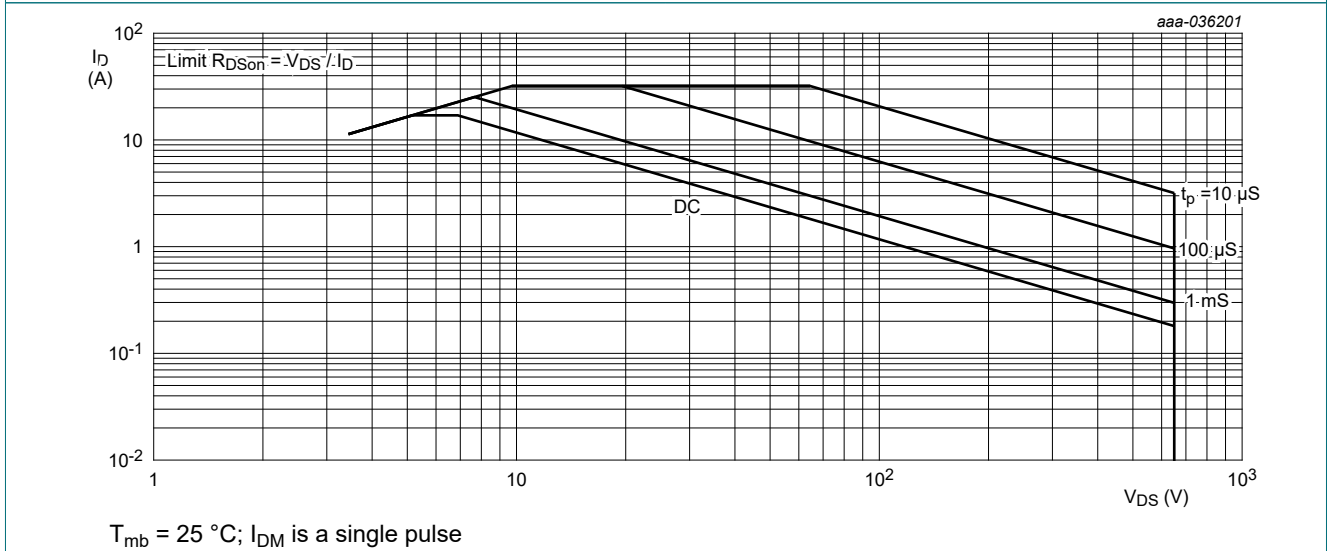


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	Fig. 3	-	-	1.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	-	60.3	K/W

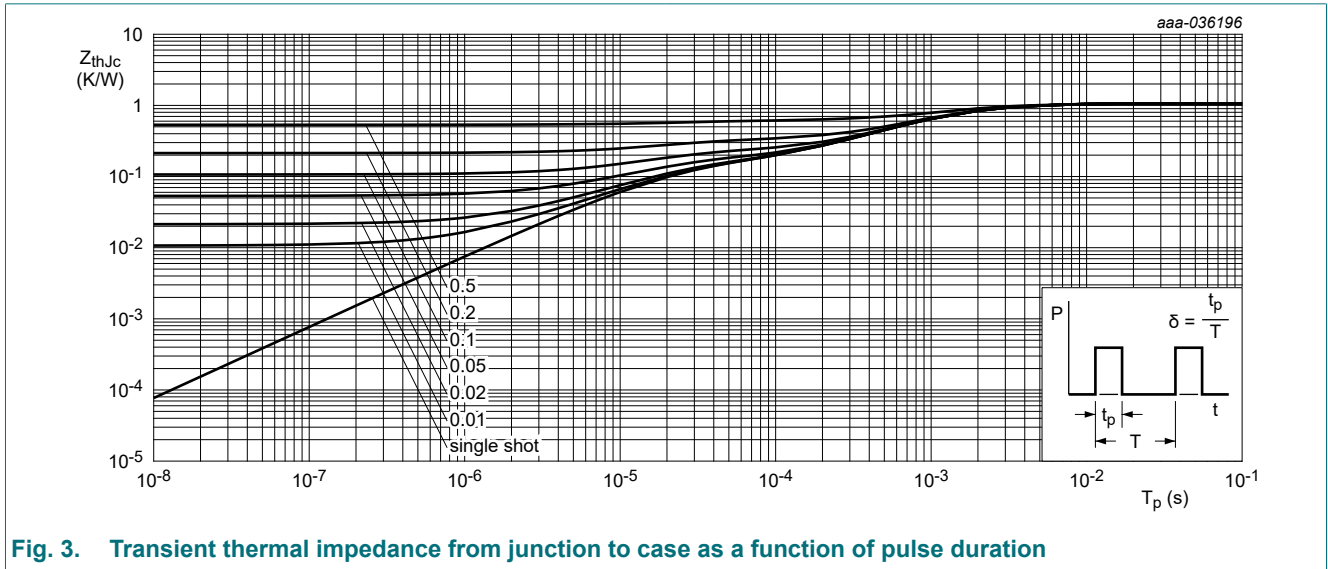


Fig. 3. Transient thermal impedance from junction to case as a function of pulse duration

10. Characteristics

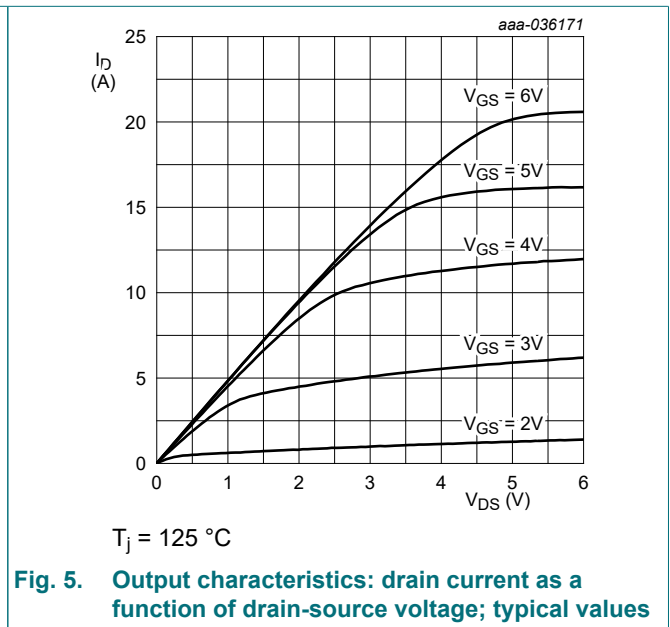
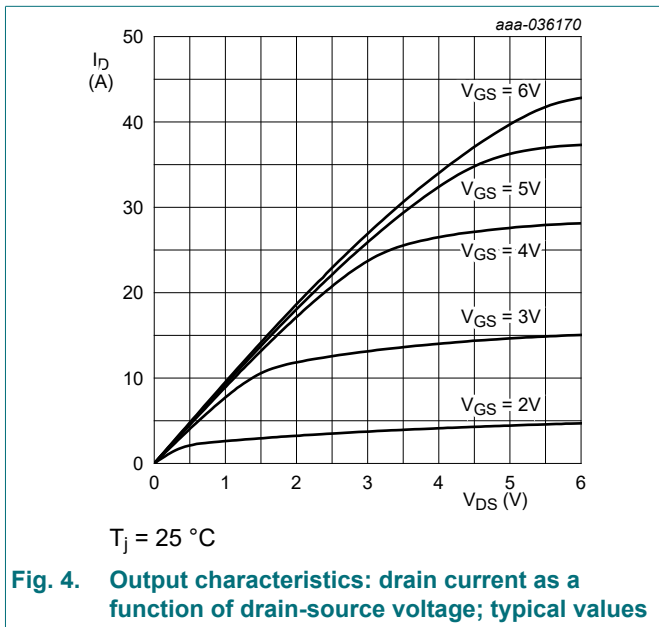
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 17.2 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 8	1.2	1.7	2.5	V
		$I_D = 17.2 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 8	-	1.7	-	V
I_{DSS}	drain leakage current	$V_{DS} = 650 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 9	-	0.6	25	μA
		$V_{DS} = 650 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 9	-	7	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 6 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 10	-	70	-	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 6 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 11; Fig. 12; Fig. 13	-	106	140	m Ω
		$V_{GS} = 6 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 11; Fig. 14	-	230	-	m Ω
R_G	gate resistance	$f = 5 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ open drain	-	3.5	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 400 \text{ V}; V_{GS} = 6 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 15; Fig. 16	-	3.5	-	nC
Q_{GS}	gate-source charge		-	0.3	-	nC
Q_{GD}	gate-drain charge		-	1.2	-	nC

650 V, 140 mOhm Gallium Nitride (GaN) FET in a DFN 5 mm x 6 mm package

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 5\text{ A}$; $V_{DS} = 400\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 15	-	2.1	-	V
C_{iss}	input capacitance	$V_{DS} = 400\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 100\text{ kHz}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 17	-	125	-	pF
C_{oss}	output capacitance		-	41	-	pF
C_{rss}	reverse transfer capacitance		-	0.4	-	pF
$C_{o(er)}$	effective output capacitance, energy related	$0\text{ V} \leq V_{DS} \leq 400\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 18	[1]	-	59	pF
$C_{o(tr)}$	effective output capacitance, time related	$0\text{ V} \leq V_{DS} \leq 400\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	[2]	-	82	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 400\text{ V}$; $V_{GS} = 6\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; $I_D = 10\text{ A}$; $L = 318\text{ }\mu\text{H}$; $R_{on} = 10\text{ }\Omega$; $R_{off} = 2\text{ }\Omega$; Fig. 19 ; Fig. 20	-	3	-	ns
t_r	rise time		-	5	-	ns
$t_{d(off)}$	turn-off delay time		-	4	-	ns
t_f	fall time		-	4	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	[3]	-	33	nC
Source-drain characteristics						
V_{SD}	source-drain voltage	$I_S = 5\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 21 ; Fig. 22 ; Fig. 23 ; Fig. 24	-	2.4	-	V

- [1] $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V
- [2] $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V
- [3] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and $Q_D = 0$. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)



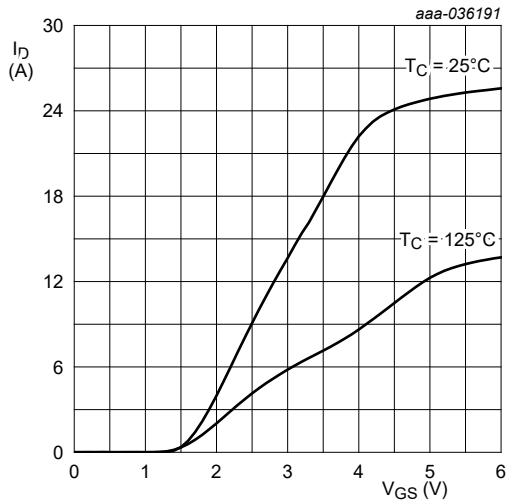


Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values

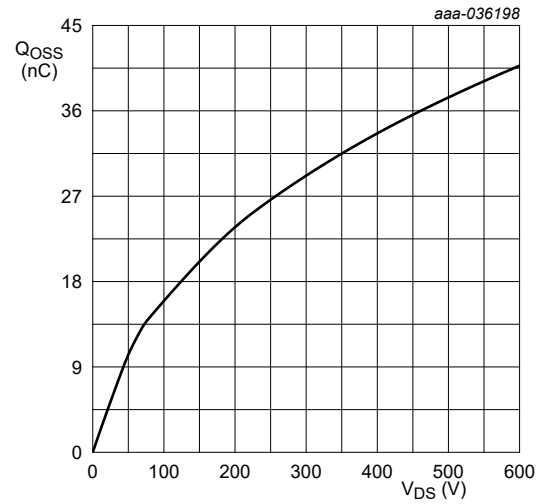


Fig. 7. Output charge as a function of drain-source voltage; typical values
Freq. = 100 kHz

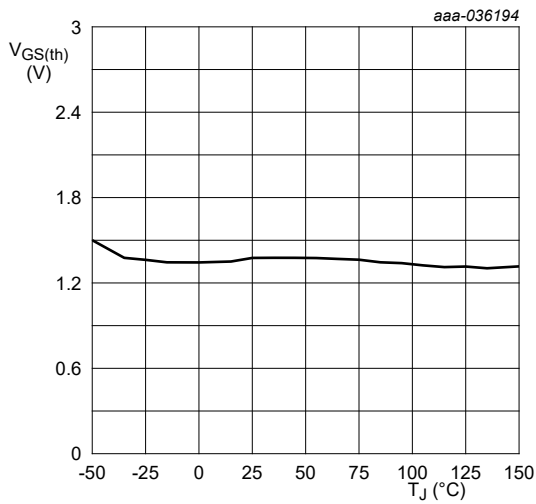


Fig. 8. Gate-source threshold voltage as a function of junction temperature
 $I_D = 17.2 \text{ mA}$; $V_{DS} = V_{GS}$

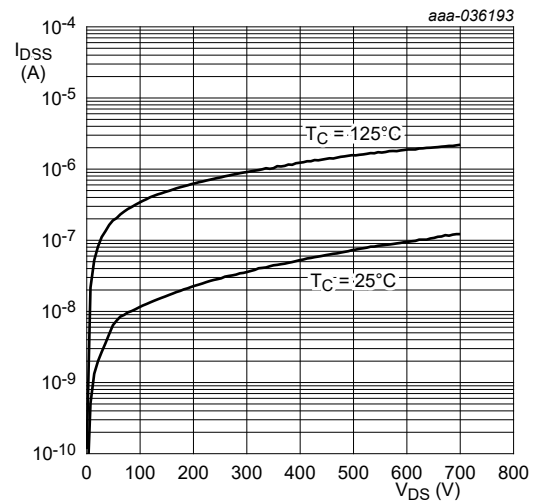
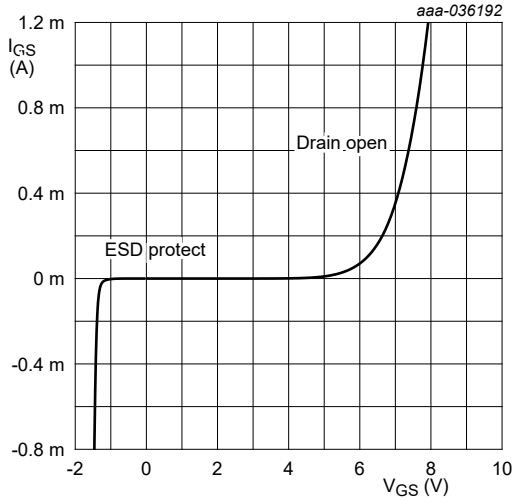
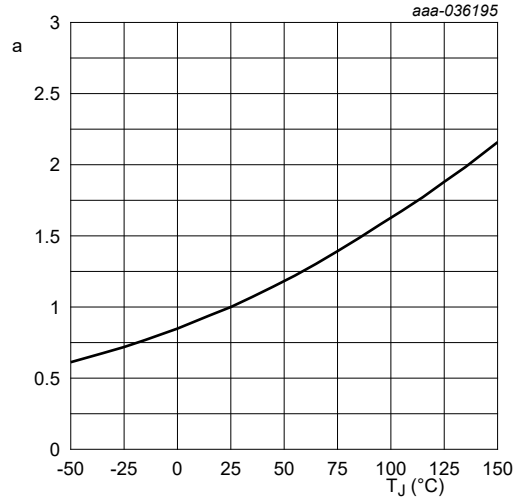


Fig. 9. Drain-source current as a function of drain-source voltage; typical values
 $V_{GS} = 0 \text{ V}$



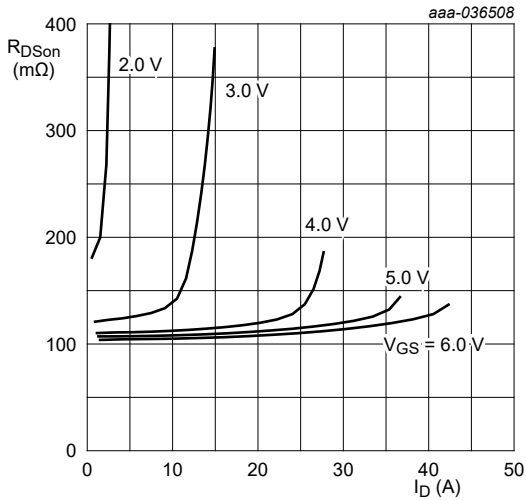
I_g reverse turn on by ESD unit

Fig. 10. Gate-source current as a function of gate-source voltage; typical values



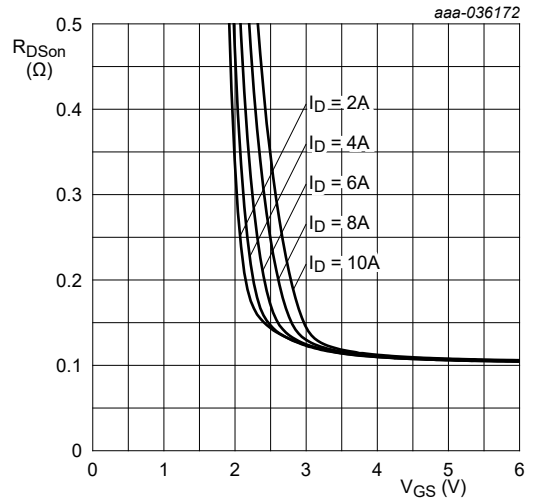
$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C

Fig. 12. Drain-source on-state resistance as a function of drain current ; typical values



T_j = 25 °C

Fig. 13. Drain-source on-state resistance as a function of gate-source voltage; typical values

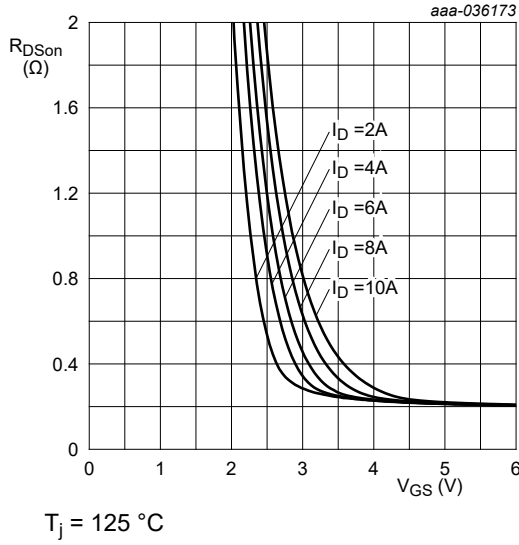


Fig. 14. Drain-source on-state resistance as a function of gate-source voltage; typical values

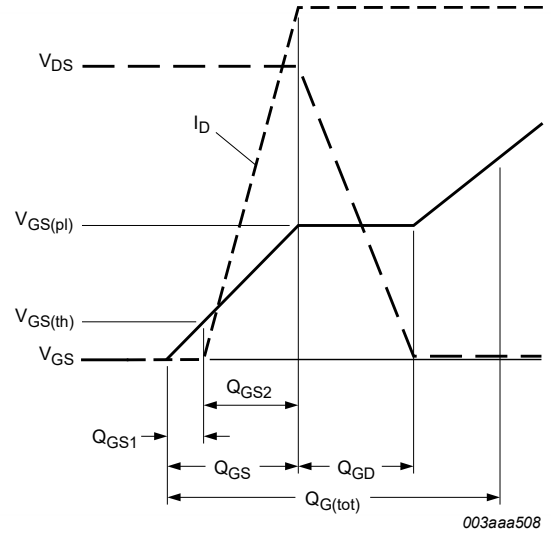


Fig. 15. Gate charge waveform definitions

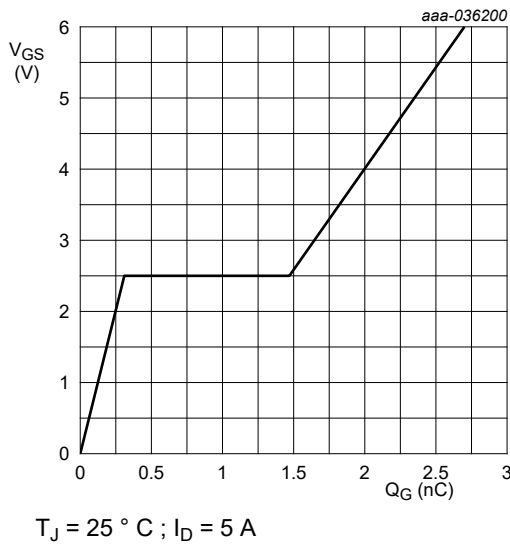


Fig. 16. Gate-source voltage as a function of gate charge; typical values

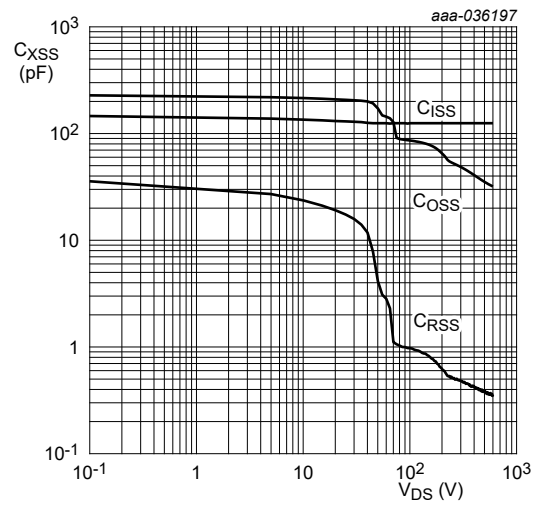
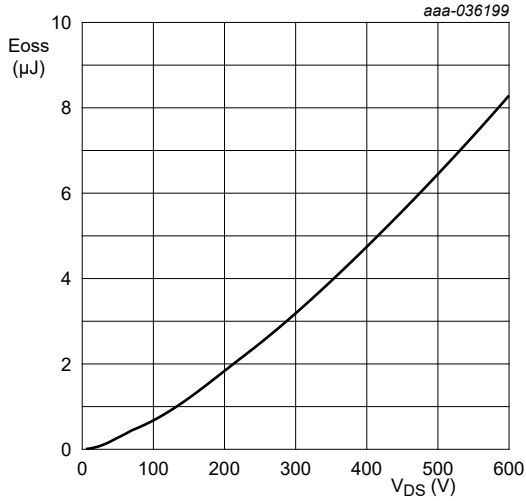
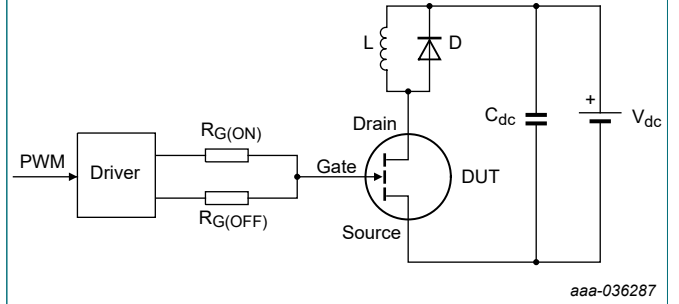


Fig. 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



Freq. = 100 kHz

Fig. 18. COSS stored energy as a function of drain-source voltage; typical values



$V_{DS} = 400 V$; $I_D = 10 A$; $L = 318 \mu H$; $V_{GS} = 6 V$;
 $R_{on} = 10 \Omega$; $R_{off} = 2 \Omega$

Fig. 19. Typical switching times with inductive load

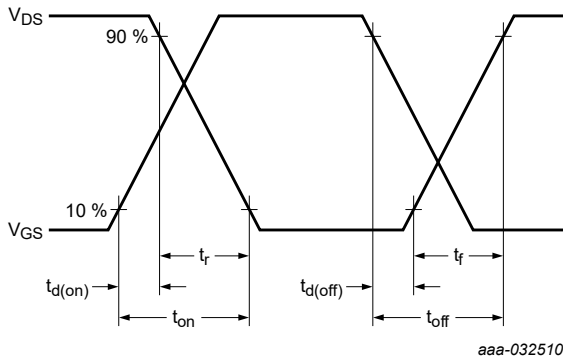
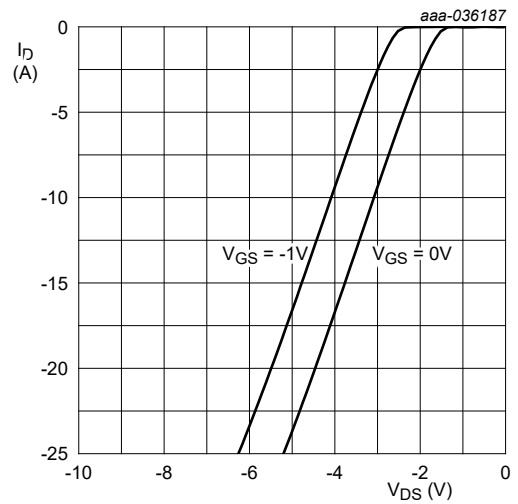
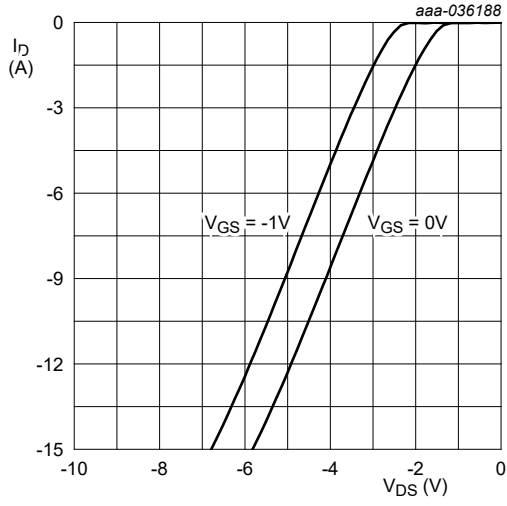


Fig. 20. Switching time waveform



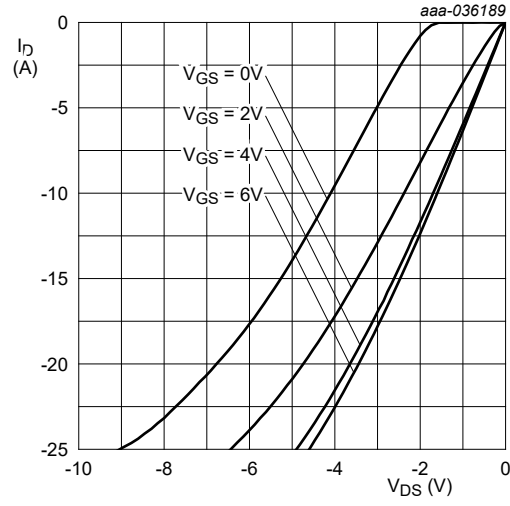
$T_j = 25 \text{ }^\circ C$

Fig. 21. Source current as a function of source-drain voltage; typical values



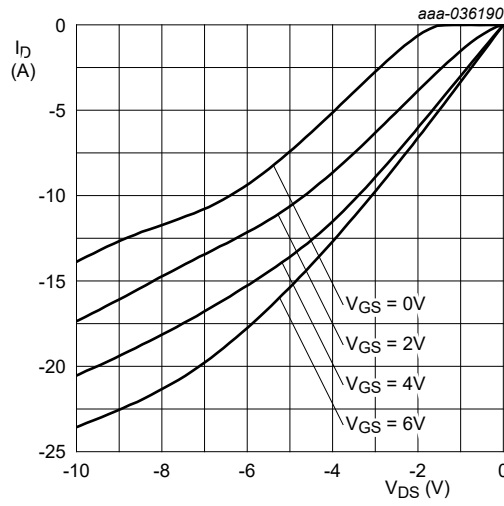
$T_j = 125\text{ °C}$

Fig. 22. Source current as a function of source-drain voltage; typical values



$T_j = 25\text{ °C}$

Fig. 23. Source current as a function of source-drain voltage; typical values



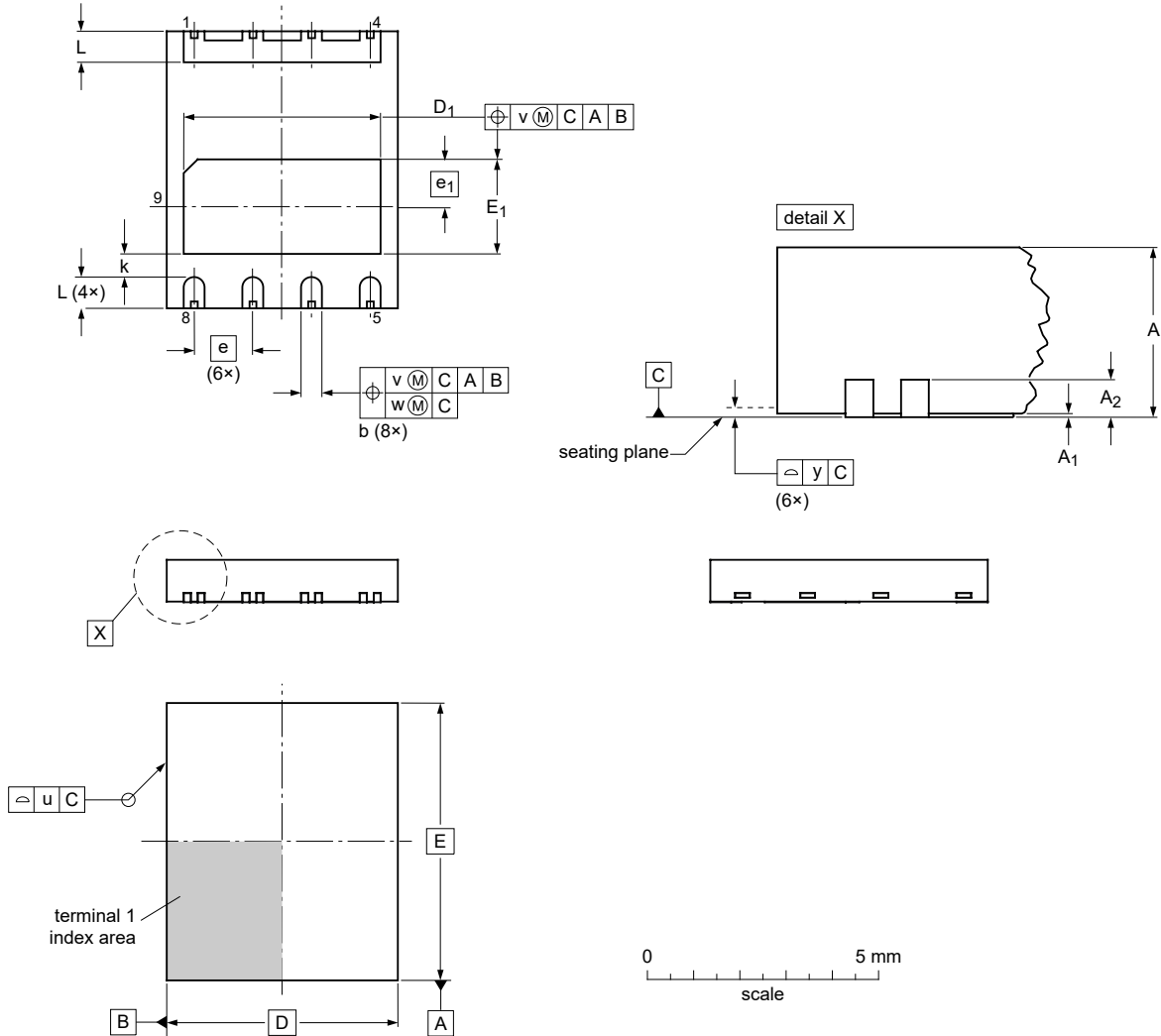
$T_j = 125\text{ °C}$

Fig. 24. Source current as a function of source-drain voltage; typical values

11. Package outline

DFN5060-5: plastic thermal enhanced small outline package; no leads; 5 terminals; body: 5 × 6 × 0.9 mm

SOT8075-1



Dimensions (mm are the original dimensions)

Unit	A	A ₁	A ₂	b	D	D ₁	E	E ₁	e	e ₁	k	L	u	v	w	y
max	1.0	0.05	0.203	0.50	5	4.36	6	2.15	1.27	0.8	0.5	0.775				
nom	0.9	0.02	REF	0.45	BSC	4.26	BSC	2.05	BSC	BSC	REF	0.675	0.1	0.1	0.05	0.1
min	0.8	0.00		0.40		4.16		1.95				0.575				

sot8075-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT8075-1		MO-229 compatible			23-03-03

Fig. 25. Package outline DFN5060-5 (SOT8075-1)

12. Soldering

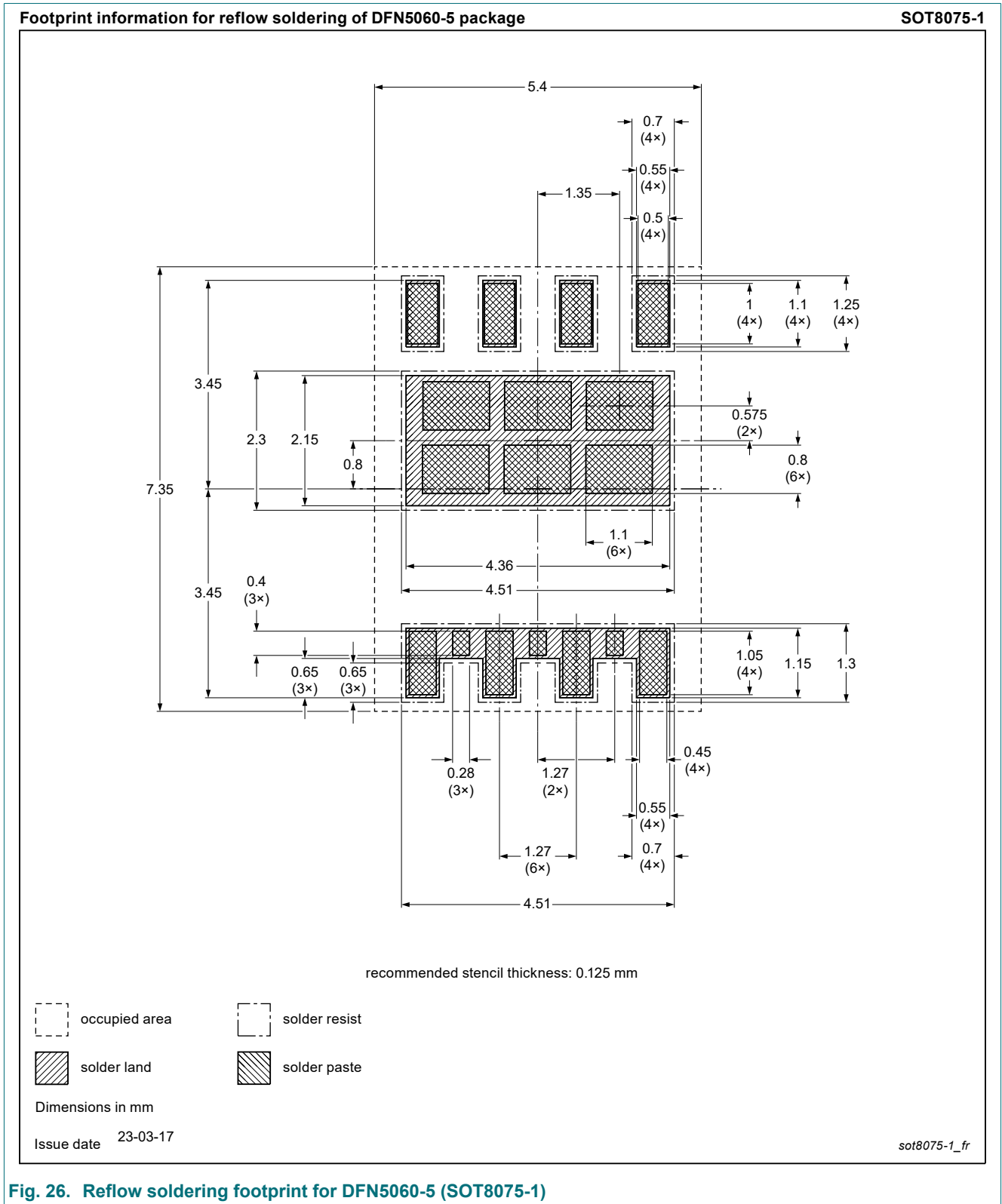


Fig. 26. Reflow soldering footprint for DFN5060-5 (SOT8075-1)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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