STANDARD MICROSYSTEMS CORPORATION

COM 5025
μPC FAMILY

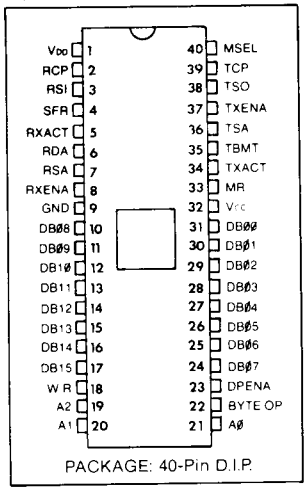
SECTION III

Multi-Protocol Universal Synchronous Receiver/Transmitter
USYNR/T

FEATURES

- ☐ Selectable Protocol—Bit or Byte oriented
- ☐ Direct TTL Compatibility
- ☐ Three-state Input/Output BUS
- ☐ Processor Compatible—8 or 16 bit
- ☐ High Speed Operation—1.5 M Baud—typical
- ☐ Fully Double Buffered—Data, Status, and Control Registers
- ☐ Full or Half Duplex Operation—independent Transmitter and Receiver Clocks
  —individually selectable data length for Receiver and Transmitter
- ☐ Master Reset—resets all Data, Status, and Control Registers
- ☐ Maintenance Select—built-in self checking

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

BIT ORIENTED PROTOCOLS—SDLC, HDLC, ADCCP
- ☐ Automatic bit stuffing and stripping
- ☐ Automatic frame character detection and generation
- ☐ Valid message protection—a valid received message is protected from overrun
- ☐ Residue Handling—for messages which terminate with a partial data byte, the number of valid data bits is available

SELECTABLE OPTIONS:
- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —None
- ☐ Primary or Secondary Station Address Mode
- ☐ All Parties Address—APA
- ☐ Extendable Address Field—to any number of bytes
- ☐ Extendable Control Field—to 2 bytes
- ☐ Idle Mode—idle FLAG characters or MARK the line
- ☐ Point to Point, Multi-drop, or Loop Configuration

BYTE ORIENTED PROTOCOLS—BiSync, DDCMP
- ☐ Automatic detection and generation of SYNC characters

SELECTABLE OPTIONS:
- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Variable SYNC character—5, 6, 7, or 8 bits
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —VRC (odd/even parity)
  —None
- ☐ Strip Sync—deletion of leading SYNC characters after synchronization
- ☐ Idle Mode—idle SYNC characters or MARK the line

APPLICATIONS

- ☐ Intelligent Terminals
- ☐ Line Controllers
- ☐ Network Processors
- ☐ Front End Communications
- ☐ Remote Data Concentractors
- ☐ Communication Test Equipment
- ☐ Computer to Computer Links
- ☐ Hard Disk Data Handler

General Description

The COM 5025 is a COPLAMOS® n channel silicon gate MOS/LSI device that meets the majority of synchronous communications requirements, by interfacing parallel digital systems to synchronous serial data communication channels while requiring a minimum of controller overhead.

The COM 5025 is well suited for applications such as computer to modem interfaces, computer to computer serial links and in terminal applications. Since higher level decisions and responses are made or initiated by the controller, some degree of intelligence in each controller of the device is necessary.

Newly emerging protocols such as SDLC, HDLC, and ADCCP will be able to utilize the COM 5025 with a high degree of efficiency as zero insertion for transmission and zero deletion for reception are done automatically. These protocols will be referred to as Bit Oriented Protocols (BOP). Any differences between them will be discussed in their respective sections. Conventional synchronous protocols that are control character oriented such as BISYNC can also utilize this device. Control Character oriented protocols will be referred to as CCP protocols. Other types of protocols that operate on a byte or character count basis can also utilize the COM 5025 with a high degree of efficiency in most cases. These protocols, such as DDCMP will also be referred to as CCP protocols.

The COM 5025 is designed to operate in a synchronous communications system where some external source is expected to provide the necessary received serial data, and all clock signals properly synchronized according to EIA standard RS334. The external controller of the chip will provide the necessary control signals, intelligence in interpreting control signals from the device and data to be transmitted in accord with RS334.

The receiver and transmitter are as symmetrical as possible without loss of efficiency. The controller of the device will be responsible for all higher level decisions and interpretation of some fields within message frames. The degree to which this occurs is dependent on the protocol being implemented. The receiver and transmitter logic operate as two totally independent sections with a minimum of common logic.

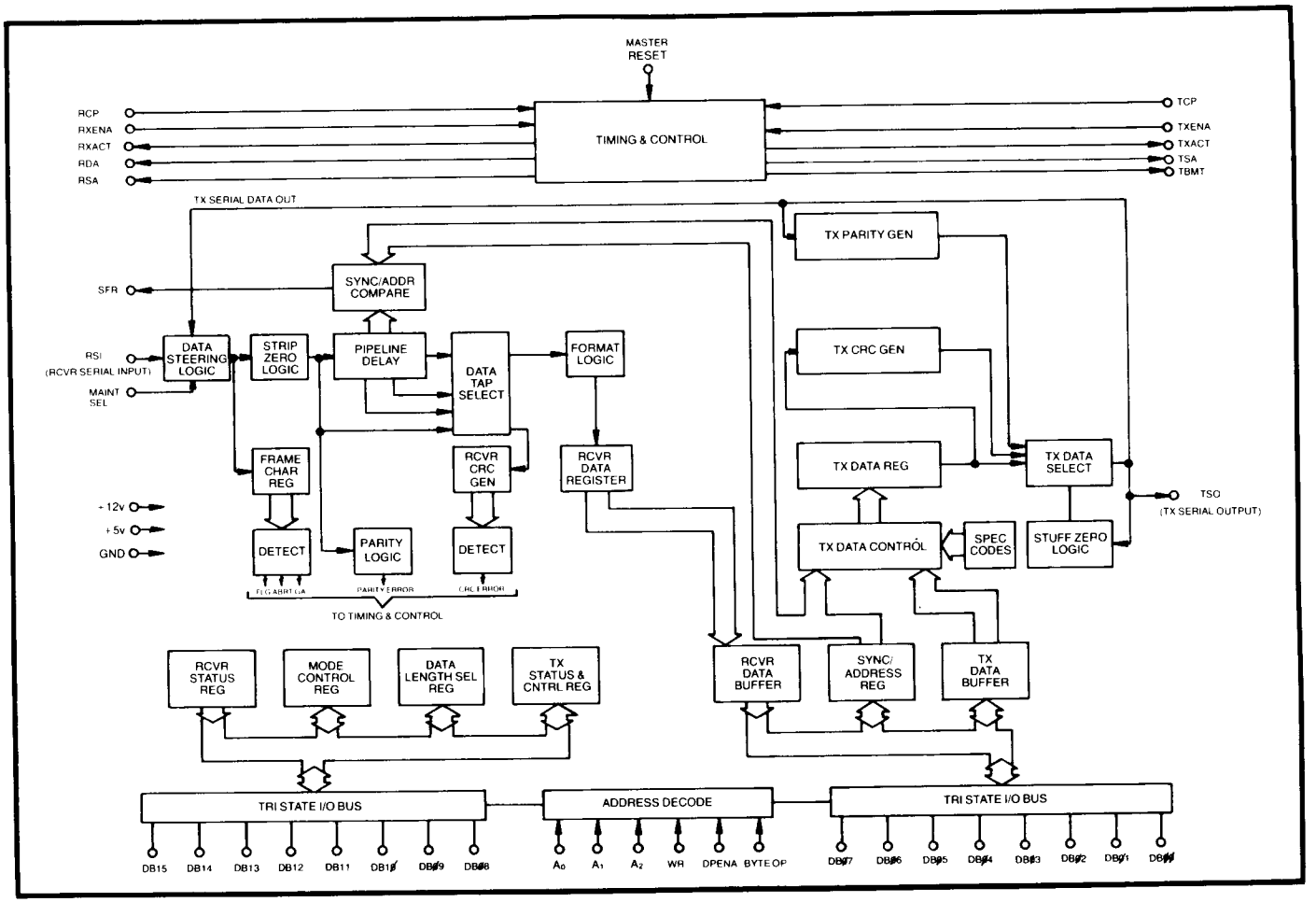
References:

1. ANSI—American National Standards Institute
   X353, XS34/589
   202-466-2299
2. CCITT—Consultative Committee for International Telephone and Telegraph
   X.25
   202-632-1007
3. EIA—Electronic Industries Association
   TR30, RS334
   202-659-2200
4. IBM
   General Information Brochure, GA27-3093
   Loop Interface—OEM Information, GA27-3098
   System Journal—Vol. 15, No. 1, 1976; G321-0044

Terminology

Term	Definition	Term	Definition
BOP	Bit Oriented Protocols: SDLC, HDLC, ADCCP	GA	01111111 (0 (LSB) followed by 7-1's)
CCP	Control Character Protocols: BiSync, DDCMP	LSB	First transmitted bit, First received bit
TDB	Transmitter Data Buffer	MSB	Last transmitted bit, Last received bit
RDB	Receiver Data Buffer	RDP	Receiver Data Path
TDSR	Transmitter Data Shift Register	TDP	Transmitter Data Path
FLAG	01111110	LM	Loop Mode
ABORT	11111111 (7 or more contiguous 1's)		

BLOCK DIAGRAM



Description of Pin Functions

Pin No.	Symbol	Name	I/O	Function
1	V_{DD}	Power Supply	PS	+12 volt Power Supply.
2	RCP	Receiver Clock	I	The positive-going edge of this clock shifts data into the receiver shift register.
3	RSI	Receiver Serial Input	I	This input accepts the serial bit input stream.
4	SFR	Sync/Flag Received	O	This output is set high, for 1 clock time of the RCP, each time a sync or flag character is received.
5	RXACT	Receiver Active	O	This output is asserted when the RDP presents the first data character of the message to the controller. In the BOP mode the first data character is the first non-flag character (address byte). In the CCP mode: 1. if strip-sync is set; the first non-sync character is the first data character 2. if strip-sync is not set; the first data character is the character following the second sync. In the BOP mode the trailing (next) FLAG resets RXACT. In the CCP mode RXACT is never reset, it can be cleared via RXENA.
6	RDA	Receiver Data Available	O	This output is set high when the RDP has assembled an entire character and transferred it into the RDB. This output is reset by reading the RDB.
7	RSA	Receiver Status Available	O	This output is set high: 1. CCP—in the event of receiver over run (ROR) or parity error (if selected), 2. BOP—in the event of ROR, CRC error (if selected) receiving REOM or RAB/GA. This output is reset by reading the receiver status register or dropping of RXENA.
8	RXENA	Receiver Enable	I	A high level input allows the processing of RSI data. A low level disables the RDP and resets RDA, RSA and RXACT.
9	GND	Ground	GND	Ground
10	DBØ8	Data Bus	I/O	Bidirectional Data Bus.
11	DBØ9	Data Bus	I/O	Bidirectional Data Bus.
12	DB1Ø	Data Bus	I/O	Bidirectional Data Bus.
13	DB11	Data Bus	I/O	Bidirectional Data Bus.
14	DB12	Data Bus	I/O	Bidirectional Data Bus.
15	DB13	Data Bus	I/O	Bidirectional Data Bus.
16	DB14	Data Bus	I/O	Bidirectional Data Bus.
17	DB15	Data Bus	I/O	Bidirectional Data Bus.
				Wire "OR" with DBØØ-DBØ7 For 8 bit data bus
18	W/R	Write/Read	I	Controls direction of data port. W/R = 1, Write. W/R = 0, Read.
19	A2	Address 2	I	Address input—MSB.
20	A1	Address 1	I	Address input.
21	AØ	Address 0	I	Address input—LSB.
22	BYTE OP	Byte Operation	I	If asserted, byte operation (data port is 8 bits wide) is selected. If BYTE OP = 0, data port is 16 bits wide.
23	DPENA	Data Port Enable	I	Strobe for data port. After address, byte op, W/R and data are set-up DPENA may be strobed. If reading the port, DPENA may reset (depending on register selected by address) RDA or RSA. If writing into the port, DPENA may reset (depending on register selected by address) TBMT.
24	DBØ7	Data Bus	I/O	Bidirectional Data Bus—MSB.
25	DBØ6	Data Bus	I/O	Bidirectional Data Bus.
26	DBØ5	Data Bus	I/O	Bidirectional Data Bus.
27	DBØ4	Data Bus	I/O	Bidirectional Data Bus.
28	DBØ3	Data Bus	I/O	Bidirectional Data Bus.
29	DBØ2	Data Bus	I/O	Bidirectional Data Bus.
30	DBØ1	Data Bus	I/O	Bidirectional Data Bus.
31	DBØØ	Data Bus	I/O	Bidirectional Data Bus—LSB.
32	V_{CC}	Power Supply	PS	+5 volt Power Supply.
33	MR	Master Reset	I	This input should be pulsed high after power turn on. This will: clear all flags, and status conditions, set TBMT = 1, TSO = 1 and place the device in the primary BOP mode with 8 bit TX/RX data length, CRC CCITT initialized to all 1's.
34	TXACT	Transmitter Active	O	This output indicates the status of the TDP. TXACT will go high after asserting TXENA and TSOM coinsidently with the first TSO bit. This output will reset one half clock after the byte during which TXENA is dropped.
35	TBMT	Transmitter Buffer Empty	O	This output is at a high level when the TDB or the TX Status and Control Register may be loaded with the new data. TBMT = 0 on any write access to TDB or TX Status and Control Register. TBMT returns high when the TDSR is loaded.
36	TSA	Transmitter Status Available	O	TERR bit, indicating transmitter underflow. Reset by MR or assertion of TSOM.
37	TXENA	Transmitter Enable	I	A high level input allows the processing of transmitter data.
38	TSO	Transmitter Serial Output	O	This output is the transmitted character.
39	TCP	Transmitter Clock	I	The positive going edge of this clock shifts data out of the transmitter shift register.
40	MSEL	Maintenance Select	I	Internally RSI becomes TSO and RCP becomes $\overline{TCP}$. Externally RSI is disabled and TSO = 1.

Definition of Terms
Register Bit Assignment Chart 1 and 2

Receiver Status Register

Data Bu	Term	Definition
DBØ8	RSOM	Receiver Start of Message—read only bit. In BOP mode only, goes high when first non-flag (address byte) character loaded into RDB. It is cleared when the second byte is loaded into the RDB.
DBØ9	REOM	Receiver End of Message—read only bit. In BOP mode only, set high when last byte of data loaded into RDB, or when an ABORT character is received. It is cleared on reading of Receiver Status Register or dropping of RXENA.
DB1Ø	RAB/GA	Received ABORT or GO AHEAD character, read only bit. In BOP mode only, if LM=0 this bit is set on receiving an ABORT character; if LM=1 this bit is set on receiving a GO AHEAD character. This is cleared on reading of Receiver Status Register or dropping of RXENA.
DB11	ROR	Receiver Over Run—read only bit. Set high when received data transferred into RDB and previous data has not been read, indicating failure to service RDA within one character time. Cleared on reading of Receiver Status Register or dropping of RXENA.
DB12-14	A,B,C	Assembled Bit Count—read only bits. In BOP mode only, examine when REOM=1. ABC=0, message terminated on stated boundary. ABC=XXX, message terminated (by FLAG or GA) on unstated boundary, binary value of ABC = number of valid bits available in RDB (right hand justified).
DB15	ERR CHK	Error Check—read only bit. In BOP set high if CRC selected and received in error, examine when REOM=1. In CCP mode: 1. set high if parity selected and received in error, 2. if CRC selected (tested at end of each byte) ERR CHK = 1 if CRC GOOD, ERR CHK = 0 if CRC NOT GOOD. Controller must determine the last byte of the message.

Transmitter Status and Control Register

DB8	TSOM	Transmitter Start of Message—W/R bit. Provided TXENA=1, TSOM initiates start of message. In BOP, TSOM=1 generates FLAG and continues to send FLAG's until TSOM=0, then begin data. In CCP: 1. IDLE=0, transmit out of SYNC register, continue until TSOM=0, then begin data. 2. IDLE=1 transmit out of TDB. In BOP mode there is also a Special Space Sequence of 16-0's initiated by TSOM=1 and TEOM=1. SSS is followed by FLAG.
DB9	TEOM	Transmit End of Message—W/R bit. Used to terminate a message. In BOP mode, TEOM=1 sends CRC, then FLAG; if TXENA=1 and TEOM=1 continue to send FLAG's, if TXENA=0 and TEOM=1 MARK line. In CCP: 1. IDLE=0, TEOM=1 send SYNC, if TXENA=1 and TEOM=1 continue to send SYNC's, if TXENA=0 and TEOM=1 MARK line. 2. IDLE=1, TEOM=1, MARK line.
DB1Ø	TXAB	Transmitter Abort—W/R bit. In BOP mode only, TXAB=1 finish present character then: 1. IDLE=0, transmit ABORT 2. IDLE=1, transmit FLAG.
DB11	TXGA	Transmit Go Ahead—W/R bit. In BOP mode only, modifies character called for by TEOM. GA sent in place of FLAG. Allows loop termination—GA character.
DB15	TERR	Transmitter Error—read only bit. Underflow, set high when TDB not loaded in time to maintain continuous transmission. In BOP automatically transmit: 1. IDLE=0, ABORT 2. IDLE=1, FLAG. In CCP automatically transmit: 1. IDLE=0, SYNC 2. IDLE=1, MARK. Cleared by TSOM.

Mode Control Register

DB8-1Ø	X,Y,Z	Z Y X —W/R bits. These are the error control bits. 0 0 0 $X^{16}+X^{12}+X^5+1$ CCITT—Initialize to "1" 0 0 1 $X^{16}+X^{12}+X^5+1$ CCITT—Initialize to "0" 0 1 0 Not used 0 1 1 $X^{16}+X^{15}+X^2+1$—CRC16 1 0 0 Odd Parity—CCP Only 1 0 1 Even Parity—CCP Only 1 1 0 Not Used 1 1 1 Inhibit all error detection and transmission Note: Do not modify XYZ until both data paths are idle
DB11	IDLE	IDLE mode select—W/R bit. Affects transmitter only. In BOP—control the type of character sent when TXAB asserted or in the event of data underflow. In CCP—controls the method of initial SYNC character transmission and underflow, "1" = transmit SYNC from TDB, "0"=transmit SYNC from SYNC/ADDRESS register.
DB12	SEC ADD	Secondary Address Mode—W/R bit. In BOP mode only—after FLAG looks for address match prior to activating RDP, if no match found, begin FLAG search again. SEC ADD bit should not be set if EXADD=1 or EXCON=1.
DB13	STRIP SYNC/LOOP	Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping.
DB14	PROTOCOL	PROTOCOL—W/R bit. BOP=0, CCP=1
DB15	*APA	All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP.

Data Length Select Register

DB13-15	TXDL	Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character 1 0 0 Four bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 0 0 1 One bit per character* *For data length only, not to be used for SYNC character (CCP mode).
DB8-1Ø	RXDL	Receiver Data Length—W/R bits. RXDL3 RXDL2 RXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character 1 0 0 Four bits per character 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character
DB11	EXCON	Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD =1.
DB12	EXADD	Extended Address Field—W/R bit. In receiver only; LSB of address byte tested for a "1". If NO—continue receiving address bytes, if YES go into control field. EXADD bit should not be set if SEC ADD =1.

*Note: Product manufactured before 1Q79 may not have this feature.

Register Bit Assignment Chart 1

REGISTER	DPØ7	DPØ6	DPØ5	DPØ4	DPØ3	DPØ2	DPØ1	DPØØ
Receiver Data Buffer (Read Only- Right Justified- Unused Bits=0)	RD7 MSB	RD6	RD5	RD4	RD3	RD2	RD1	RDØ LSB
Transmitter Data Register (Read/Write- Unused Inputs=X)	TD7 MSB	TD6	TD5	TD4	TD3	TD2	TD1	TDØ LSB
Sync/Secondary Address (Read/Write- Right Justified- Unused Inputs=X)	SSA7 MSB	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSAØ LSB

Register Bit Assignment Chart 2

REGISTER	DP15	DP14	DP13	DP12	DP11	DP1Ø	DPØ9	DPØ8
Receiver Status (Read Only)	ERR CHK	C	B	A	ROR	RAB/GA	REOM	RSOM
TX Status and Control (Read/Write)	TERR (Read Only)	0	0	0	TXGA	TXAB	TEOM	TSOM
Mode Control (Read/Write)	*APA	PROTOCOL	STRIP SYNC/ LOOP	SEC ADD	IDLE	Z	Y	X
Data Length Select (Read/Write)	TXDL3	TXDL2	TXDL1	EXADD	EXCON	RXDL3	RXDL2	RXDL1

* Note: Product manufactured before 1Q79 may not have this feature.

Register Address Selection

1) BYTE OP = 0, data port 16 bits wide

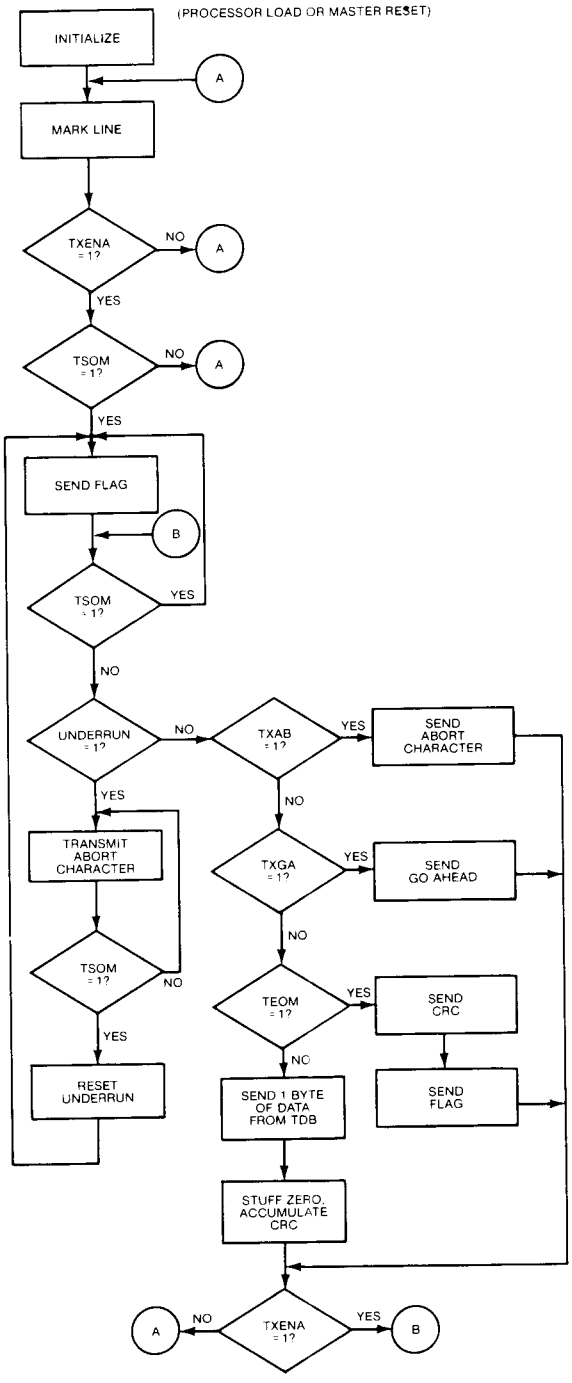
A2	A1	AØ	Register
0	0	X	Receiver Status Register and Receiver Data Buffer
0	1	X	Transmitter Status and Control Register and Transmitter Data Buffer
1	0	X	Mode Control Register and SYNC/Address Register
1	1	X	Data Length Select Register

X = don't care

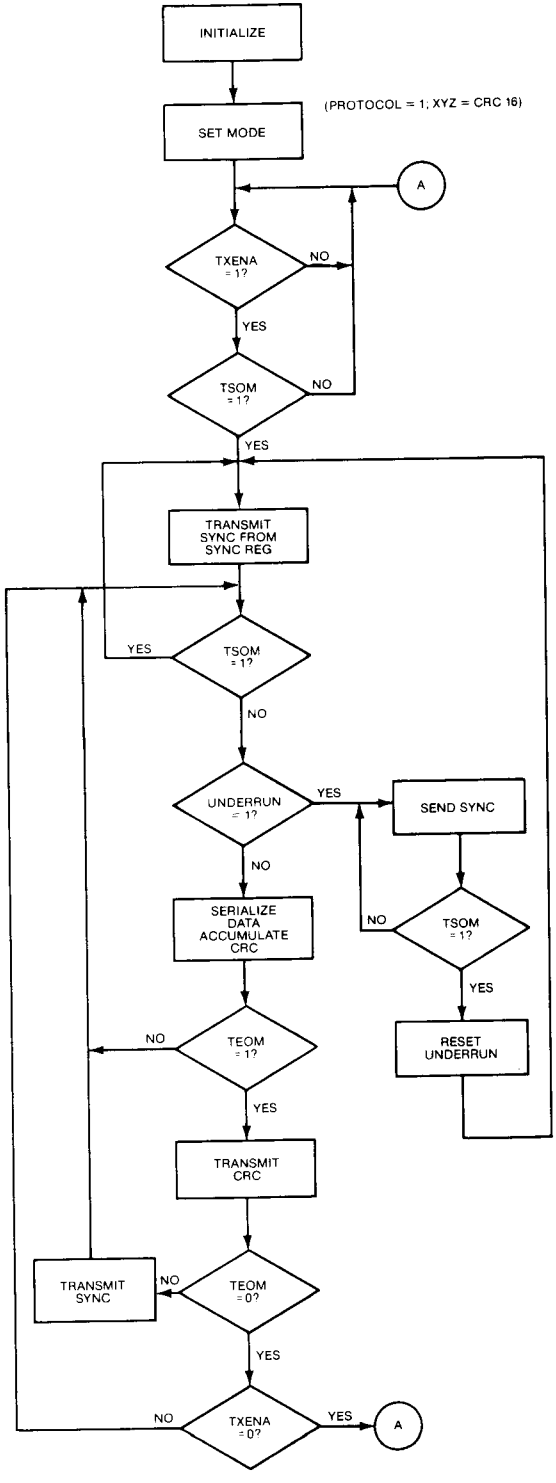
2) BYTE OP = 1, data port 8 bits wide

A2	A1	AØ	Register
0	0	0	Receiver Data Buffer
0	0	1	Receiver Status Register
0	1	0	Transmitter Data Buffer
0	1	1	Transmitter Status and Control Register
1	0	0	SYNC/Address Register
1	0	1	Mode Control Register
1	1	0	———————
1	1	1	Data Length Select Register

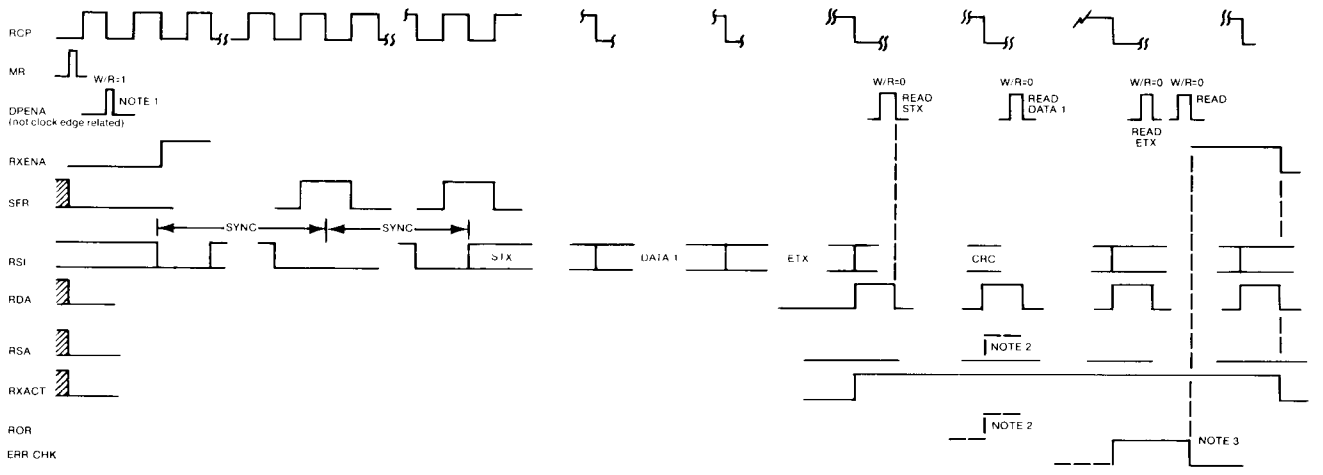
BOP TRANSMITTER OPERATION



CCP TRANSMITTER OPERATION

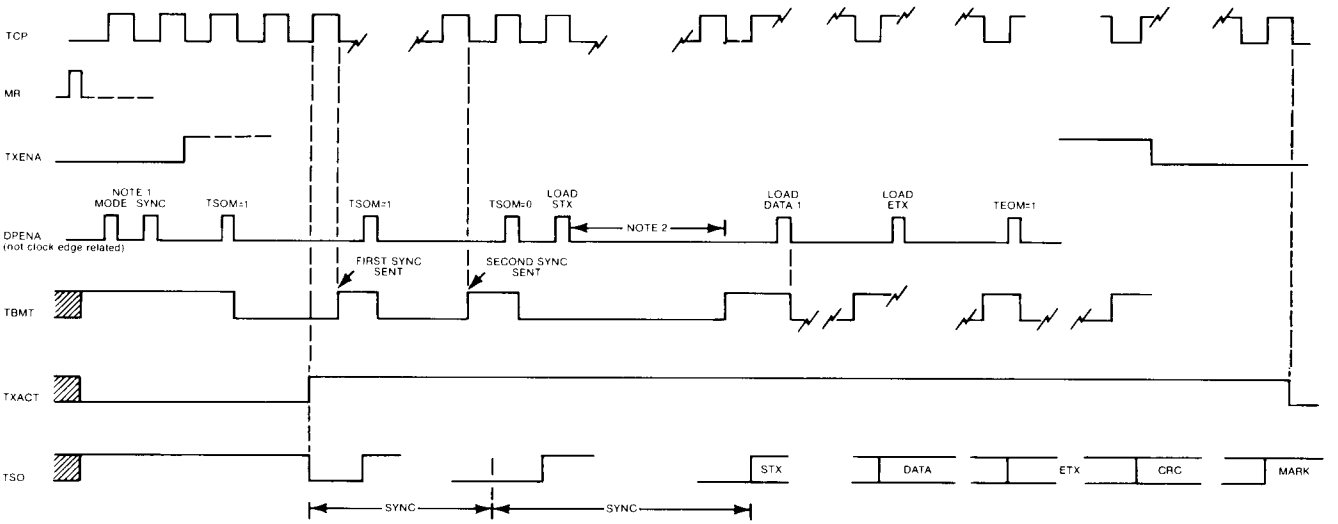


CCP RECEIVER TIMING



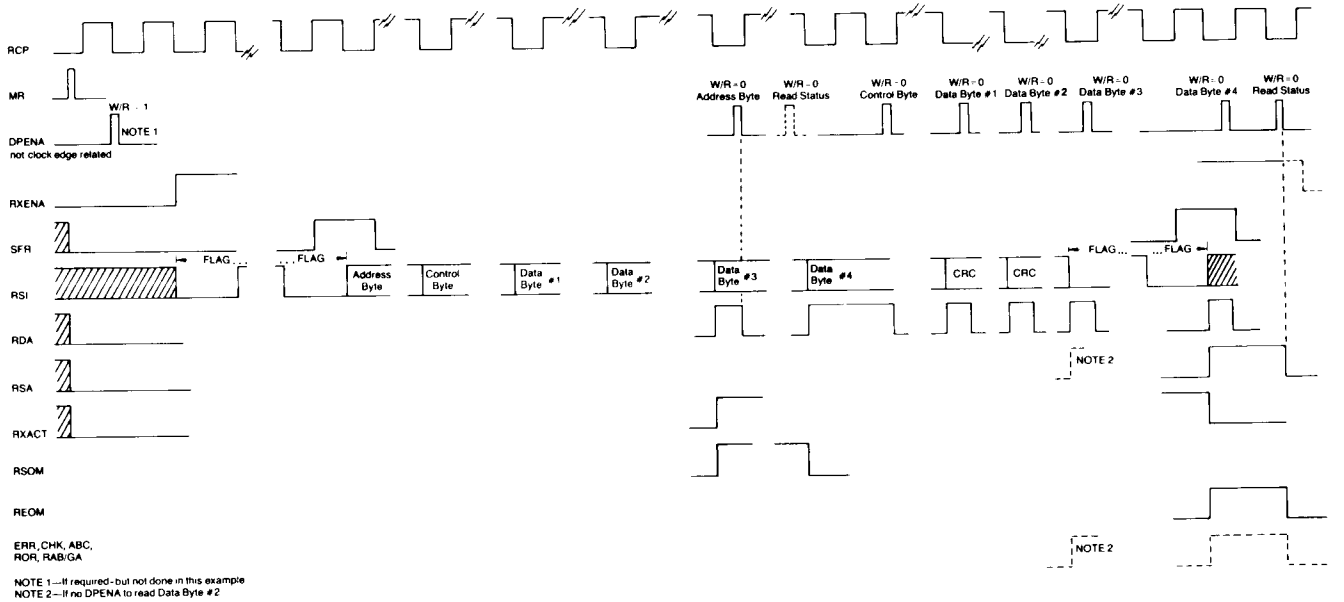
NOTE 1—Mode set for CCP with CRC selected
NOTE 2—If overrun had occured – no READ STX
NOTE 3—ERR CHK must be sampled before next byte or before RXENA brought low

CCP TRANSMITTER OPERATION



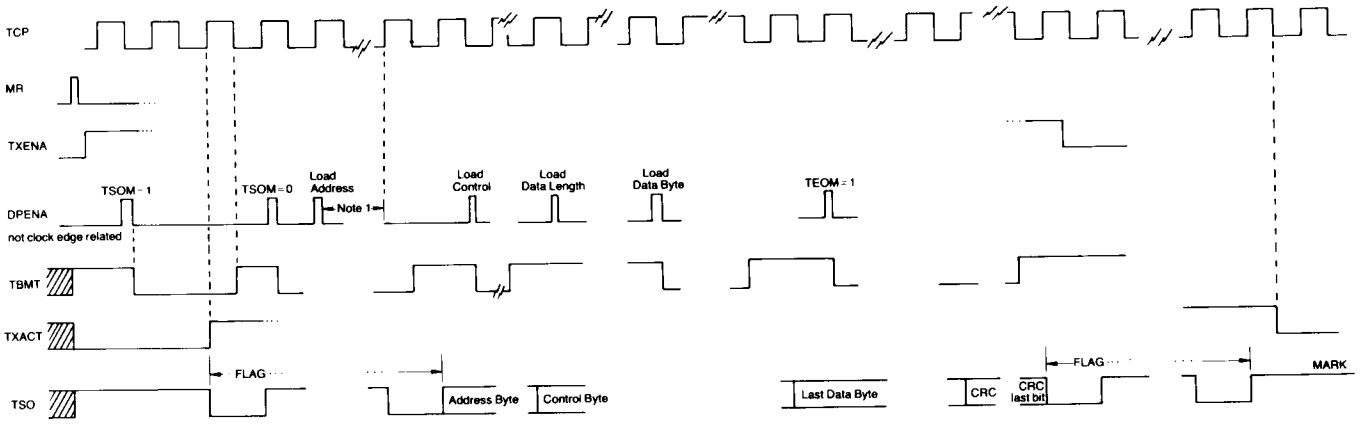
NOTE 1—Mode is CCP with CRC selected
NOTE 2 - Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT=1 to avoid underrun

BOP RECEIVER TIMING



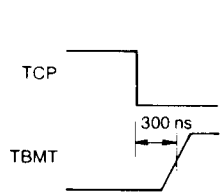
NOTE 1—If required - but not done in this example
NOTE 2—If no DPENA to read Data Byte #2

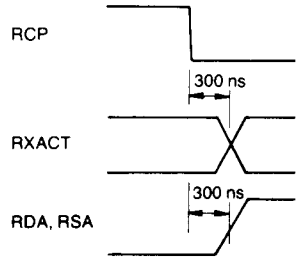
BOP TRANSMITTER OPERATION

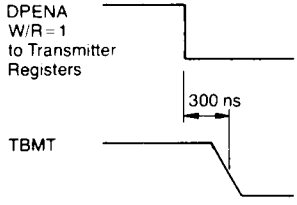


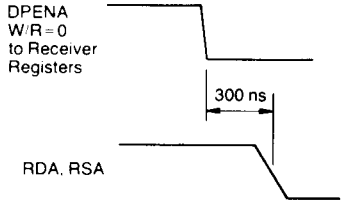
Note 1—Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT = 1. To avoid underrun.

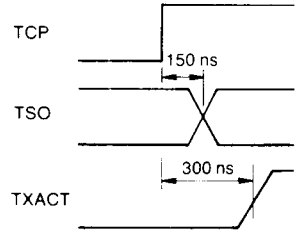
AC TIMING DIAGRAMS

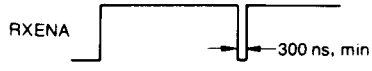








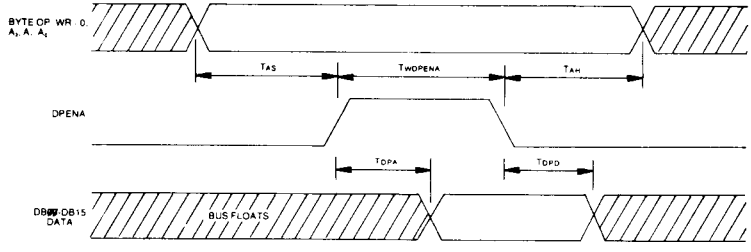




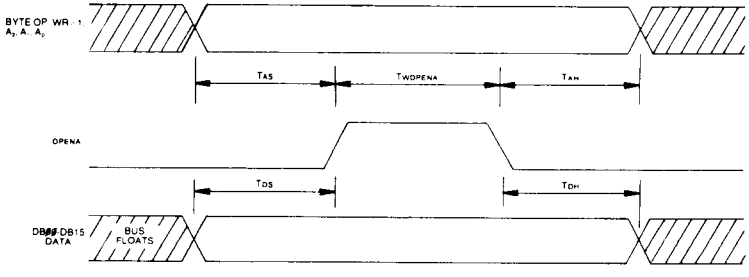
Resets: RDP-RDA, RSA, RXACT, receiver into search mode (for FLAG)

Note: Unless otherwise specified all times are maximum.

Data Port Timing



READ FROM USYNR/T



WRITE TO USYNR/T

MAXIMUM GUARANTEED RATINGS*

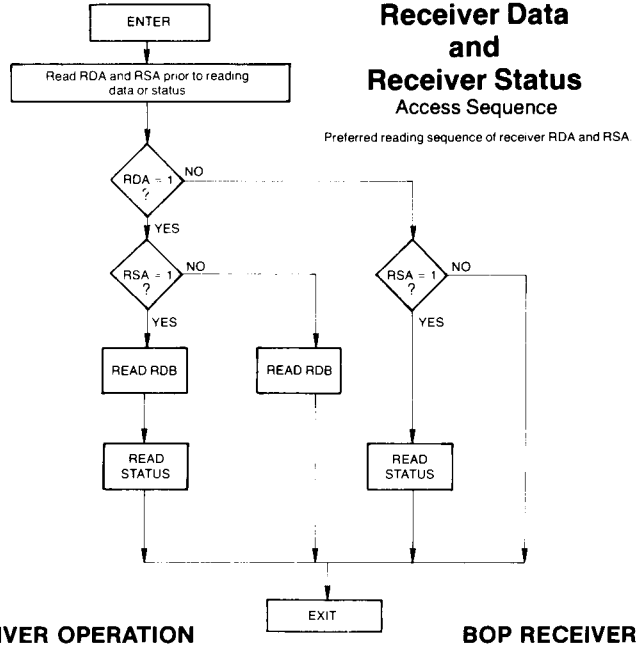
Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL}=1.6ma
High Level, V_{OH}	2.4				I_{OH}=40μa
INPUT LEAKAGE					
Data Bus		5.0	50.0	μa	0≤V_{IN}≤5v, DPENA=0 or W/R=1
All others				μa	V_{IN}=+5v
INPUT CAPACITANCE					
Data Bus, C_{IN}				pf	
Address Bus, C_{IN}				pf	
Clock, C_{IN}				pf	
All other, C_{IN}				pf	
POWER SUPPLY CURRENT					
I_{CC}			70	ma	
I_{DD}			90	ma	
					T_A=25°C
A.C. Characteristics					
CLOCK-RCP, TCP					
frequency	DC		1.5	MHz	
PW_H	325			ns	
PW_L	325			ns	
t_r, t_f		10		ns	
DPENA, T_{WDPENA}	250		50 μs	ns	
Set-up Time, T_{AS}	0			ns	
Byte Op, W/R					
A_2, A_1, A_0					
Hold Time, T_{AH}	0			ns	
Byte Op, WIR,					
A_2, A_1, A_0					
DATA BUS ACCESS, T_{DPA}			150	ns	
DATA BUS DISABLE DELAY, T_{DPD}			100	ns	
DATA BUS SET-UP TIME, T_{DBS}	0			ns	
DATA BUS HOLD TIME, T_{DBH}	100			ns	
MASTER RESET, MR	350			ns	

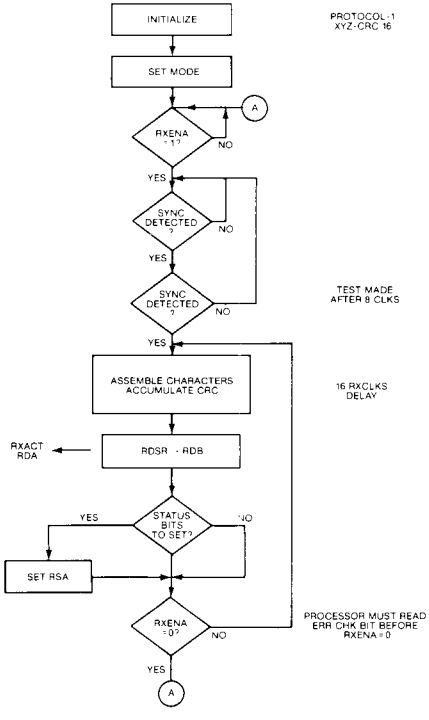


Receiver Data and Receiver Status

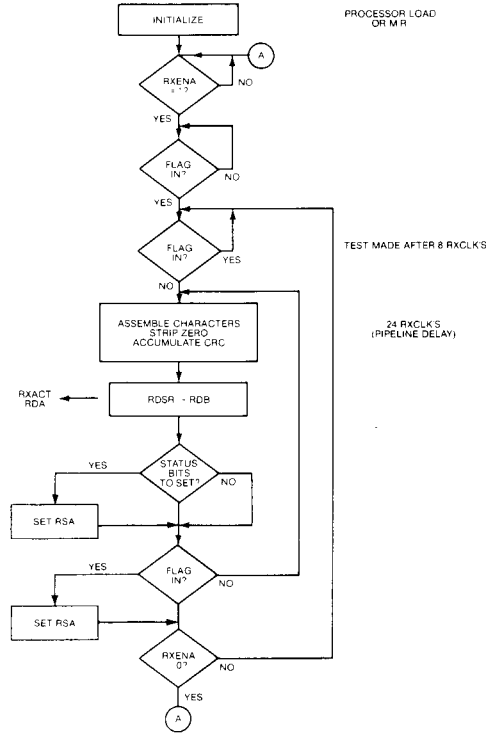
Access Sequence

Preferred reading sequence of receiver RDA and RSA

CCP RECEIVER OPERATION



BOP RECEIVER OPERATION



STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications, consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.