PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

FEATURES

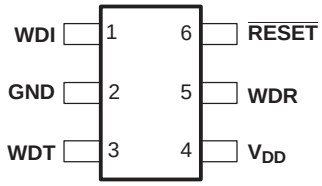
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of -55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Window-Watchdog With Programmable Delay and Window Ratio**
- **6-Pin SOT-23 Package**
- **Supply Current of 9 μA (Typ)**
- **Power On Reset Generator With a Fixed Delay Time of 25 ms**
- **Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, 5 V**
- **Open-Drain Reset Output**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- **Applications Using DSPs, Microcontrollers, or Microprocessors**
- **Safety Critical Systems**
- **Automotive Systems**
- **Healing Systems**

TPS3813
DBV PACKAGE
(TOP VIEW)



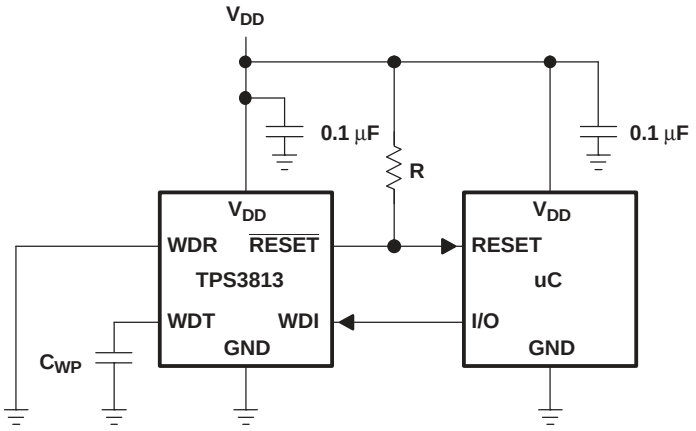
ACTUAL SIZE
3,00 mm x 3,00 mm

DESCRIPTION

The TPS3813 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power on, $\overline{\text{RESET}}$ is asserted when supply voltage (V_{DD}) becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_d = 25 ms typical, starts after V_{DD} has risen above the threshold voltage (V_{IT}). When the supply voltage drops below the threshold voltage (V_{IT}), the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage (V_{IT}) set by an internal voltage divider.

TYPICAL OPERATING CIRCUIT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

For safety critical applications the TPS3813 family incorporates a so-called window-watchdog with programmable delay and window ratio. The upper limit of the watchdog time-out can be set by either connecting WDT to GND, V_{DD}, or using an external capacitor. The lower limit and thus the window ratio is set by connecting WDR to GND or V_{DD}. The supervised processor now needs to trigger the TPS3813 within this window not to assert a $\overline{\text{RESET}}$.

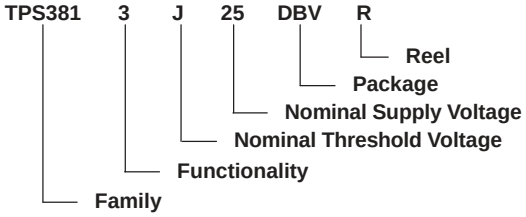
The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 6-pin SOT-23 package.

The TPS3813 devices are characterized for operation over a temperature range of –55°C to 125°C.

PACKAGE INFORMATION

T_A	DEVICE NAME	THRESHOLD VOLTAGE	MARKING
–55°C to 125°C	TPS3813J25MDBVREP	2.25 V	PLEM
	TPS3813L30MDBVREP	2.64 V	PLFM
	TPS3813K33MDBVREP	2.93 V	PLGM
	TPS3813I50MDBVREP	4.55 V	PLHM

ORDERING INFORMATION



TPS3813 FUNCTION/TRUTH TABLE

$V_{DD} > V_{IT}$	$\overline{\text{RESET}}$
0	L
1	H

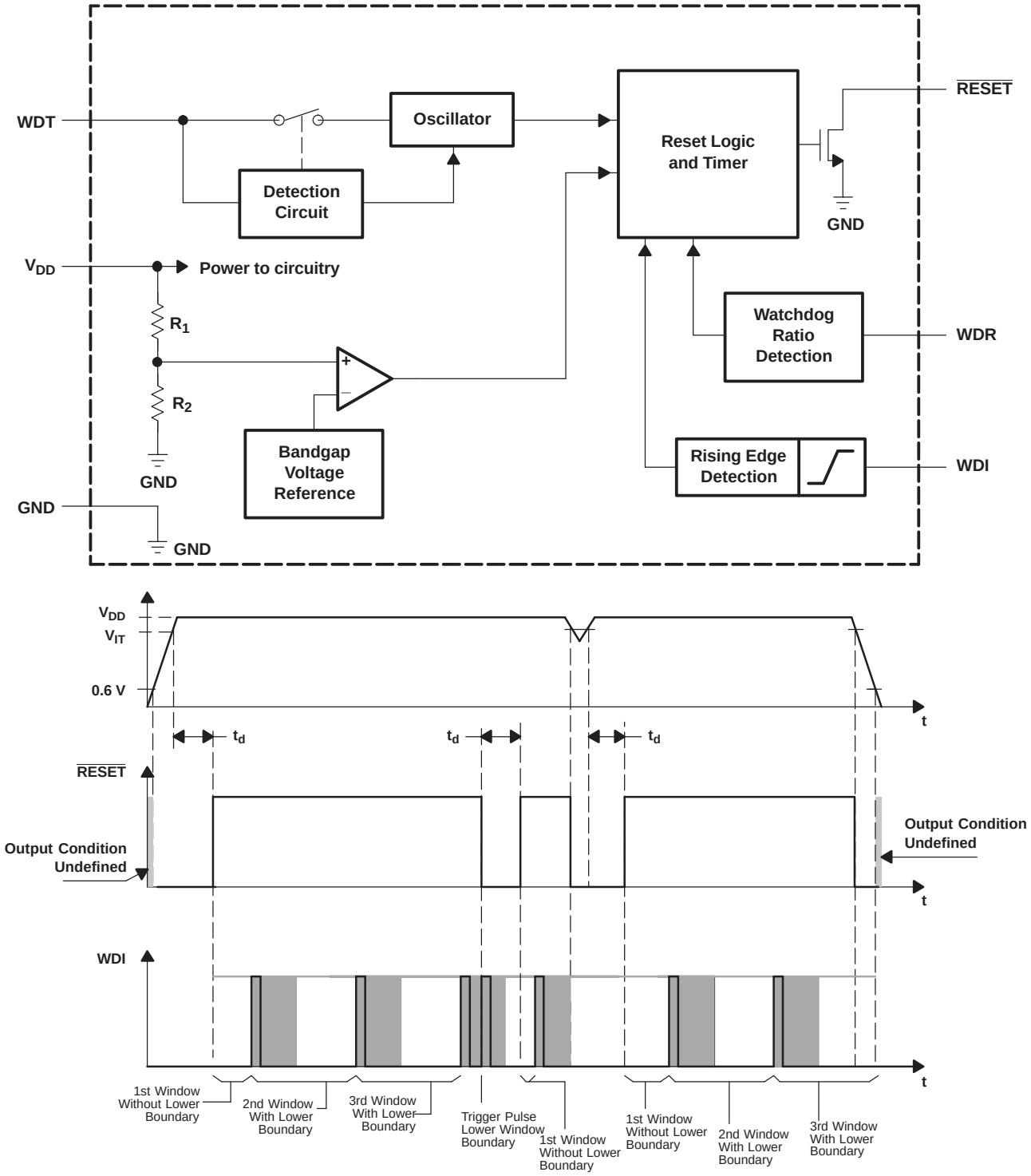


Figure 1. Timing Diagram

The lower boundary of the watchdog window starts with the rising edge of the WDI trigger pulse. At the same time, all internal timers will be reset. If an external capacitor is used, the lower boundary is impacted due to the different oscillator frequency. This is described in more detail in the following section. The timing diagram and especially the shaded boundary is prepared in a nonreal ratio scale to better visualize the description.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	2	I	Ground
$\overline{\text{RESET}}$	6	O	Open-drain reset output
V_{DD}	4	I	Supply voltage and supervising input
WDI	1	I	Watchdog timer input
WDR	5	I	Selectable watchdog window ratio input
WDT	3	I	Programmable watchdog delay input

DETAILED DESCRIPTION

IMPLEMENTED WINDOW-WATCHDOG SETTINGS

There are two different ways to set up the watchdog window. The first way is to use the implemented timing which is a default setting. Or, the default settings can be activated by wiring the WDT and WDR pin to V_{DD} or GND. There are a total of four different timings available with these settings which are listed in the table below.

SELECTED OPERATION MODE		WINDOW FRAME	LOWER WINDOW FRAME
WDT = 0 V	WDR = 0 V	Max = 0.3 s	Max = 9.46 ms
		Typ = 0.25 s	Typ = 7.86 ms
		Min = 0.2 s	Min = 6.27 ms
	WDR = V_{DD}	Max = 0.3 s	Max = 2.43 ms
		Typ = 0.25 s	Typ = 2 ms
		Min = 0.2 s	Min = 1.58 ms
WDT = V_{DD}	WDR = 0 V	Max = 3 s	Max = 93.8 ms
		Typ = 2.5 s	Typ = 78.2 ms
		Min = 2 s	Min = 62.5 ms
	WDR = V_{DD}	Max = 3 s	Max = 23.5 ms
		Typ = 2.5 s	Typ = 19.6 ms
		Min = 2 s	Min = 15.6 ms

To visualize the values named in the table, a timing diagram (see Figure 2) was prepared. The timing diagram is used to describe the upper and lower boundary settings. For an application, the important boundaries are the $t_{boundary,max}$ and $t_{window,min}$. Within these values, the watchdog timer should be retriggered to avoid a timeout condition or a boundary violation in the event of a trigger pulse in the lower boundary. The values in the table above are typical and worst case conditions. They are valid over the whole temperature range of –55°C to 125°C.

In the shaded area of Figure 2, it cannot be predicted if the device will detect a violation or not and release a reset. This is also the case between the boundary tolerance of $t_{boundary,min}$ and $t_{boundary,max}$ as well as between $t_{window,min}$ and $t_{window,max}$. It is important to set up the trigger pulses accordingly to avoid violations in these areas.

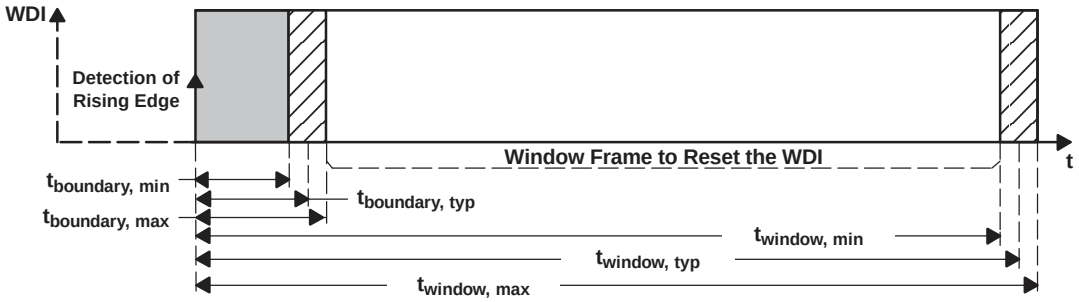


Figure 2. Upper and Lower Boundary Visualization

TIMING RULES OF WINDOW-WATCHDOG

After the reset of the supervisor is released, the lower boundary of the first WDI window is disabled. However, after the first WDI pulse low-to-high transition is detected, the lower boundary function of the window is enabled. All further WDI pulses will need to fit into the configured window frame.

PROGRAMMABLE WINDOW-WATCHDOG BY USING AN EXTERNAL CAPACITOR

The upper boundary of the watchdog timer can be set by an external capacitor connected between the WDT pin and GND. Common consumer electronic capacitors can be used to implement this feature. They should have low ESR and low tolerances since the tolerances have to be considered if the calculations are performed. The first formula is used to calculate the upper window frame. After calculating the upper window frame, the lower boundary can be calculated. As in the last example, the most important values are the $t_{boundary,max}$ and $t_{window,min}$. The trigger pulse has to fit into this window frame.

The external capacitor should have a value between a minimum of 47 pF and a maximum of 63 nF.

SELECTED OPERATION MODE		WINDOW FRAME
WDT = external capacitor $C_{(ext)}$	WDR = 0 V and WDR = V_{DD}	$t_{window,max} = 1.25 \times t_{window,typ}$
		$t_{window,min} = 0.75 \times t_{window,typ}$

$$t_{window,typ} = \left(\frac{C_{(ext)}}{15.55\ pF} + 1 \right) \times 6.25\ ms \quad (1)$$

LOWER BOUNDARY CALCULATION

The lower boundary can be calculated based on the values given in the switching characteristics. Additionally, facts have to be taken into account to verify that the lower boundary is where it is expected. Since the internal oscillator of the window watchdog is running free, any rising edge at the WDI pin will be taken into account at the next internal clock cycle. This happens regardless of the external source. Since the shift between internal and external clock is not known, it is best to consider the worst case condition for calculating this value.

SELECTED OPERATION MODE		LOWER BOUNDARY OF FRAME
WDT = external capacitor $C_{(ext)}$	WDR = 0 V	$t_{boundary,max} = t_{window,max} / 23.5$
		$t_{boundary,typ} = t_{window,typ} / 25.8$
		$t_{boundary,min} = t_{window,min} / 28.7$
	WDR = V_{DD}	$t_{boundary,max} = t_{window,max} / 51.6$
		$t_{boundary,typ} = t_{window,typ} / 64.5$
		$t_{boundary,min} = t_{window,min} / 92.7$

WATCHDOG SOFTWARE CONSIDERATIONS

To benefit from the window watchdog feature and help the watchdog timer monitor the software execution more closely, it is recommended that the watchdog be set and reset at different points in the program rather than pulsing the watchdog input periodically by using the prescaler of a microcontroller or DSP. Furthermore, the watchdog trigger pulses should be set to different timings inside the window frame to release a defined reset, if the program should hang in any subroutine. This allows the window watchdog to detect timeouts of the trigger pulse as well as pulses that distort the lower boundary.

APPLICATION EXAMPLE

A typical application example (see Figure 3) is used to describe the function of the watchdog in more detail.

To configure the window watchdog function, two pins are provided by the TPS3813. These pins set the window timeout and ratio.

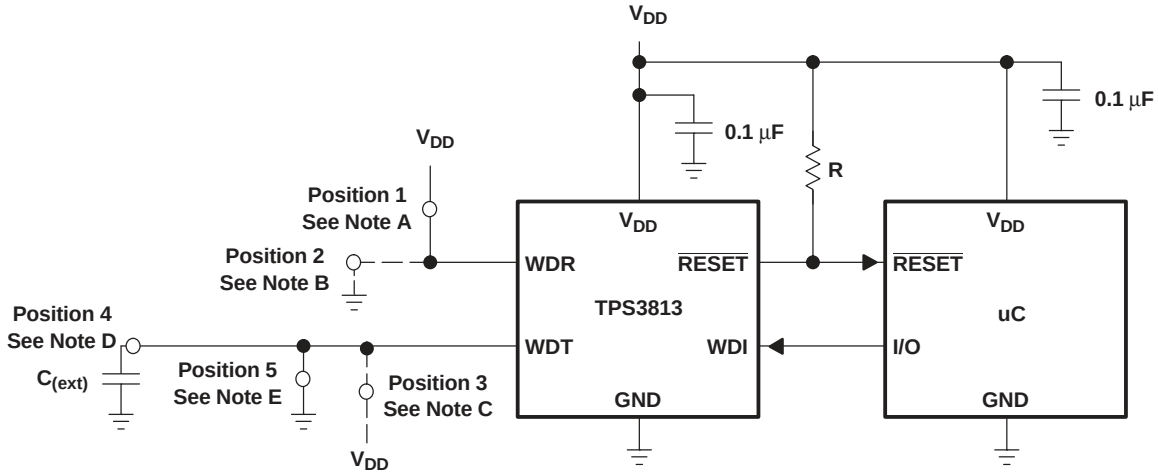
The window watchdog ratio is a fixed ratio, which determines the lower boundary of the window frame. It can be configured in two different frame sizes.

If the window watchdog ratio pin (WDR) is set to V_{DD}, Position 1 in Figure 3, then the lower window frame is a value based on a ratio calculation of the overall window timeout size: For the watchdog timeout pin (WDT) connected to GND, it is a ratio of 1:124.9, for WDT connected to V_{DD}, it is a ratio of 1:127.7, and for an external capacitor connected to WDT, it is a ratio of 1:64.5.

If the window watchdog ratio pin (WDR) is set to GND, Position 2, the lower window frame will be a value based on a ratio calculation of the overall window timeout size: For the watchdog timeout pin (WDT) connected to GND, it will be a ratio of 1:31.8, for WDT connected to V_{DD} it will be 1:32, and for an external capacitor connected to WDT it will be 1:25.8.

The watchdog timeout can be set in two fixed timings of 0.25 seconds and 2.5 seconds for the window or can by programmed by connecting a external capacitor with a low leakage current at WDT.

Example: If the watchdog timeout pin (WDT) is connected to V_{DD}, the timeout will be 2.5 seconds. If the window watchdog ratio pin (WDR) is set in this configuration to a ratio of 1:127.7 by connecting the pin to V_{DD}, the lower boundary is 19.6 ms.



A. Watchdog window ratio
B. Watchdog timeout set to typical 2.5 sec
C. Watchdog timeout programmed by external capacitor
D. Watchdog timeout set to typical 0.25 sec

Figure 3. Application Example

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
V_{DD}	Supply voltage(2)	7 V
	RESET	–0.3 V to V_{DD} + 0.3 V
	All other pins (2)	–0.3 V to 7 V
I_{OL}	Maximum low output current	5 mA
I_{OH}	Maximum high output current	–5 mA
I_{IK}	Input clamp current (V_I < 0 or V_I > V_{DD})	±20 mA
I_{OK}	Output clamp current (V_O < 0 or V_O > V_{DD})	±20 mA
	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range	–55°C to 125°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Soldering temperature	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device should not be operated at 7 V for more than t = 1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

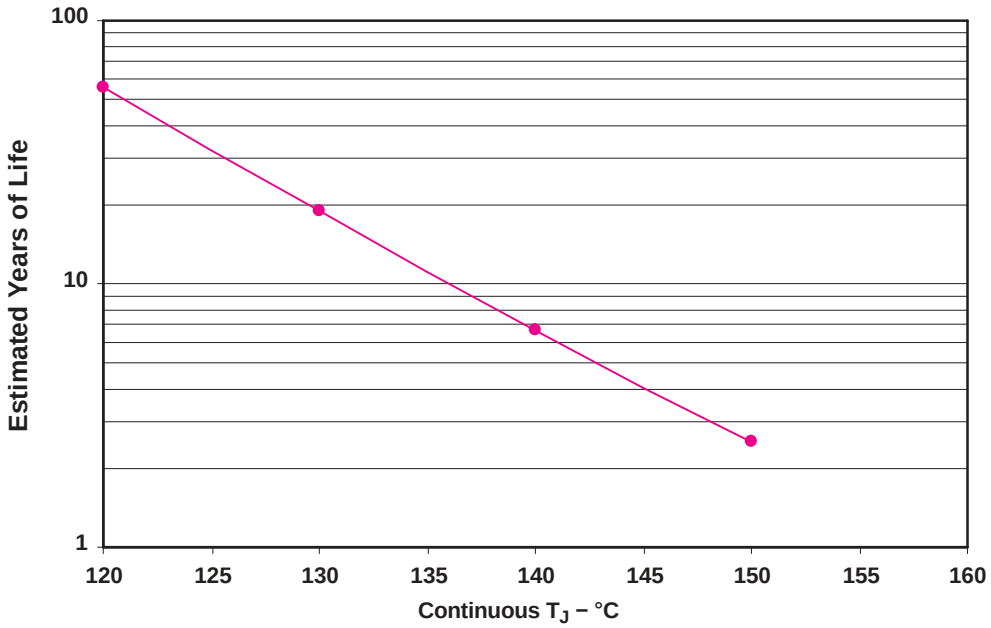


Figure 4. TPS3813K33DBV Wirebond Life

RECOMMENDED OPERATING CONDITIONS

at specified temperature range

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2	6	V
V_I	Input voltage	0	V_{DD} + 0.3	V
V_{IH}	High-level input voltage	0.7 x V_{DD}		V
V_{IL}	Low-level input voltage		0.3 x V_{DD}	V
$\Delta t/\Delta V$	Input transition rise and fall rate		100	ns/V
t_w	Pulse width of WDI trigger pulse	50		ns
T_A	Operating free-air temperature range	–55	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V, I_{OL} = 500 µA				0.2	V
			V_{DD} = 3.3 V I_{OL} = 2 mA				0.4	
			V_{DD} = 6 V, I_{OL} = 4 mA				0.4	
	Power up reset voltage (1)		V_{DD} ≥ 1.1 V, I_{OL}= 50 µA				0.2	V
V_{IT}	Negative-going input threshold voltage (2)	TPS3813J25			2.2	2.25	2.3	V
		TPS3813L30			2.58	2.64	2.7	
		TPS3813K33	T_A = 25°C		2.87	2.93	3	
			T_A = Full Range		2.8		3.1	
		TPS3813I50			4.45	4.55	4.65	
V_{hys}	Hysteresis	TPS3813J25				30		mV
		TPS3813L30				35		
		TPS3813K33				40		
		TPS3813I50				60		
I_{IH}	High-level input current	WDI, WDR	WDI = V_{DD} = 6 V, WDR = V_{DD} = 6 V	T_A = 25°C	–100		100	nA
				T_A = Full Range	–1000		1000	
		WDT	WDT = V_{DD} = 6 V, V_{DD} > V_{IT}, $\overline{RESET}$ = High	T_A = 25°C	–100		100	
				T_A = Full Range	–1000		1000	
I_{IL}	Low-level input current	WDI, WDR	WDI = 0 V, WDR = 0 V, V_{DD} = 6 V	T_A = 25°C	–100		100	
				T_A = Full Range	–1000		1000	
		WDT	WDT = 0 V, V_{DD} > V_{IT}, $\overline{RESET}$ = High	T_A = 25°C	–100		100	
				T_A = Full Range	–1000		1000	
I_{OH}	High-level output current		V_{DD} = V_{OH} = 6 V	T_A = 25°C			100	nA
				T_A = Full Range			1000	
I_{DD}	Supply current		V_{DD} = 2 V output unconnected			9	13	µA
			V_{DD} = 5 V output unconnected			20	25	
C_I	Input capacitance		V_I = 0 V to V_{DD}			5		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥ 15 µs/V.
(2) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminals.

TIMING REQUIREMENTS

at R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width at V_{DD}	V_{DD} = $V_{IT–}$ + 0.2 V, V_{DD} = $V_{IT–}$ – 0.2 V	3			µs

SWITCHING CHARACTERISTICS

at R_L = 1 MΩ, C_L = 50 pF, T_A = -55°C to 125°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} \geq V_{IT}$ + 0.2 V, See Figure 1	T_A = 25°C	20	25	30	ms
				T_A = Full Range	15		40	
$t_{t(out)}$	Watchdog time-out	Upper limit	WDT = 0 V			0.25		s
			WDT = V_{DD}			2.5		
			WDT = programmable (1)			See (2)		ms
	Watchdog window ratio		WDR = 0 V, WDT = 0 V			1:31.8		
			WDR = 0 V, WDT = V_{DD}			1:32		
			WDR = 0 V, WDT = programmable			1:25.8		
			WDR = V_{DD}, WDT = 0 V			1:124.9		
			WDR = V_{DD}, WDT = V_{DD}			1:127.7		
			WDR = V_{DD}, WDT = programmable			1:64.5		
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{\text{RESET}}$ delay	$V_{IL} = V_{IT}$ - 0.2 V, $V_{IH} = V_{IT}$ + 0.2 V			30		µs

(1) 155 pF < $C_{(ext)}$ < 63 nF
(2) ($C_{(ext)}$ ÷ 15.55 pF + 1) x 6.25 ms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

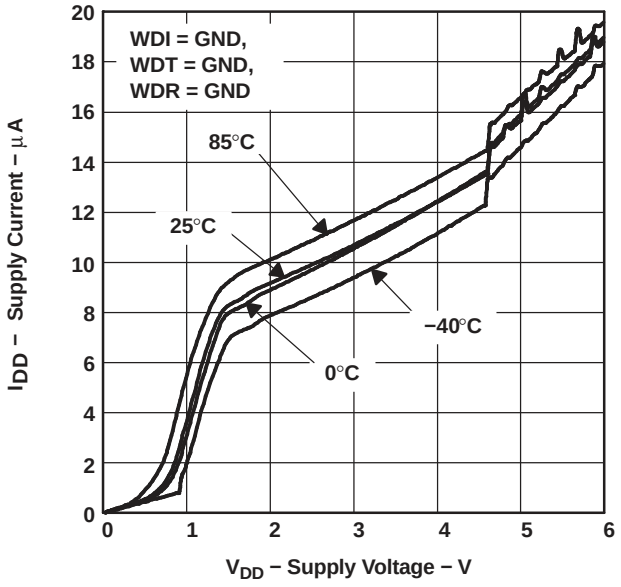


Figure 5.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

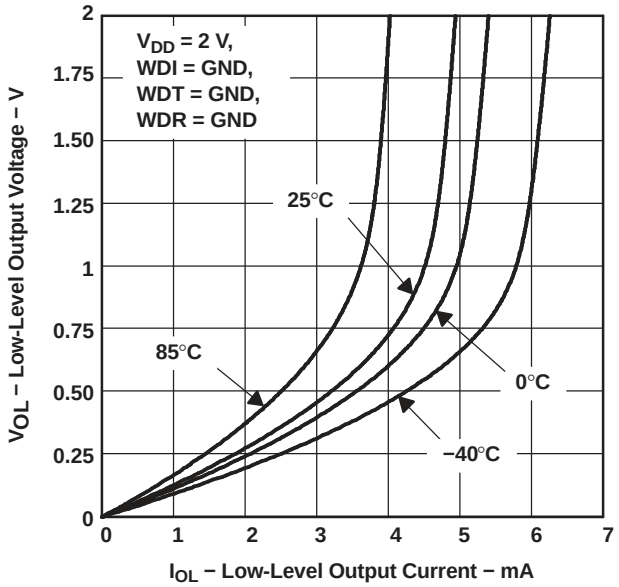


Figure 6.

TYPICAL CHARACTERISTICS (continued)

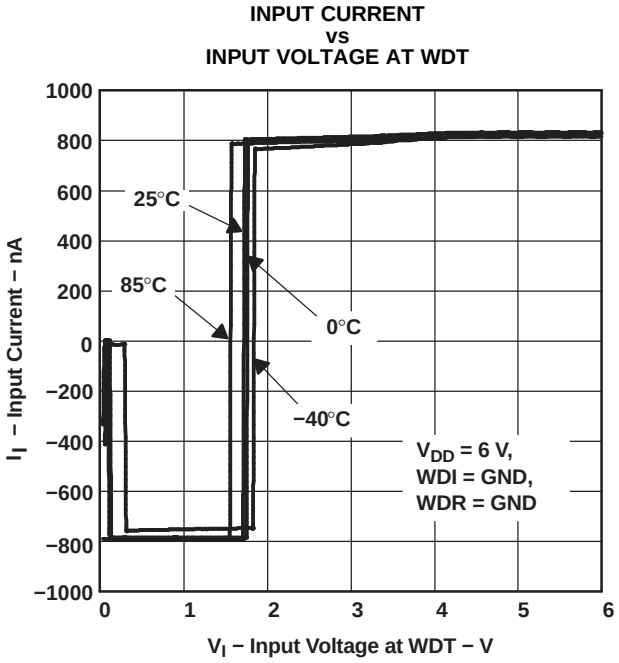


Figure 7.

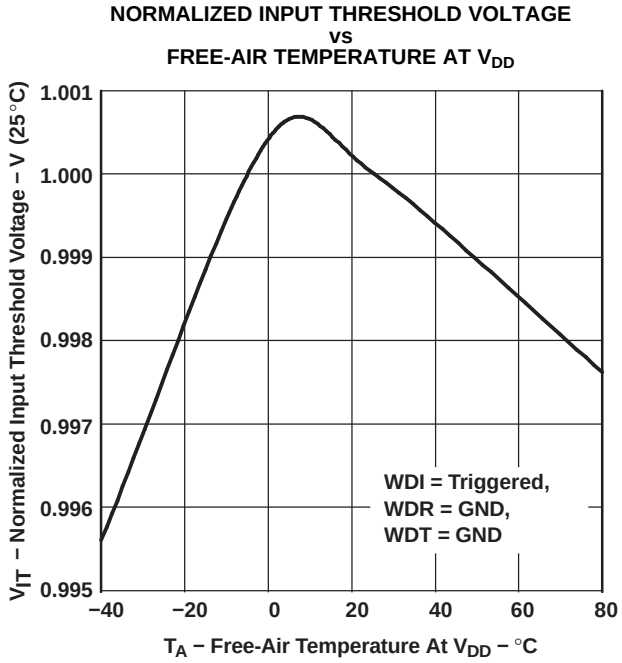


Figure 8.

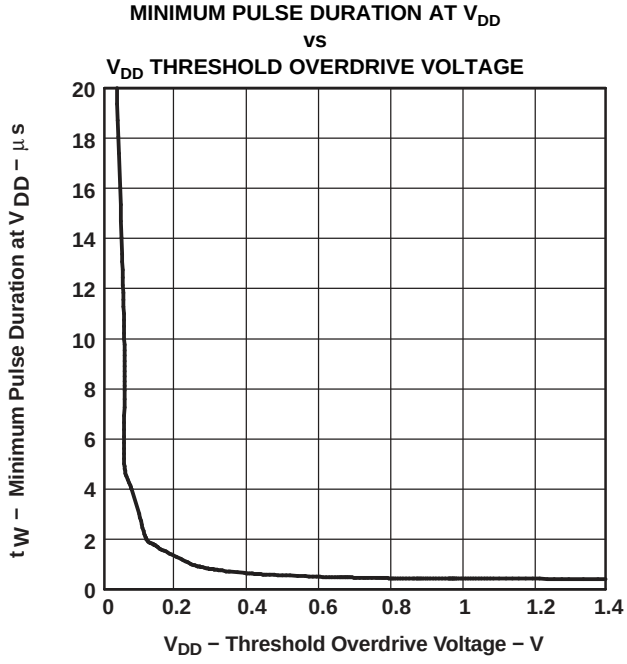


Figure 9.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
2T13K33MDBVREPG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PLGM	Samples
TPS3813K33MDBVREP	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PLGM	Samples
V62/06627-01XE	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PLGM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

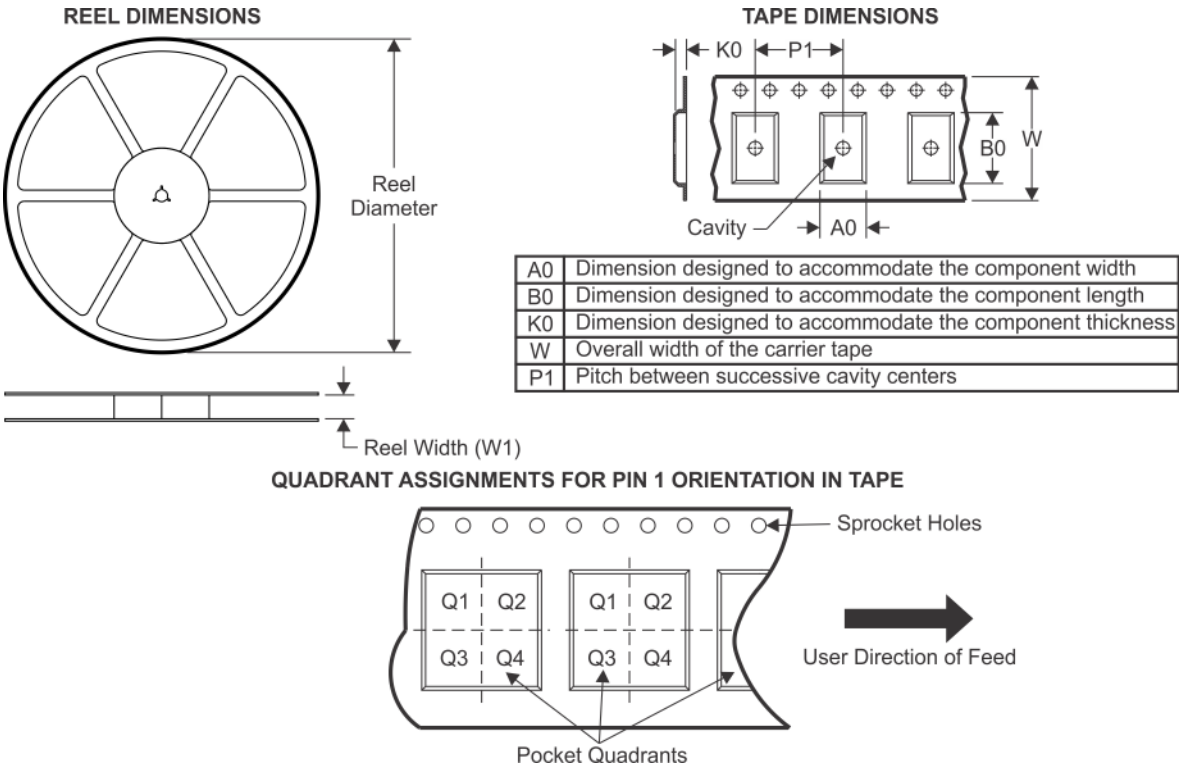
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

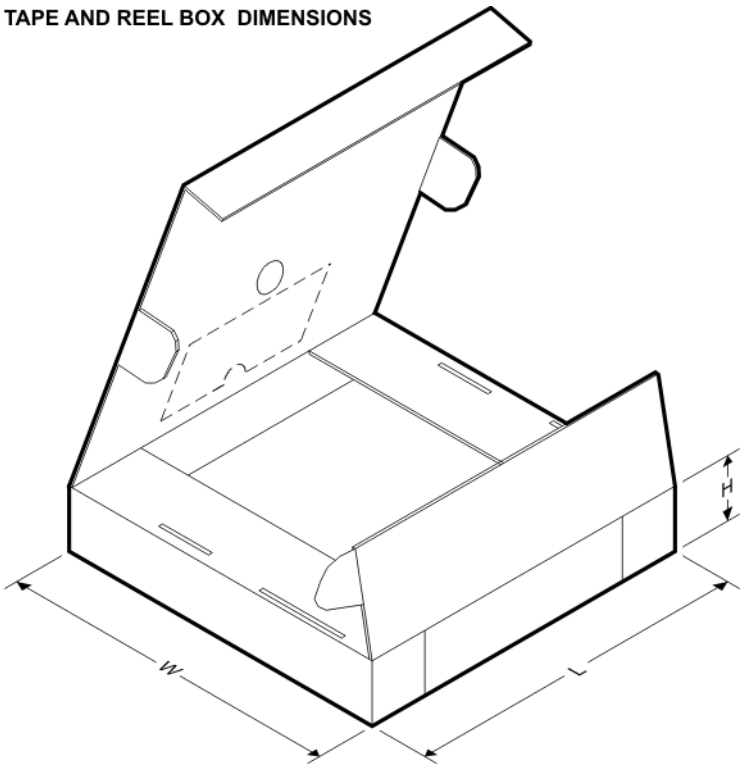


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3813K33MDBVREP	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

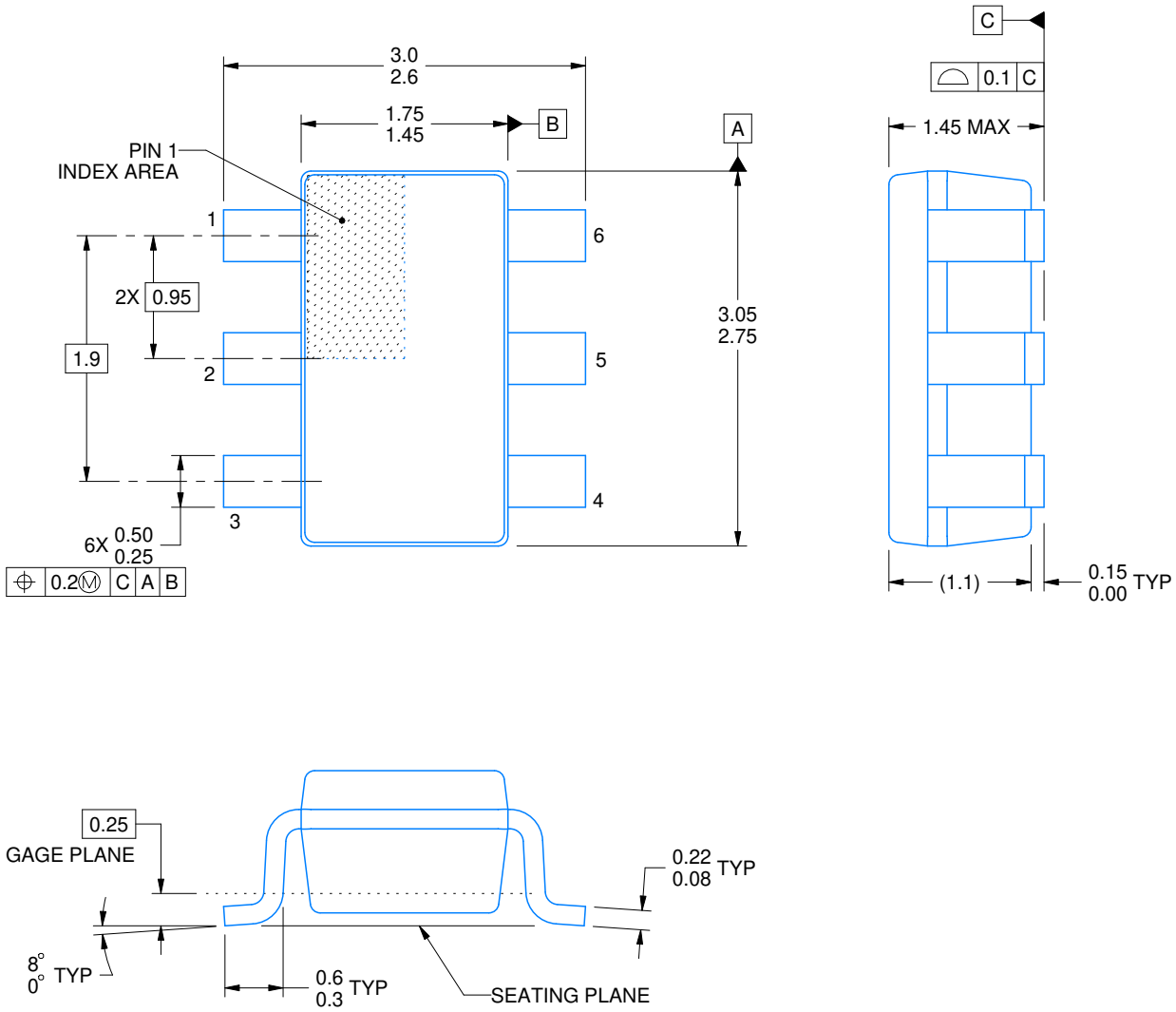
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3813K33MDBVREP	SOT-23	DBV	6	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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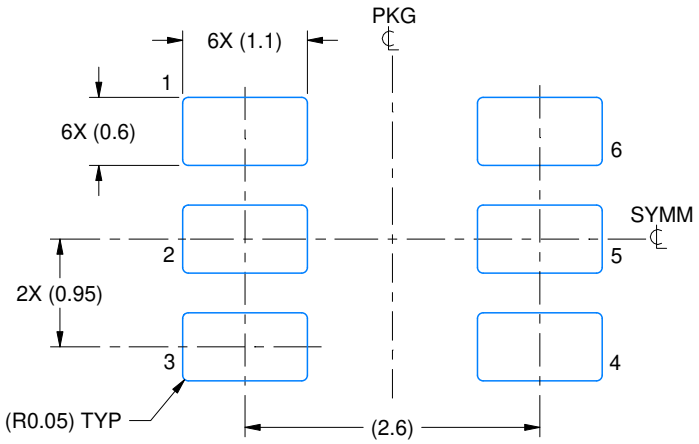
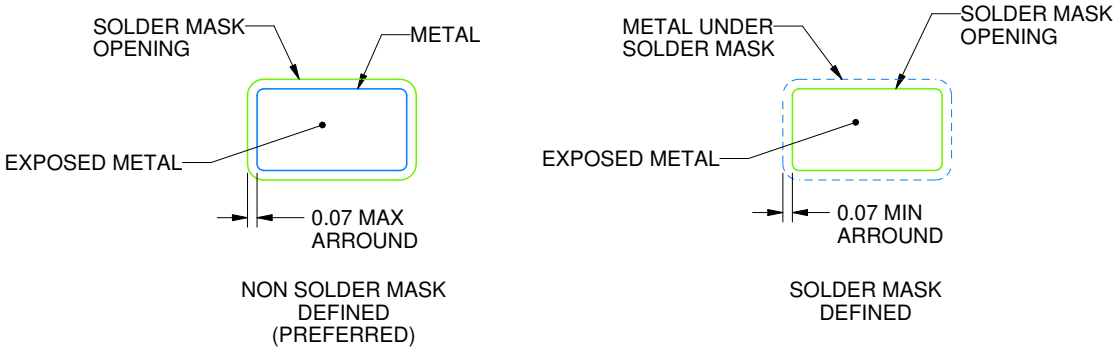
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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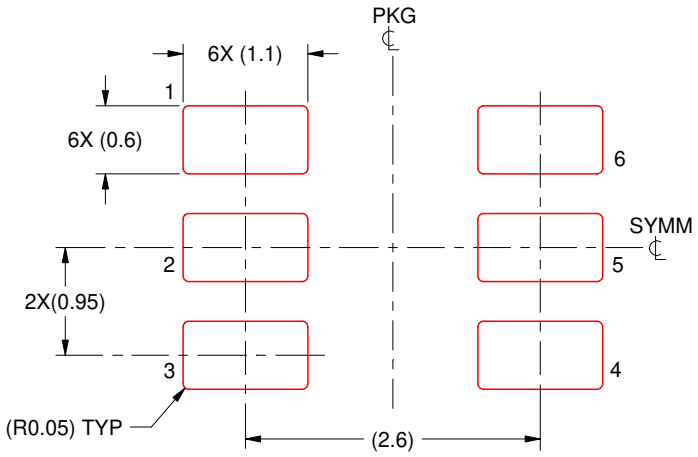
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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