Burr-Brown Products
from Texas Instruments

DEM-DAI1704/06 Demo Board

User's Guide

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DAV Digital Audio/Imaging Japan (DAIJ)

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Chapter 1

DEM-DAI1704/06 Module Description

The DEM-DAI1704/06 is an evaluation module for the PCM1704 and DF1704/DF1706 digital-to-analog converters (DACs). This module can achieve 24-bit/96-kHz sampling format.

This DEM-DAI1704/06 uses two PCM1704 DACs (stereo), two OPA627 for current/voltage amplification, an OPA2134 in a second-order low-pass filter (LPF) in the analog section, and a digital audio receiver and a DF1704/DF1706 DAC in the digital section.

Digital data can be connected to either input of the DF1704/DF1706 or directly input into the PCM1704. An SPDIF signal is also accepted by the digital audio interface device (coax and optic).

The DEM-DAI1704/06 requires three power supplies: 5 V for digital, ±5 V for the DACs (PCM1704), and ±15 V for the analog output circuit.

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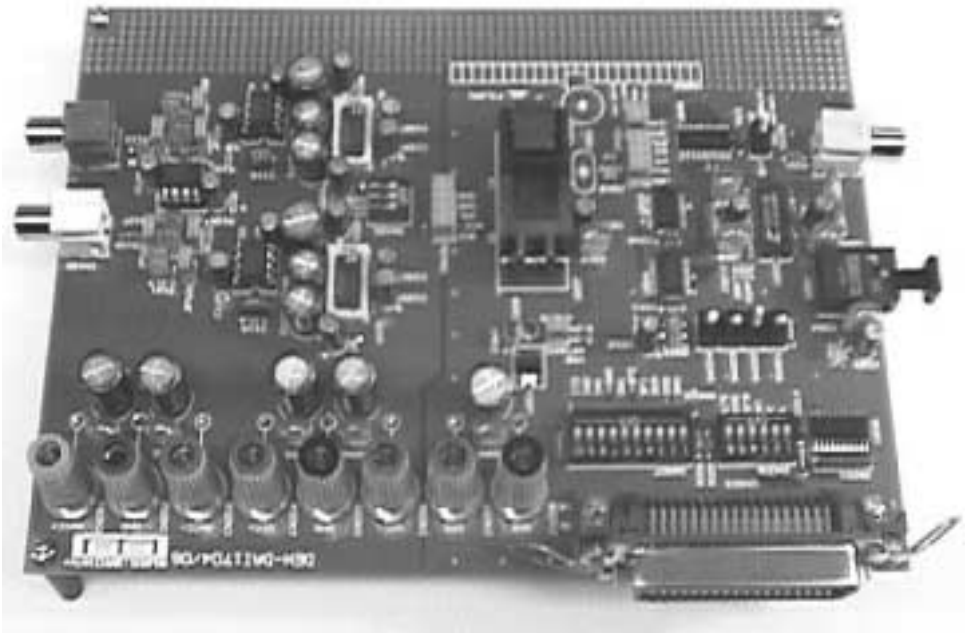
Figure 1–1. DEM-DAI1704/06 Board



The following table provides ordering information for the DEM-DAI1704/06 evaluation module.

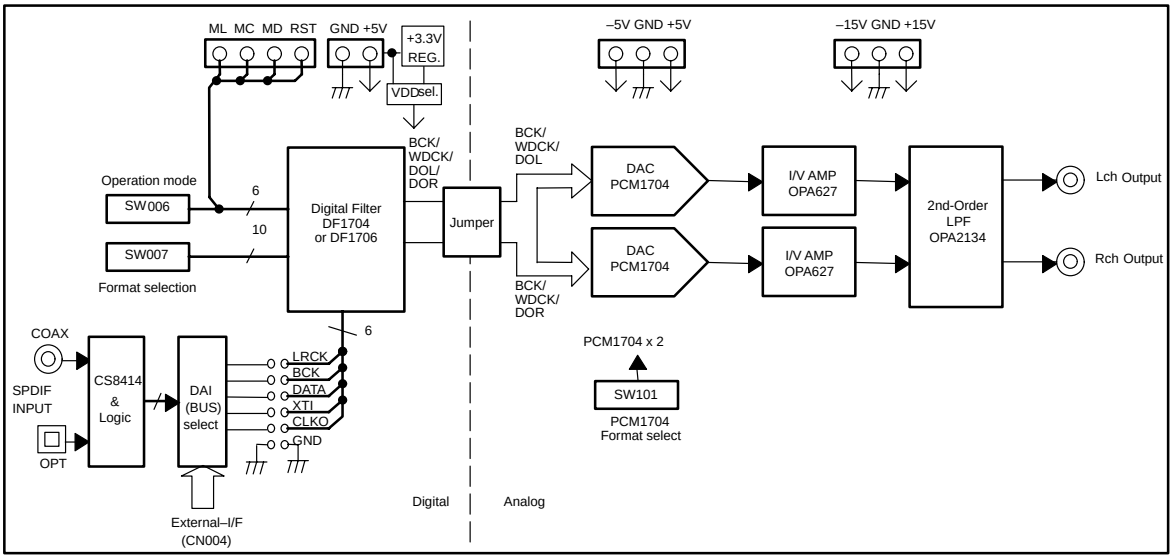
1.1 Ordering Information

Model	Construction
DEM-DAI1704	DF1704+PCM1704
DEM-DAI1706	DF1706+PCM1704

1.2 Block Diagram

Figure 1–2 shows the internal block diagram of the DEM–DAI1704/06 board.

Figure 1–2. Internal Block Diagram



1.3 DEM-DAI1704/06

- ❏ Connect the 5-V, ±5-V, and ±15-V power supplies to V_{DD}, V_{CC}, $-V_{CC}$, AV_{CC}, $-AV_{CC}$, and GND through connectors CN051–058.
- ❏ Connect SPDIF signal to CN001(COAX) or U001(OPT).
- ❏ Set all positions of SW006 to high and all positions of SW007 to low for software control.
- ❏ Set input data format and demonstration software with SW001–003.

The system clock and other digital signals are supplied from the digital audio receiver through the jumper block to DF1704 or DF1706.

1.4 Configuration Controls

1.4.1 Digital Audio Receiver

1.4.1.1 Output Data Format

SW001 (M0)	SW002 (M1)	SW003 (M2)	OUTPUT DATA FORMAT
L	L	L	16–24-bit left-justified, MSB-first
L	H	L	I^2S
H	L	H	16-bit standard, right-justified
L	H	H	18-bit standard, right-justified

SW004: Manual reset for CS8414
SW005: Digital audio interface selection:
Internal—CS8414
External—(CN004)
JP001: BCK Selection:
Remove the jumper from *BCK* to *BCK(L/J)* when using *left-justified MSB-first* data format.

1.4.2 Digital Filter (DF1704/DF1706)

1.4.2.1 Serial I/F

SW006	H	L
MUTE	Mute off	Mute on
MODE	Software mode	Hardware mode
RSTB	Normal operation	Reset operation
MDI(CKO)	x2 input	Same as input
MC(LRIP)	H: L–ch, L: R–ch	H: R–ch, L: L–ch
ML(RESV)	Reserved	

ML, MC, MD: These pins are serial-control data input in software mode.
RESV, LRPI, CKO: Hardware can control functions by setting H or L.
LRIP : Polarity control for LRCK clock
CKO : Output clock frequency control over system clock

1.4.2.2 Filter Selection

SW007	H	L
DEM	De-emphasis on	De-emphasis off
OSS	x4 Oversampling	x8 oversampling
SRO	Slow rolloff	Sharp rolloff

1.4.2.3 Input Data Format

IIS	IW1	IW0	Input Data Format
L	L	L	16-bit standard, right-justified
L	L	H	20-bit standard, right-justified
L	H	L	24-bit standard, right-justified
L	H	H	16-24-bit left-justified, MSB-first
H	L	L	16-bit I^2S
H	L	H	24-bit I^2S

1.4.2.4 Output Data Format

OW1	OW2	Input Data Format
L	L	16-bit MSB-first

L	H	18-bit MSB-first
H	L	20-bit MSB-first
H	H	24-bit MSB-first

1.4.2.5 Sampling Rate for De-Emphasis Control

SF1	SF0	Input Data Format
L	L	44.1 kHz
L	H	Reserved
H	L	48 kHz
H	H	32 kHz

1.4.3 PCM1704

SW101	H	L
20-bit	24-bit data interface	20-bit data interface
INVL	Normal phase for L-ch	Invert phase for L-ch
INVR	Normal phase for R-ch	Invert phase for R-ch

Input data phase can be inverted by INVL, INVR control.

1.5 Jumpers

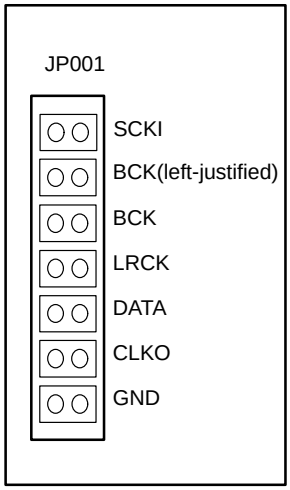
There are 19 jumpers on board:

- ❑ JP001: For digital signal to DF1704 or DF1706
- ❑ CN059: For power supply selection (3.3 V or 5 V)
- ❑ CN101: For digital signal to PCM1704
- ❑ JP101–106: For *f*c of second-order postfilter

1.5.1 JP001

The digital signal generated by the digital audio receiver is input to this jumper. If each pin is shorted, the digital signal goes to the DF1704 or DF1706.

Figure 1–3. Jumper JP001



1.5.2 CN059

The board has a 3.3-V voltage regulator used as the digital power supply for the DF1706. The CN059 jumper determines the supply voltage for the digital filter.

3.3 V: DF1706
5 V: DF1704

1.5.3 JP101–106 (Six Pieces)

These jumpers determine the *f*c of the second-order postfilter.

Short JP101–106	*f*c = 54 kHz
Open JP101–106	*f*c = 108 kHz

1.6 Demonstration Software (Version 0.0X)

Demonstration software is provided to control the DF1704/DF1706's internal register using a PC under Microsoft Windows™ 3.1/95/98. *This software uses a printer cable* to connect between the PC and the DEM-DAI1704/06's connector CN003.

1.6.1 Installation

Demonstration software includes a total five files in the DEM1704&06 directory (folder) on floppy disk. These files are:

- ❏ Dem1704&06.exe
- ❏ Dem1704&06.ini
- ❏ Vbrjp200.dll
- ❏ inpout.dll
- ❏ Ver.dll

Copy these files to a convenient directory (folder) such as C:\DEM1704&06.

Then change printer-port address in Dem1704&06.ini to:
&H378, &H278 or &H3BC0.

(Most PCs use &H378 as the default-printer port address)

1.6.2 Operation

After executing Dem1704&06.exe, the window shown in Figure 1–4 appears on the screen. This window shows the contents of the internal register.

There are two menus on top of the panel:

Execute (E): This menu has the following options:

Initialize (I): Initialize all internal register
Reset (R) : Reset all selected data to DF1704/06
Exit (X) : Exit this program

Window (W): This menu has Attenuation, Interface Format, and Function options, as shown in Figure 1–5.

Attenuation (A):

This panel controls the attenuation function of the DF1704/06.

Interface format control (I):

This panel controls input and output I/F format.

Function control (F):

This panel controls other functions.

Figure 1–4. DFI1704/06 Top Menu

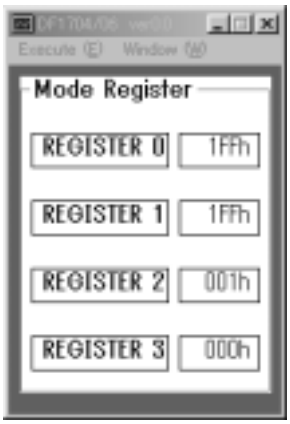
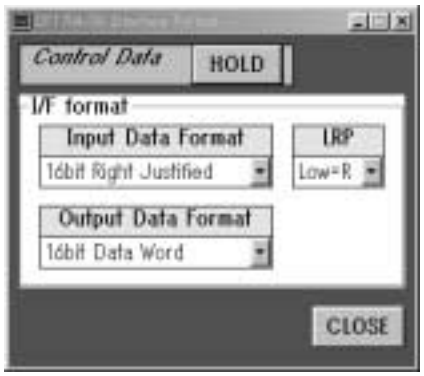


Figure 1–5. DFI1704/06 Window Submenus

Attenuation Window

Interface Format Window



Function Window

Chapter 2

Schematics and Board Layout

This chapter presents the DEM-DAI1704/06 schematics and printed circuit board layout.

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2.1 Schematics

This section presents the DEM–DAI1704/06 schematic diagrams.

Figure 2–1. Digital Section (Digital Audio Interface/Digital Filter)

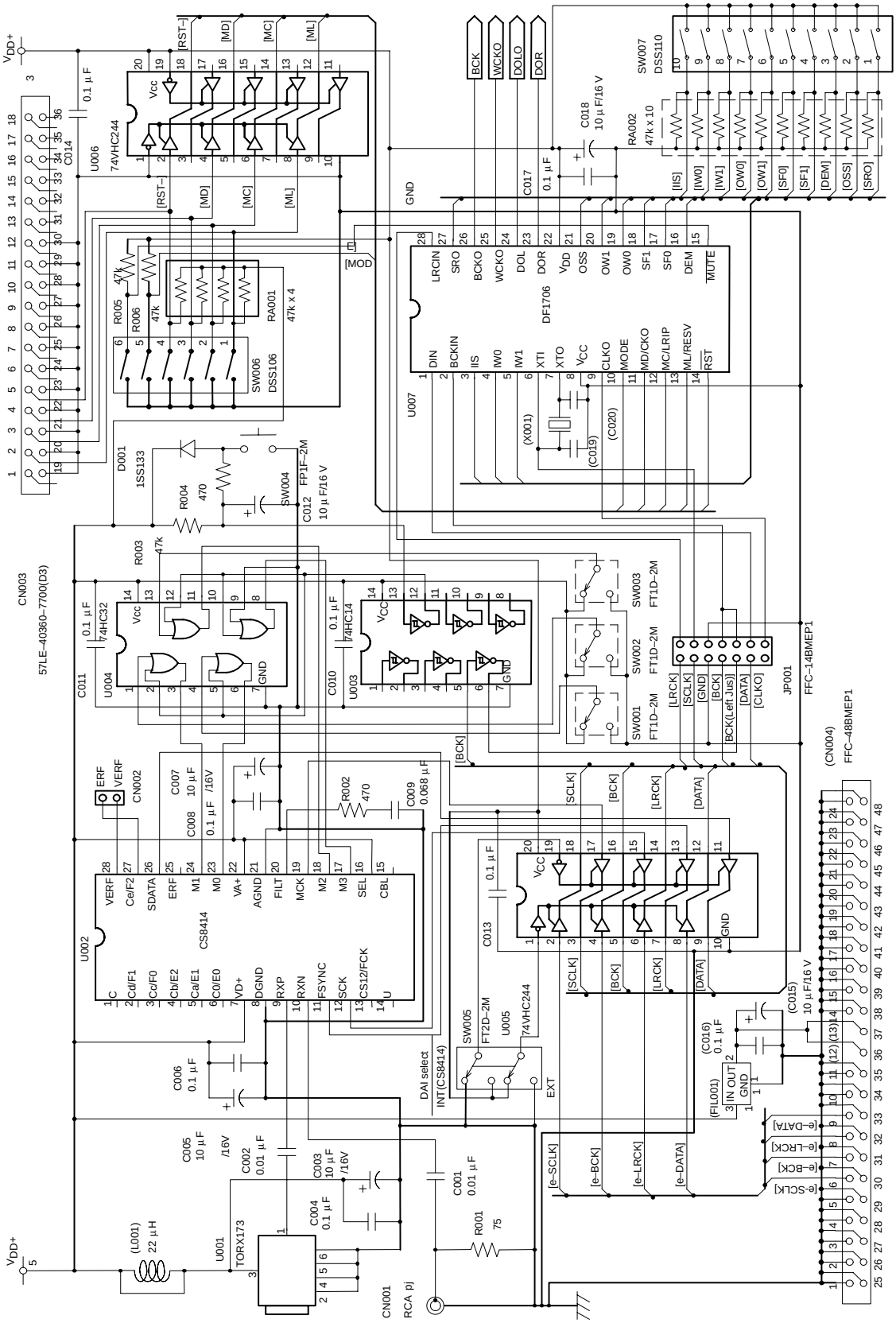


Figure 2–2. Connector and Regulator

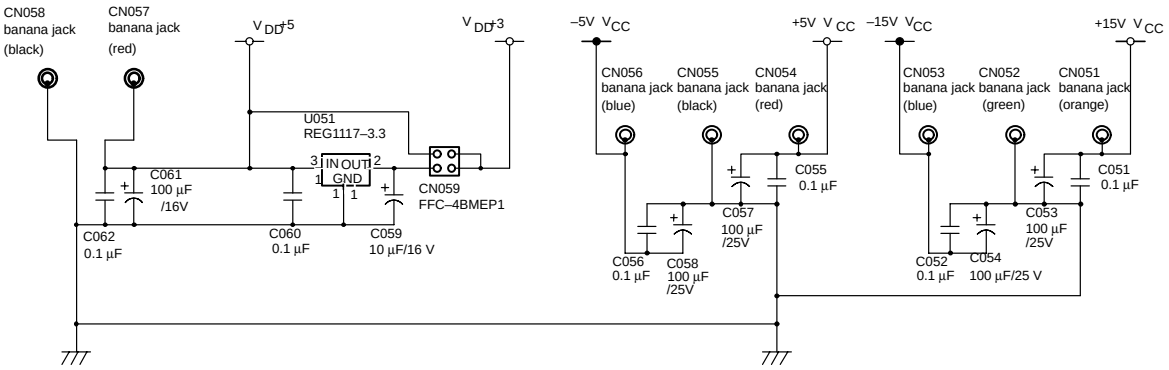
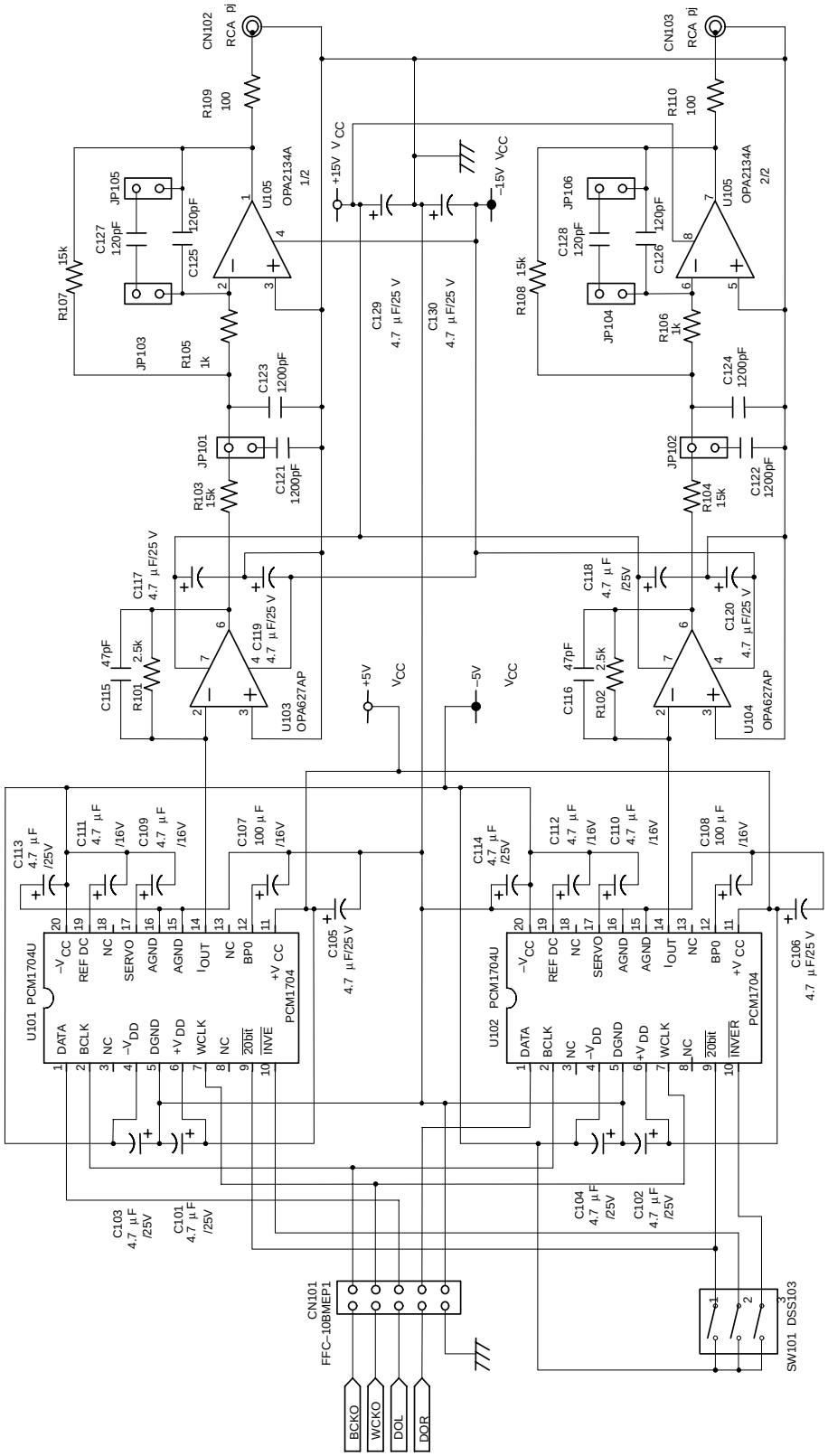


Figure 2–3. Analog Section (DAC, I/V, and LPF Amplifier)



2.2 Board Layout

This section presents the DEM–DAI1704/06 board layout.

Figure 2–4. Board Layout—Top View

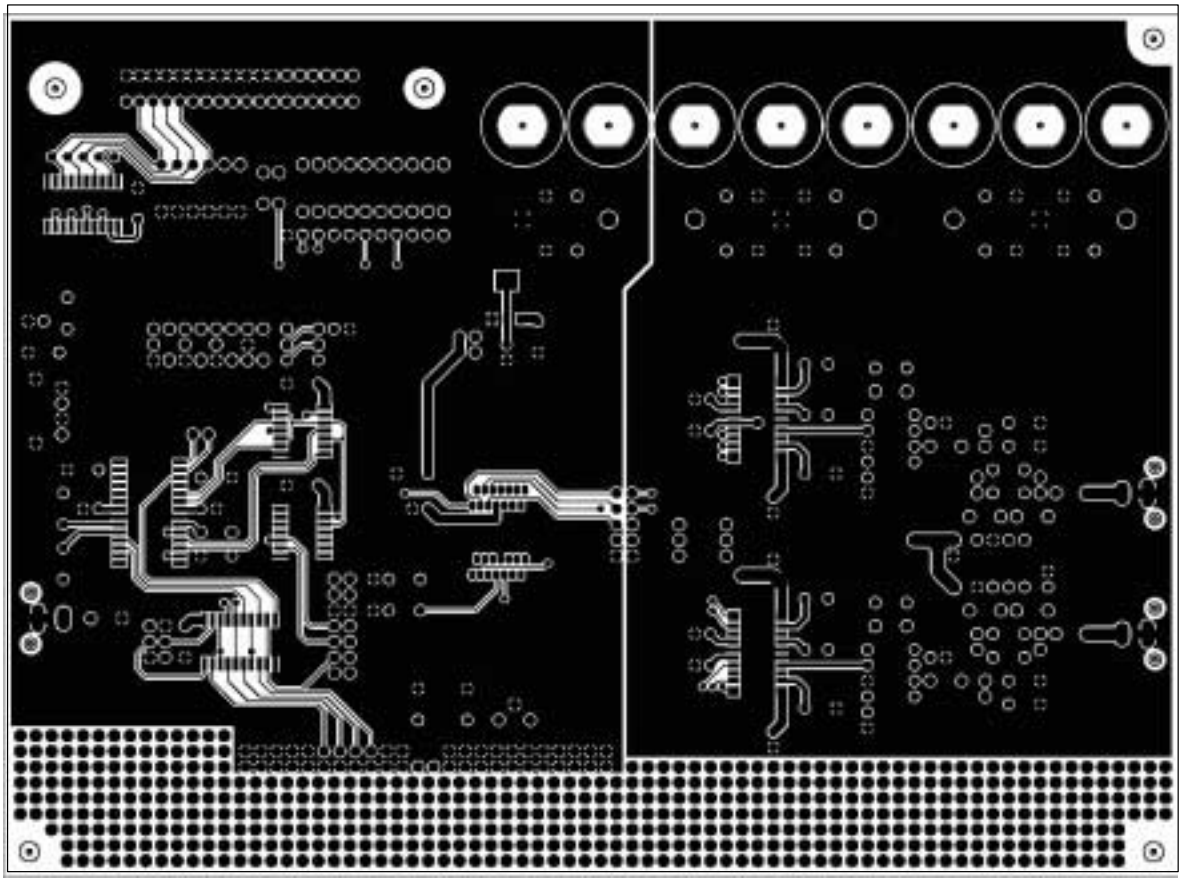


Figure 2–5. Board Layout—Bottom View

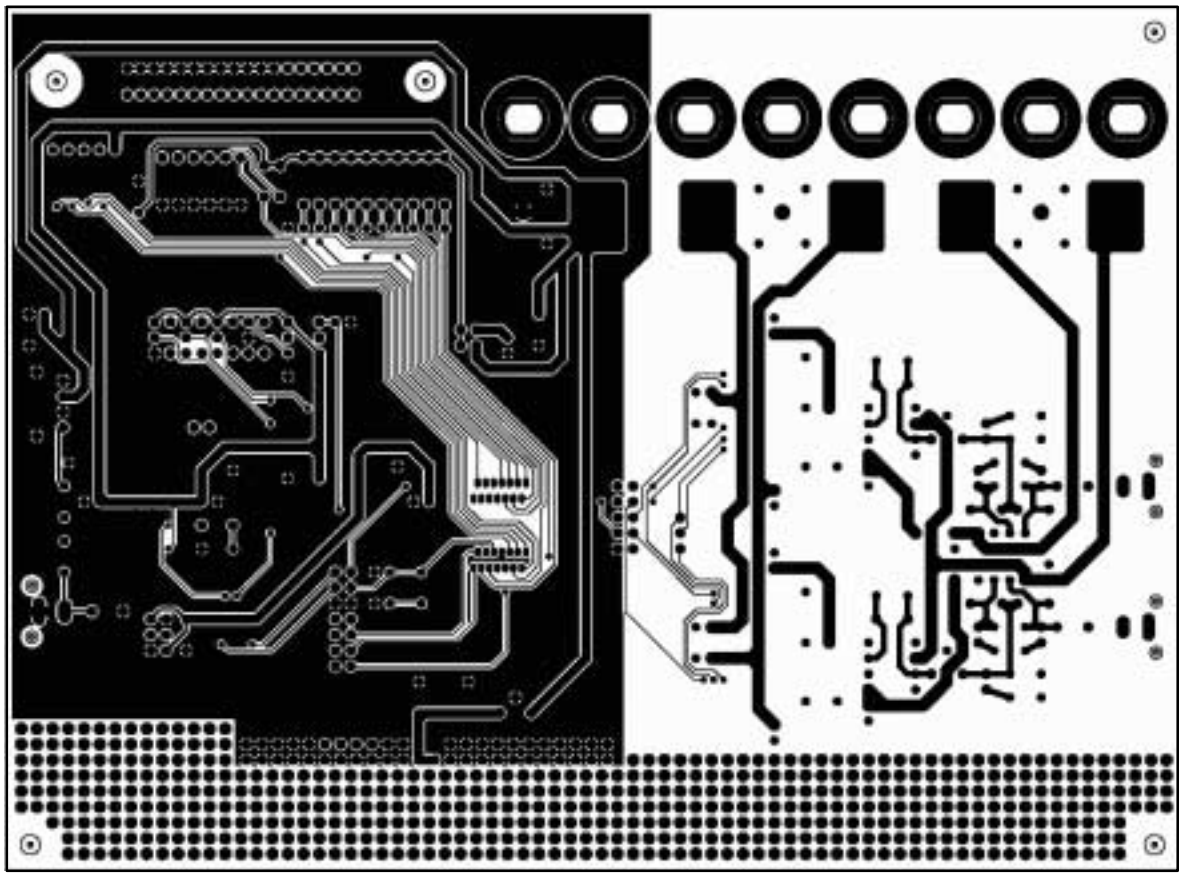


Figure 2–6. Board Layout—Silkscreen