6V, 6A, 1.5MHz ACOT® Synchronous Step-Down Converter in 2.5mm x 2mm Package

General Description

The RT5789A/B is a simple, easy-to-use, 6A synchronous step-down DC-DC converter with an input supply voltage range of 2.5V to 6V. The device build-in an accurate 0.6V (±1.5%) reference voltage and can operate in 100% duty cycle as a very low dropout voltage regulator. the RT5789A/B integrates low $R_{DS(ON)}$ power MOSFETs to achieve high efficiency and is available in TSOT-23-8 (FC) package and UDFN-8L 2.5x2(FC) package.

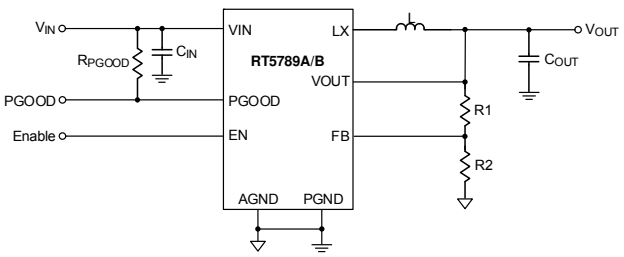
The RT5789A/B adopts Advanced Constant On-Time (ACOT®) control architecture to provide an ultrafast transient response with few external components and to operate in nearly constant switching frequency over the line, load, and output voltage range. The RT5789A/B is designed to operate at 1.5MHz fixed frequency. While the RT5789A automatically enters power saving mode (PSM) operation at light load to maintain high efficiency. RT5789B operates in Forced PWM over the loading range, that helps meet tight voltage regulation accuracy requirements.

The RT5789A/B senses both FETs current for a robust over-current protection. It prevents the device from the catastrophic damage in output short circuit, over current or inductor saturation. The individual enable control input and power good indicator provides flexible system power sequence control a built-in soft-start function prevents inrush current during start-up. The device also includes input under-voltage lockout, output under-voltage protection, and over-temperature protection (thermal shutdown) to provide safe and smooth operation in all operating conditions.

Features

- **6A Converter With Built-In 18mΩ/16mΩ Low $R_{DS(ON)}$ Power FETs**
- **Input Supply Voltage Range : 2.5V to 6V**
- **Output Voltage Range : 0.6V to 6V**
- **Operates Up to 100% Duty Cycle**
- **Advanced Constant On-Time (ACOT®) Control**
  - **Ultrafast Transient Response**
  - **No Needs For External Compensations**
  - **Optimized for Low-ESR Ceramic Output Capacitors**
- **0.6V ±1.5% High-Accuracy Feedback Reference Voltage**
- **35μA Operation Quiescent Current (RT5789A)**
- **Robust Over-Current Protection for Both FETs**
- **Optional for Operation Modes :**
  - **Power Saving Mode (PSM) (RT5789A)**
  - **Forced PWM Mode (RT5789B)**
- **Fixed Switching Frequency : 1.5MHz**
- **Monotonic Start-Up for Pre-Biased Output**
- **Individual Enable Control Input**
- **Power Good Indicator**
- **Built-In Internally Fixed Soft-Start (Typ. 1.5ms)**
- **100% Duty Cycle Mode**
- **Internal Output Discharge**
- **Input Under-Voltage Lockout (UVLO)**
- **Output Under-Voltage Protection (UVP) with Hiccup Mode**
- **Over-Temperature Protection**
- **Available in TSOT-23-8 (FC) Package and UDFN-8L 2.5x2 (FC) Package**

Simplified Application Circuit



Ordering Information

RT5789A/B □□

- Package Type
  - J8F : TSOT-23-8 (FC)
  - QUF: UDFN-8L 2.5x2 (FC) (U-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- PWM Operation Mode
  - A : Automatic PSM
  - B : Forced PWM

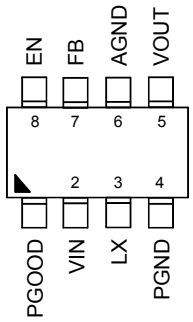
Note :

Richtek products are :

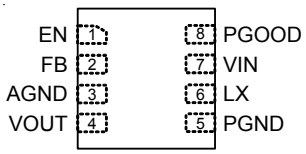
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



TSOT-23-8 (FC)



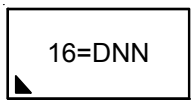
UDFN-8L 2.5x2 (FC)

Applications

- WLAN ASIC Power / Storage (SSD and HDD)
- Mobile Phones and Handheld Devices
- STB, Cable Modem, and xDSL Platforms
- General Purpose for POL LV Buck Converter

Marking Information

RT5789AGJ8F



16= : Product Code

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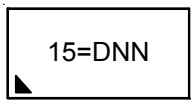
RT5789BGJ8F



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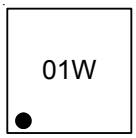

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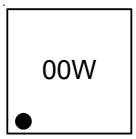
RT5789BGQUF



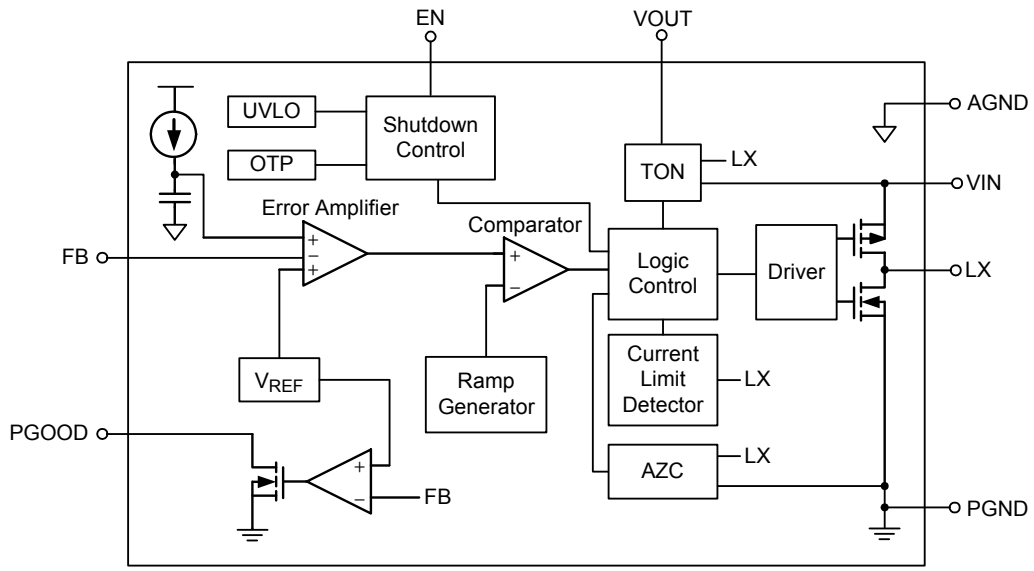
00 : Product Code

W : Date Code

Functional Pin Description

Pin No.		Pin Name	Pin Function
TSOT-23-8 (FC)	UDFN-8L 2.5x2 (FC)		
1	8	PGOOD	Open-drain power-good indication output. The power-good function is activated after soft-start is finished.
2	7	VIN	Power input. The input voltage range is from 2.5V to 6V. Connect a suitable input bypass capacitor (typically of greater than 10μF) between this pin and PGND. The bypass capacitor should be placed as close to the IC as possible.
3	6	LX	Switch node between the internal switch and the synchronous rectifier. Connect the output LC filter from this pin to the output load.
4	5	PGND	Power ground. This pin, connected to analog ground, must be soldered to a large PCB copper area for maximum power dissipation.
5	4	VOUT	Output voltage sense input. This pin is used to monitor and adjust output voltage to enhance load transient regulation.
6	3	AGND	Analog ground. It provides a ground return path for the control circuitry and internal reference. Connect AGND to a clean inner GND point with separate trace.
7	2	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at a feedback reference voltage, typically 0.6V.
8	1	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.

Functional Block Diagram



Operation

The RT5789A/B is a low-voltage, high-efficiency, synchronous step-down DC-DC converter that can deliver up to 6A output current from a 2.5V to 6V input supply. The RT5789A/B adopts ACOT® control mode, which can reduce the output capacitance and provide ultrafast transient responses, and allow minimal component sizes without any additional external compensation network. The device includes a built-in ramp voltage generator, which takes up the virtual inductor current as an input. With the internal ramp signal, the device can be compensated to achieve good stability even with low-ESR ceramic capacitors, since the need for the output capacitor's ESR to generate an ESR ramp voltage can be eliminated.

Low V_{IN} ACOT® One-Shot Operation

For a low V_{IN} ACOT® converter, a built-in error amplifier is used to keep track of the feedback voltage, as shown in the Functional Block Diagram. In steady state, the error amplifier compares the feedback voltage V_{FB} and an internal reference voltage. If the virtual inductor current ramp voltage is lower than the output of the error amplifier, a new pre-determined fixed on-time will be triggered by the on-time one-shot generator, provided that minimum-off-time one-shot is cleared and the measured inductor current through the synchronous rectifier (low-side switch) is below the current limit I_{LIM_L}. During the on-time, the high-side switch is turned on and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. If the output voltage has not reached its nominal level, another on-time, however, can only be generated after a short blanking time, or called minimum off-time, which is triggered by the minimum-off-time one-shot generator. It is to prevent another immediate on-time being triggered during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time t_{OFF_MIN} is kept short so that the inductor current can be raised up quickly by rapidly repeated on-times when needed. Such feature makes reaction speed of the ACOT®-based converters to load transients extremely fast.

Enable Control

The RT5789A/B provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{ENL}) of the enable input (EN), the converter will enter into shutdown mode, that is, the converter is disabled and switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLO}). During shutdown mode, the

supply current can be reduced to I_{SHDN} (1μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{ENH}) while the V_{IN} voltage is higher than UVLO threshold (V_{UVLO}), the device will be turned on, that is, switching being enabled and soft-start sequence being initiated.

Input Under-Voltage Lockout

In addition to the EN pin, the RT5789A/B also provides enable control through the VIN pin. It features an under-voltage lockout (UVLO) function that monitors the internal linear regulator (VCC). If V_{EN} rises above V_{ENH} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the input voltage V_{IN} goes below the UVLO falling threshold voltage ($V_{UVLO} - \Delta V_{UVLO}$), this switching will be inhibited; if V_{IN} rises above the UVLO-rising threshold (V_{UVLO}), the device will resume switching.

Over-Current Protection

The RT5789A/B is protected from over current conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET. The robust over current protection mechanism prevents the converter to be damaged from a catastrophic condition, i.e. the inductor is shorted or saturated.

High-Side MOSFET Over-Current Protection

The device senses high-side current after a deglitch time when the high-side MOSFET is turned-on. Each cycle when the sensed current is higher than the high-side switch peak current limit threshold, I_{LIM_H}, then the device enters high side over current protection. At the same time, the high-side MOSFET is turned off and the low-side MOSFET is turned on.

Low-Side MOSFET Over-Current Protection

The RT5789A/B detects low side current after a minimum-off-time while the low-side MOSFET is turned on. If the detected low-side current is higher than the low-side switch valley current limit threshold, I_{LIM_L}, the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM}). That is, another on-time can only be triggered when the inductor current goes below the low-side current limit.

If the output load current exceeds the available inductor current (clamped by the above-mentioned low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output under-voltage protection trip threshold, the IC will stop switching to avoid excessive heat.

Output Under-Voltage Protection

The RT5789A/B includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (typically 50% of the internal reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches.

Hiccup Mode

If the output under-voltage condition continues for a period of time, the RT5789A/B will enter output under-voltage protection with hiccup mode. During hiccup mode, the device remains shut down. After a period of time, a soft-start sequence for auto-recovery will be initiated. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed.

Soft-Start (SS)

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RT5789A/B provides an internal soft-start feature for inrush control. During the start-up sequence, the internal capacitor is charged by an internal current source I_{SS} to generate a soft-start ramp voltage as a reference voltage to an error amplifier. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage V_{FB} to ensure the converters have a smooth start-up. The typical soft-start time is 1.5ms.

Power Good Indication

The RT5789A/B provides a power-good (PGOOD) open-drain output pin. It is to be connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above a power-good threshold (V_{TH_PGLH}) (typically 95% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} drops by a power-good hysteresis (ΔV_{TH_PGLH}) (typically 5% of the target value) or exceeds V_{TH_PGHL} (typically 110% of the target value), the PGOOD pin will be pulled low. For V_{FB} higher than V_{TH_PGHL}, V_{PGOOD} can be pulled high again if V_{FB} drops back by a power-good hysteresis (ΔV_{TH_PGHL}) (typically 5% of the target value). Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND.

Over-Temperature Protection (Thermal Shutdown)

The RT5789A/B includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold T_{SD}. Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 7V
- LX Pin Switch Voltage ---------- –0.3V to (V_{IN} + 0.3V)
  <10ns ---------- –5V to 8.5V
- Other Pins ---------- –0.3V to (V_{IN} + 0.3V)
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings (Note 2)

- ESD Susceptibility
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 2.5V to 6V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		TSOT-23-8 (FC)	UDFN-8L 2.5x2 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	95.2	98.4	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	3.3	1.1	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	4.6	7.2	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	73.9	56.6	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	13	2.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	53.8	35.9	°C/W

Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Operating Voltage	V_{IN}		2.5	--	6	V
Under-Voltage Lockout Threshold	V_{UVLO}		2.15	2.3	2.45	
Under-Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	260	--	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	0	1	μA
Quiescent Current	I_Q	RT5789A	--	35	50	μA
		RT5789B	--	600	--	
Enable Voltage						
Enable Threshold Voltage	V_{ENH}	V_{EN} rising	1.2	--	--	V
	V_{ENL}	V_{EN} falling	--	--	0.4	
Enable Input Current	I_{IH}	V_{EN} = 2V	--	1.5	--	μA
		V_{EN} = 0V	--	0	--	
Feedback Voltage						
Feedback Input Current	I_{FB}	V_{FB} = 0.6V	--	10	--	nA
Feedback Voltage	V_{FB}		0.591	0.6	0.609	V
Current Limit						
High-Side Switch Peak Current Limit	I_{LIM_H}		--	9.7	--	A
Low-Side Switch Valley Current Limit	I_{LIM_L}		6	7.5	9.1	
Switching						
Switching Frequency	f_{SW}	V_{OUT} = 1.2V	1300	1500	1700	kHz
Minimum Off-Time	t_{OFF_MIN}		--	60	--	ns
Internal MOSFET						
High-Side On-Resistance	$R_{DS(ON)\_H}$		--	18	--	mΩ
Low-Side On-Resistance	$R_{DS(ON)\_L}$		--	16	--	
Soft-Start						
Fixed Soft-Start Time	t_{SS}		1	1.5	--	ms
V_{OUT}						
Output Discharge Resistor		(Note 5)	--	1	--	kΩ
Power Good						
Power-Good High Threshold	V_{TH_PGLH}	V_{FB} rising. PGOOD goes high	--	95	--	$\%V_{FB}$
Power-Good High Hysteresis	ΔV_{TH_PGLH}	V_{FB} falling. PGOOD goes low	--	5	--	$\%V_{FB}$
Power-Good Low Threshold	V_{TH_PGHL}	V_{FB} rising. PGOOD goes low	--	110	--	$\%V_{FB}$
Power-Good Low Hysteresis	ΔV_{TH_PGHL}	V_{FB} falling. PGOOD goes high	--	5	--	$\%V_{FB}$
Power Good Delay Time			--	15	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good Sink Current Capability		I_{PGOOD} sinks 1mA	--	--	0.4	V
Power Good Internal Pull Up Resistance			--	550	--	kΩ
Over-Temperature Protection						
Thermal Shutdown	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	30	--	

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 50mm x 55.9mm, furthermore, outer layers with 2 oz. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Typical Application Circuit

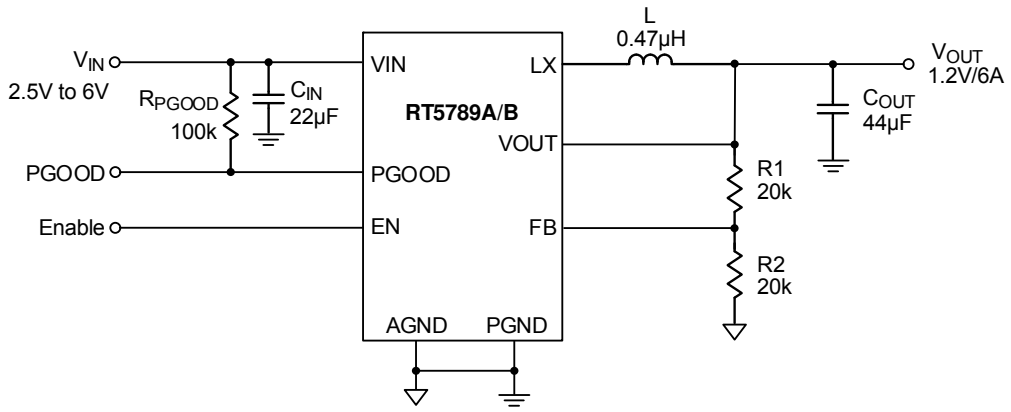


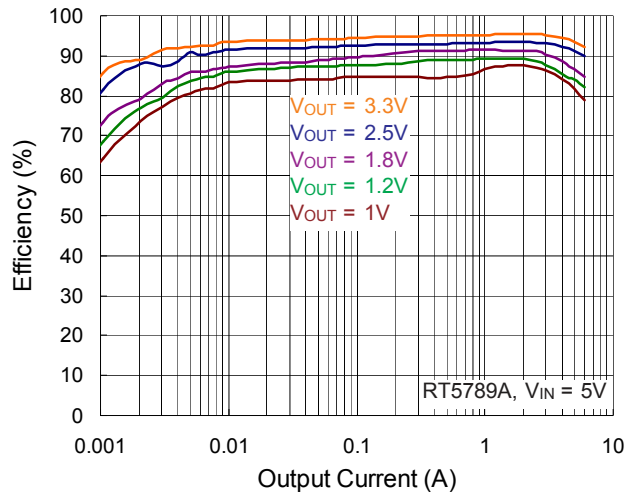
Table 1. Suggested Component Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{OUT} (µF)
0.6	0	--	0.33	66
0.8	6.7	20	0.33	66
1	13.3	20	0.33	66
1.2	20	20	0.47	44
1.8	40.2	20	0.47	44
2.5	63.4	20	0.47	44
3.3	90.9	20	0.47	44

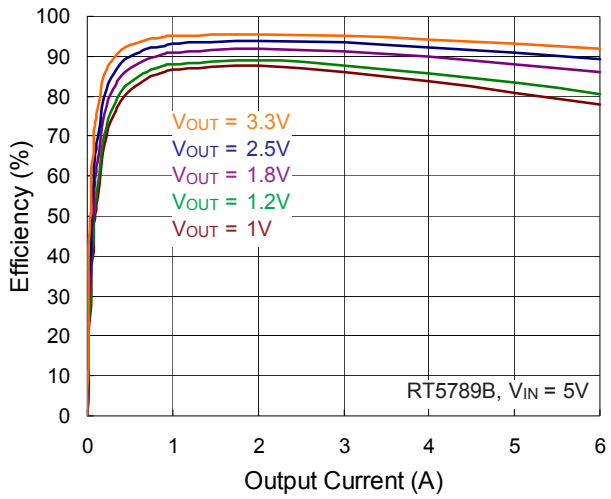
Note : All the input and output capacitances are the suggested values, which refer to the effective capacitances, and are subject to any de-rating effect, like a DC bias.

Typical Operating Characteristics

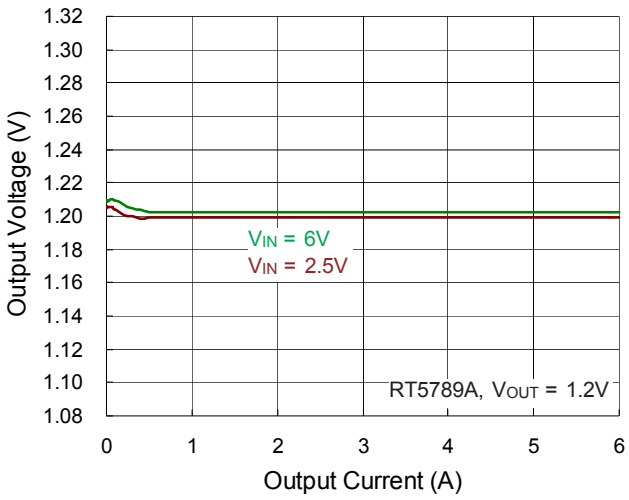
Efficiency vs. Output Current



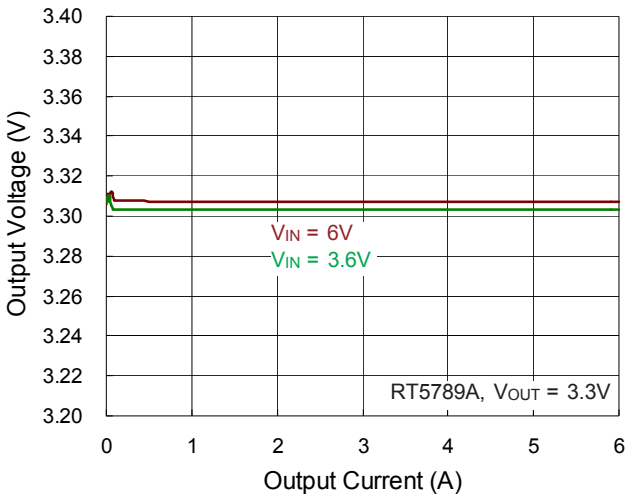
Efficiency vs. Output Current



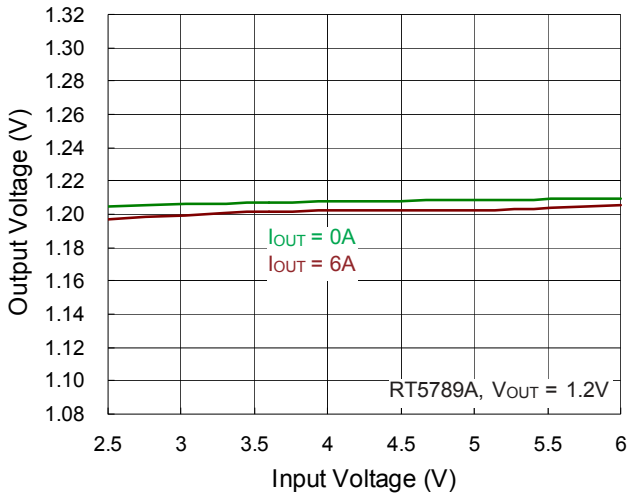
Output Voltage vs. Output Current



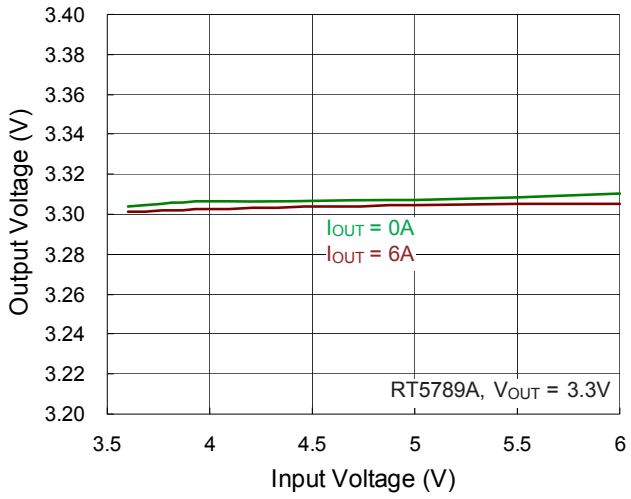
Output Voltage vs. Output Current



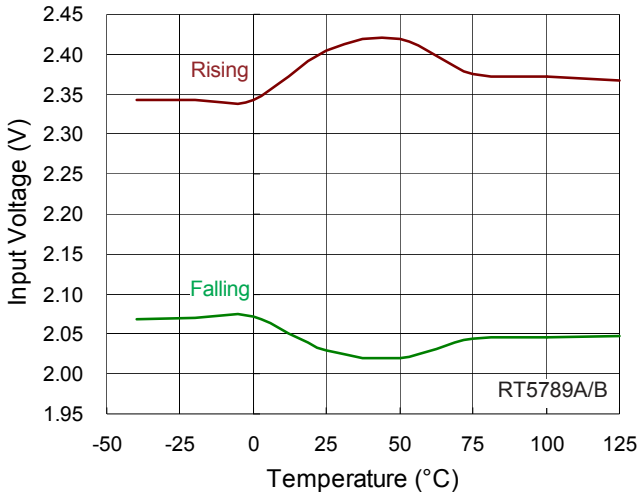
Output Voltage vs. Input Voltage



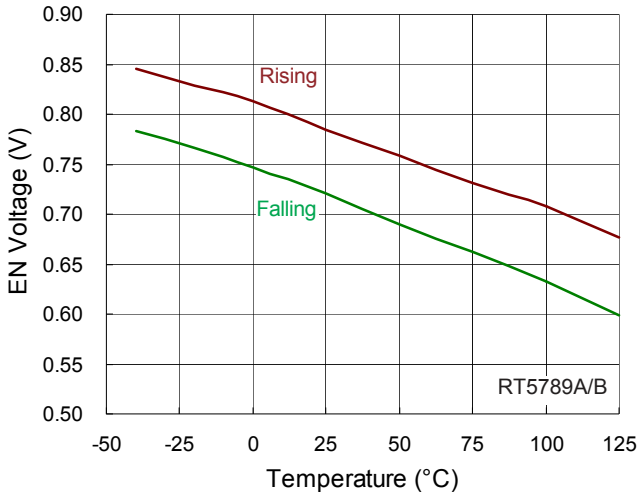
Output Voltage vs. Input Voltage



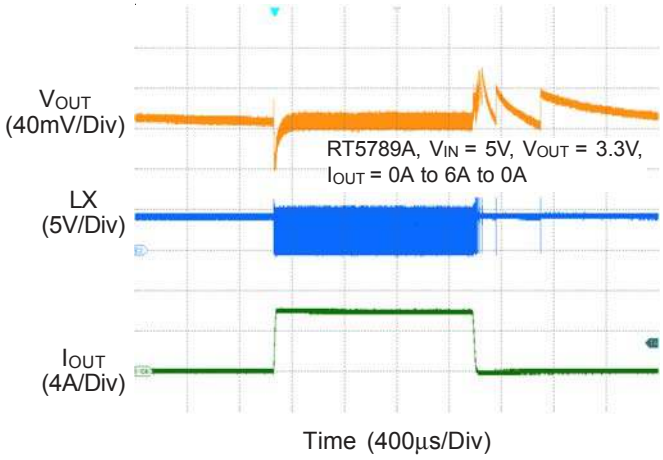
UVLO vs. Temperature



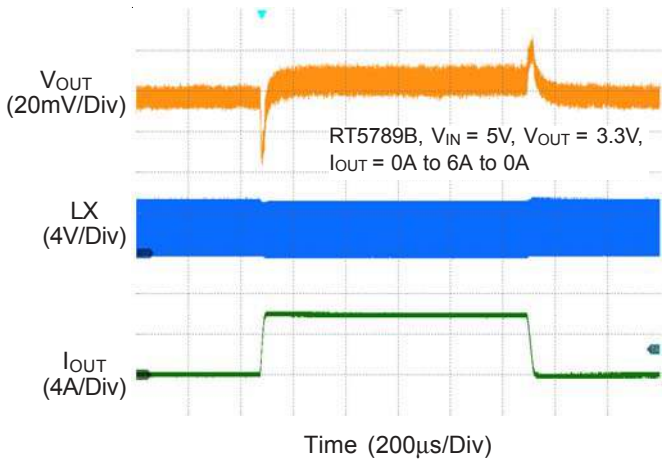
EN Voltage Threshold vs. Temperature



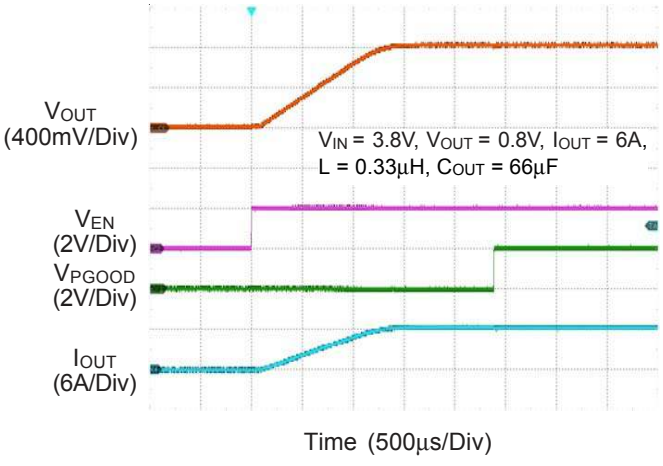
Load Transient Response



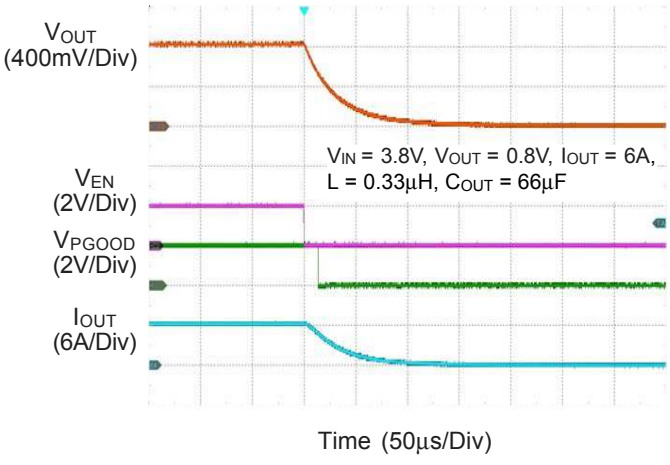
Load Transient Response



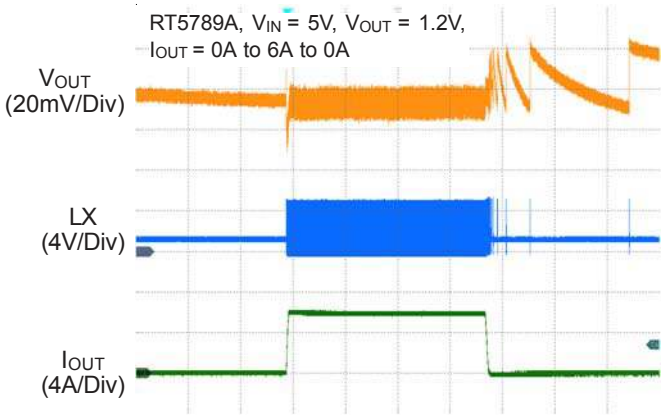
Power On from EN



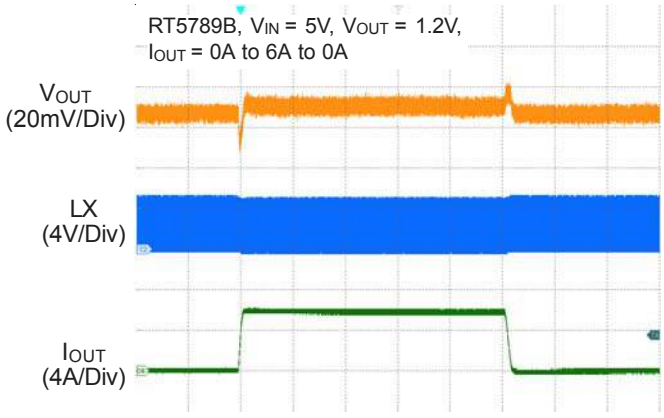
Power Off from EN



Load Transient Response



Load Transient Response



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

The output stage of a synchronous buck converter is composed of an inductor and capacitor, which stores and delivers energy to the load, and forms a second-order low-pass filter to smooth out the switch node voltage to maintain a regulated output voltage.

100% Duty-Cycle

When the input voltage drops, these Buck converters gradually increase the duty-cycle and will continuously switch-on the high side MOSFET when the input voltage drops below the regulated output voltage. This function is especially suitable in battery powered applications, and can extend application operation time when the battery is almost depleted.

Inductor Selection

When designing the output stage of the synchronous buck converter, it is recommended to start with the inductor. However, it may require several iterations because the exact inductor value is generally flexible and is optimized for low cost, small form factor, and high overall performance of the converter. Further, inductors vary with manufacturers in both material and value, and typically have a tolerance of ±20%.

Three key inductor parameters to be specified for operation with the device are inductance (L), inductor saturation current (I_{SAT}), and DC resistance (DCR), which affects performance of the output stage. An inductor with lower DCR is recommended for applications of higher peak current or load current, and it can improve system performance. Lower inductor values are beneficial to the system in physical size, cost, DCR, and transient response, but they will cause higher inductor peak current and output voltage ripple to decrease system efficiency. Conversely, higher inductor values can increase system efficiency at the expense of larger physical size, slower transient response due to the longer response time of the inductor. A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) of about 20% to 50% of the desired full output load current. To meet the inductor current ripple (ΔI_L) requirements, a minimum inductance must be chosen and the approximate inductance can be calculated by the selected input voltage, output voltage, switching frequency (f_{SW}), and inductor current ripple (ΔI_L), as below :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once the inductance is chosen, the inductor ripple current (ΔI_L) and peak inductor current (I_{L_PEAK}) can be calculated, as below :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L$$

$$I_{L\_VALLEY} = I_{OUT\_MAX} - \frac{1}{2}\Delta I_L$$

where I_{OUT_MAX} is the maximum rated output current or the required peak current.

The inductor must be selected to have a saturation current and thermal rating which exceed the required peak inductor current I_{L_PEAK}. For a robust design to maintain control of inductor current in overload or short-circuit conditions, some applications may desire inductor saturation current rating up to the high-side switch current limit of the device. However, the built-in output under-voltage protection (UVP) feature makes this unnecessary for most applications.

I_{L_PEAK} should not exceed the minimum value of the device's high-side switch current limit because the device will not be able to supply the desired output current. By reducing the inductor current ripple (ΔI_L) to increase the average inductor current (and the output current), I_{L_PEAK} can be lowered to meet the device current limit requirement.

For best efficiency, a low-loss inductor having the lowest possible DCR that still fits in the allotted dimensions will be chosen. Ferrite cores are often the best choice. However, a shielded inductor, possibly larger or more

expensive, will probably give fewer EMI and other noise problems.

The following design example is illustrated to walk through the steps to apply the equations defined above. The RT5789A/B's Typical Application Circuit for output voltage of 1.2V at maximum output current of 6A and an input voltage of 5V with inductor current ripple of 1.2A (i.e. 20%, in the recommended range of 20% to 50%, of the maximum rated output current) is taken as the design example. The approximate minimum inductor value can first be calculated as below :

$$L = \frac{1.2\times(5-1.2)}{5\times1500kHz\times1.2A} = 0.5\mu H$$

where f_{SW} is 1500kHz. The inductor current ripple will be set at 1.2A, as long as the calculated inductance of 0.5μH is used. However, the inductor of the exact inductance value may not be readily available, and therefore an inductor of a nearby value will be chosen. In this case, 0.47μH inductance is available and actually used in the Typical Application Circuit. The actual inductor current ripple (ΔI_L) and required peak inductor current (I_{L_PEAK}) can be calculated as below :

$$\Delta I_L = \frac{1.2\times(5-1.2)}{5\times1500kHz\times0.47\mu H} = 1.294A$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L = 6 + \frac{1.294}{2} = 6.647A$$

For the 0.47μH inductance value, the inductor saturation current and thermal rating should exceed 6.647A.

Input Capacitor Selection

Input capacitors are needed to smooth out the RMS ripple current (I_{RMS}) imposed by the switching currents and drawn from the input power source, by reducing the ripple voltage amplitude seen at the input of the converters. The voltage rating of the input filter capacitors must be greater than the maximum input voltage. It's also important to consider the ripple current capabilities of capacitors.

The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation :

$$I_{RMS} = I_{OUT}\times\frac{V_{OUT}}{V_{IN}}\times\sqrt{\frac{V_{IN}}{V_{OUT}}-1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. Furthermore, for a single phase buck converter, the duty cycle is approximately the ratio of output voltage to input voltage. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. The maximum I_{RMS}, as I_{RMS} (Max), can be approximated as 0.5 x I_{OUT_MAX}, where I_{OUT_MAX} is the maximum rated output current. Besides, the variation of the capacitance value with temperature, DC bias voltage, switching frequency, and allowable peal-to-peak ripple voltage that reflects back to the input, also need to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases; also, higher switching frequency allows the use of input capacitors of smaller capacitance values.

Ceramic capacitors are most commonly used to be placed right at the input of the converter to reduce ripple voltage amplitude because only ceramic capacitors have extremely low ESR which is required to reduce the ripple voltage. Note that the capacitors need to be placed as close as to the input pins as possible for highest effectiveness. Ceramic capacitors are preferred also due to their low cost, small size, high RMS current ratings, robust inrush surge current capabilities, and low parasitic inductance, which helps reduce the high-frequency ringing on the input supply.

However, care must be taken when ceramic capacitors are used at the input, and the input power is supplied by a wall adapter, connected through a long and thin wire. When a load step occurs at the output, a sudden inrush current will surge through the long inductive wire, which can induce ringing at the device's power input and potentially cause a very large voltage spike at the VIN pin to damage the device. For applications where the input power is located far from the device input, it may be required that the low-ESR ceramic input capacitors be placed in parallel with a bulk capacitor of other types, such as tantalum, electrolytic, or polymer, to dampen the voltage ringing and overshoot at the input, caused by the long input power path and input ceramic capacitor.

It is suggested to choose capacitors with higher

temperature ratings than required. Several ceramic capacitors may be parallel to meet application requirements, such as the RMS current, size, and height. The Typical Application Circuit can use one 22μF, or two 10μF and one high-frequency-noise-filtering 0.1μF low-ESR ceramic capacitors at the input.

Output Capacitor Selection :

Output capacitance affects the output voltage of the converter, the response time of the output feedback loop, and the requirements for output voltage sag and soar. The sag occurs after a sudden load step current applied, and the soar occurs after a sudden load removal. Increasing the output capacitance reduces the output voltage ripple and output sag and soar, while it increases the response time that the output voltage feedback loop takes to respond to step loads, Therefore, there is a tradeoff between output capacitance and output response. It is recommended to choose a minimum output capacitance to meet the output voltage requirements of the converter, and have a quick transient response to step loads.

The ESR of the output capacitor affects the damping of the output filter and the transient response. In general, low-ESR capacitors are good choices due to their excellent capability in energy storage and transient performance. The RT5789A/B, therefore, is specially optimized for ceramic capacitors. Consider also DC bias and aging effects while selecting the output capacitor.

- **Output Voltage Ripple**

  The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor with capacitance, C_{OUT}, and its equivalent series resistance, R_{ESR}, must be taken into consideration. The output peak-to-peak ripple voltage ΔV_{P-P}, caused by the inductor current ripple ΔI_L, is characterized by two components, which are ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, can be expressed as below :

$$\Delta V_{P-P} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

If ceramic capacitors are used as the output capacitors, both the components need to be considered due to the extremely low ESR and relatively small capacitance.

For the RT5789A/B's Typical Application Circuit for output voltage of 1.2V, and actual inductor current ripple (ΔI_L) of 1.294A, using two paralleled 22μF ceramic capacitors with ESR of about 5mΩ as output capacitors, the two output ripple components are as below :

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR} = 1.294A \times 5m\Omega = 6.47mV$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} = \frac{1.294A}{8 \times 44\mu F \times 1500kHz} = 2.451mV$$

$$\Delta V_{P-P} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C} = 8.921mV$$

- **Output Transient Undershoot and Overshoot**

  In addition to the output voltage ripple at the switching frequency, the output capacitor and its ESR also affect output voltage sag, which is undershoot on a positive load step, and output voltage soar, which is overshoot on a negative load step. With the built-in ACOT® architecture, the IC can have very fast transient responses to the load steps and small output transients.

  However, the combination of a small ceramic output capacitor (that is, of little capacitance) and a low output voltage (that is, only little charge stored in the output capacitor), used in low-duty-cycle applications (which require high inductance to get reasonable ripple currents for high input voltages), causes an increase in the size of voltage variations (i.e. sag/soar) in response to very quick load changes. Typically, the load changes slowly, compared with the IC's switching frequency. However, for present-day applications, more and more digital blocks may exhibit nearly instantaneous large transient load changes. Therefore, in the following section, how to calculate the worst-case voltage swings in response to very fast load steps will be explained in details.

  Both of the output transient undershoot and overshoot have two components : a voltage step caused by the output capacitor's ESR, and a voltage sag or soar due to the finite output capacitance and the inductor current slew rate. The following formulas can be used to check if the ESR is low enough (which is usually not a problem with ceramic capacitors) and if the output capacitance

is large enough to prevent excessive sag or soar on very fast load steps, with the chosen inductor value.

The voltage step (ΔV_{OUT_ESR}) caused by the ESR is a function of the load step (ΔI_{OUT}) and the ESR (R_{ESR}) of the output capacitor, described as below :

$$\Delta V_{OUT\_ESR} = \Delta I_{OUT} \times R_{ESR}$$

The voltage amplitude (ΔV_{OUT_SAG}) of the capacitive sag is a function of the load step (ΔI_{OUT}), the output capacitor value (C_{OUT}), the inductor value (L), the input-to-output voltage differential, and the maximum duty cycle (D_{MAX}). And, the maximum duty cycle during a fast transient can be determined by the on-time (t_{ON}) and the minimum off-time (t_{OFF_MIN}) since the ACOT® control scheme will ramp the current during on-times, which are spaced apart by a minimum off-time, that is, as fast as allowed. The approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage can be calculated according to the following equations :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

Note the actual on-time will be slightly larger than the calculated one as the IC will automatically adapt to compensate the internal voltage drops, such as the voltage across high-side switch due to on-resistance. However, both of these can be neglected since the on-time increase can compensate for the voltage drops. The output voltage sag (ΔV_{OUT_SAG}) can then be calculated as below :

$$\Delta V_{OUT\_SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The voltage amplitude of the capacitive soar is a function of the load step (ΔI_{OUT}), the output capacitor value (C_{OUT}), the inductor value (L), and the output voltage (V_{OUT}). And the output voltage soar (ΔV_{OUT_SOAR}) can be calculated as below :

$$\Delta V_{OUT\_SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with high-voltage rating, can be connected to the input supply V_{IN}, either directly or through a 100kΩ resistor. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 1, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins.

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 2. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when VIN is smaller than the VOUT target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input under-voltage lockout threshold, as shown in Figure 3.

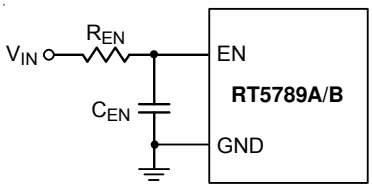


Figure 1. Enable Timing Control

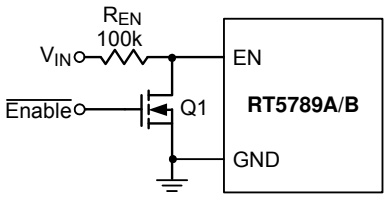


Figure 2. Logic Control for the EN Pin

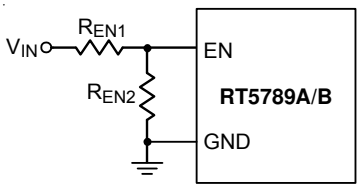


Figure 3. Resistor Divider for Under-Voltage Lockout Threshold Setting

Output Voltage Setting

The output voltage can be programmed by a resistive divider from the output to ground with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 4. The output voltage is set according to the following equation :

$$V_{OUT} = V_{TH\_FB} \times (1 + \frac{R1}{R2})$$

where V_{TH_FB} is around 0.6V (Typ).

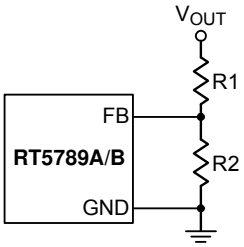


Figure 4. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 is suggested between 10kΩ and 100kΩ to minimize power consumption and noise pick-up at the FB pin. Once R2 is chosen, the resistance of R1 can then be obtained as below :

$$R1 = \frac{R2 \times (V_{OUT} - V_{TH\_FB})}{V_{TH\_FB}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used.

Power-Good Output

The PGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal V_{FB}. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over. If V_{FB} raises above a power-good threshold (V_{TH_PGLH}) (typically 95% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} drops by a power-good hysteresis (ΔV_{TH_PGLH}) (typically 5% of the target value) or exceeds V_{TH_PGHL} (typically 110% of the target value), the PGOOD pin will be pulled low. For V_{FB} above V_{TH_PGHL}, V_{PGOOD} will be pulled high again when V_{FB} drops back by a power-good hysteresis (ΔV_{TH_PGHL}) (typically 5% of the target value). Once being started-up, if any internal protection is triggered, PGOOD will be pulled low to GND.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and $\theta_{JA(EVB)}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a TSOT-23-8 (FC) package, the thermal resistance, $\theta_{JA(EVB)}$, is 73.9°C/W on a four-layer Richtek Evaluation Board. For a UDFN-8L 2.5x2 (FC) package, the thermal resistance, $\theta_{JA(EVB)}$, is 56.6°C/W on a four-layer Richtek Evaluation Board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (73.9°C/W) = 1.35W for a TSOT-23-8 (FC) package.

$P_{D(MAX)}$ = (125°C – 25°C) / (56.6°C/W) = 1.77W for a UDFN-8L 2.5x2 (FC) (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

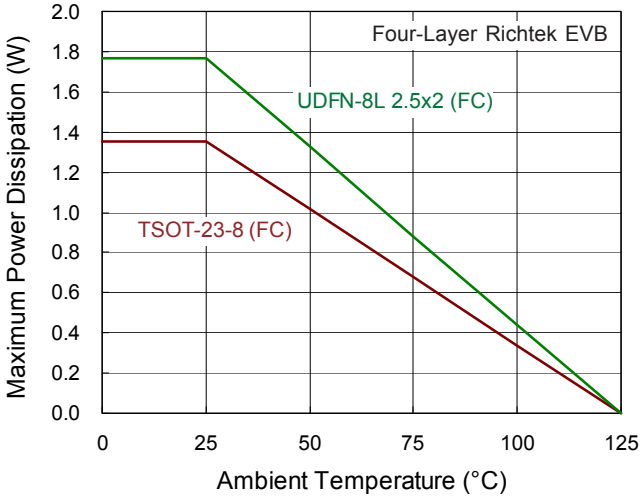


Figure 5. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout. Certain points must be considered before starting a layout using the IC.

- Make traces of the high current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- The LX node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the LX node to prevent stray as possible.
- The GND pin should be connected to a strong ground plane for heat sinking and noise protection.
- Avoid using vias in the power path connections that have switched currents (from C_{IN} to GND and C_{IN} to VIN) and the switching node (LX).

An TSOT-23-8 (FC)example of PCB layout guide is shown in Figure 6 for reference.

An UDFN-8L 2.5x2 (FC) example of PCB latout guide is shown in Figure 7 for reference.

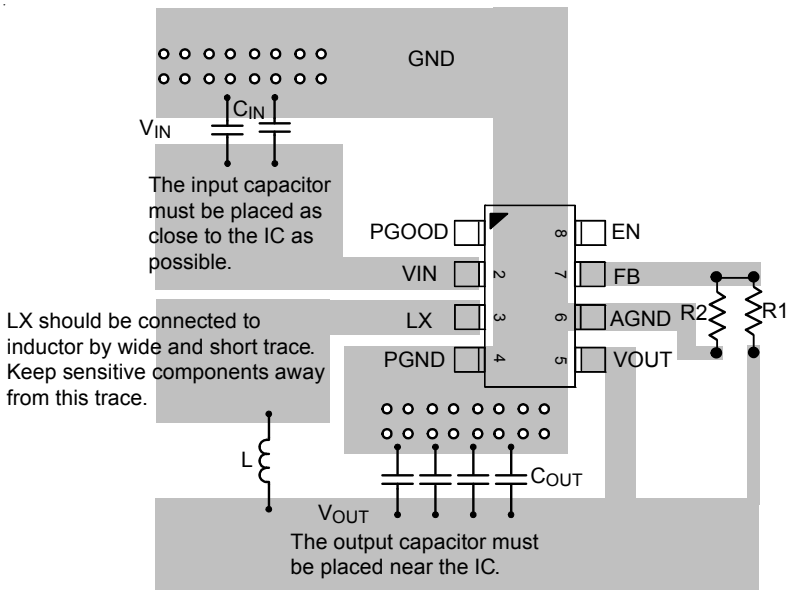


Figure 6. TSOT-23-8 (FC) PCB Layout Guide

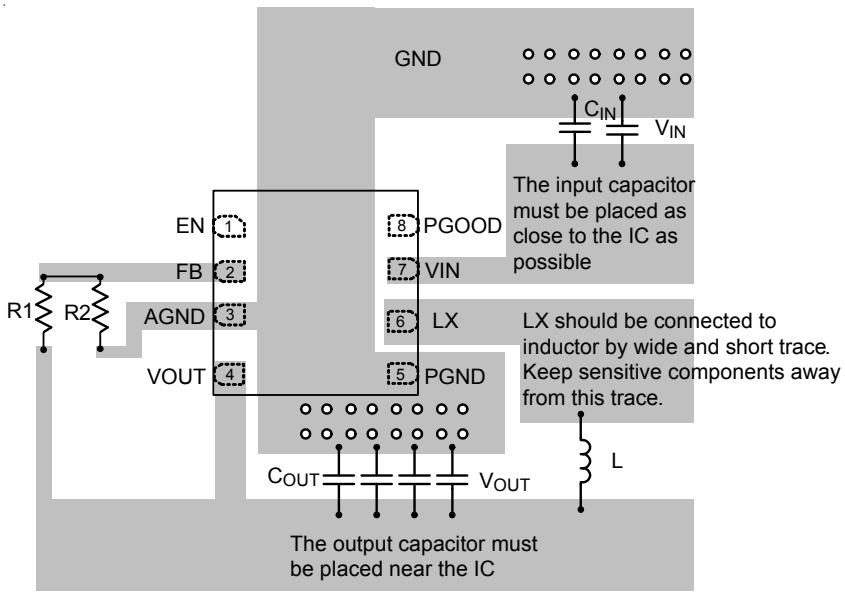
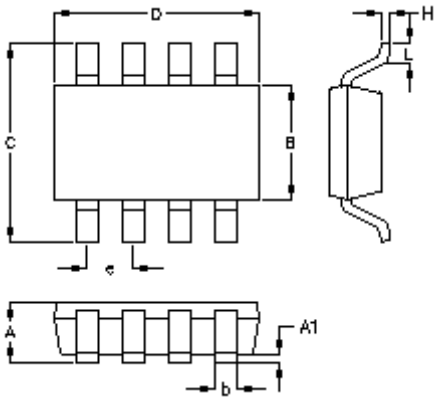


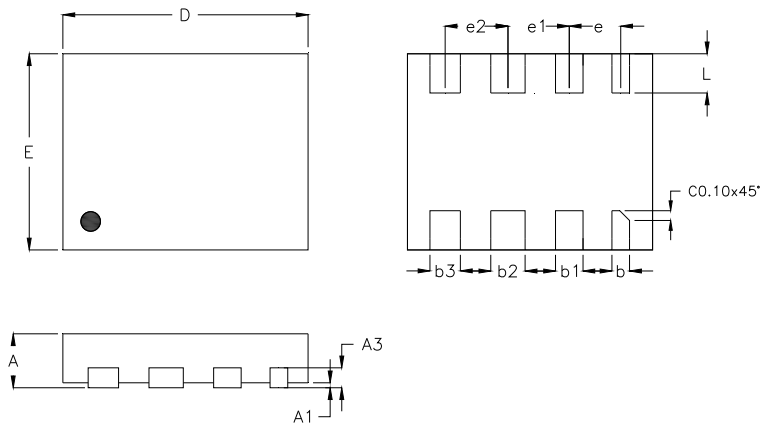
Figure 7. UDFN-8L 2.5x2 (FC) PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.220	0.380	0.009	0.015
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.585	0.715	0.023	0.028
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-8 (FC) Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.152	0.004	0.006
b	0.150	0.250	0.006	0.010
b1	0.250	0.350	0.010	0.014
b2	0.320	0.420	0.013	0.017
b3	0.280	0.380	0.011	0.015
D	2.450	2.550	0.096	0.100
E	1.950	2.050	0.077	0.081
e	0.525		0.021	
e1	0.625		0.025	
e2	0.640		0.025	
L	0.350	0.450	0.014	0.018

U-Type 8L DFN 2.5x2 (FC) Package

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Datasheet Revision History

Version	Date	Description	Item
05	2023/2/6	Modify	Simplified Application Circuit on P1 Absolute Maximum Ratings on P6 ESD Ratings on P6 Thermal Information on P6 Typical Application Circuit on P10 Typical Operating Characteristics on P12 Application Information on P14, 18