NX5DV4885E

Dual supply 1-of-2 VGA switch

Rev. 2 — 4 November 2011 Product data sheet

1. General description

The NX5DV4885E is a dual supply 1-to-2 VGA switch. It integrates high-bandwidth SPDT switches with level translating switches and level translating buffers to provide switching of input RGB signals and switching and level translation of input DDC signals to either of two output channels as well as level translation of input H-sync and V-sync signals

The NX5DV4885E is characterized for operation from −40 °C to +85 °C.

2. Features and benefits

- RGB switches:
  - Low ON resistance (4 Ω typical)
  - Low ON capacitance (12 pF typical)
  - Low output skew (50 ps)
- Low power consumption (< 2 μA)
- Level translation of sync and DDC signals
- Over-voltage tolerant inputs
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 4 kV
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101D exceeds 1000 V
  - IEC61000-4-2 contact discharge exceeds 4 kV for I/Os
- Latch-up performance exceeds 100 mA per JESD78 Class II Level A
- Specified from −40 °C to +85 °C

3. Applications

- Notebook Computers
- Docking stations
- Digital projectors
- Computer monitors
- Servers
- Storage

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX5DV4885EHF	−40 °C to +85 °C	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3

5. Marking

Table 2. Marking codes

Type number	Marking[1]
NX5DV4885EHF	x5E

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

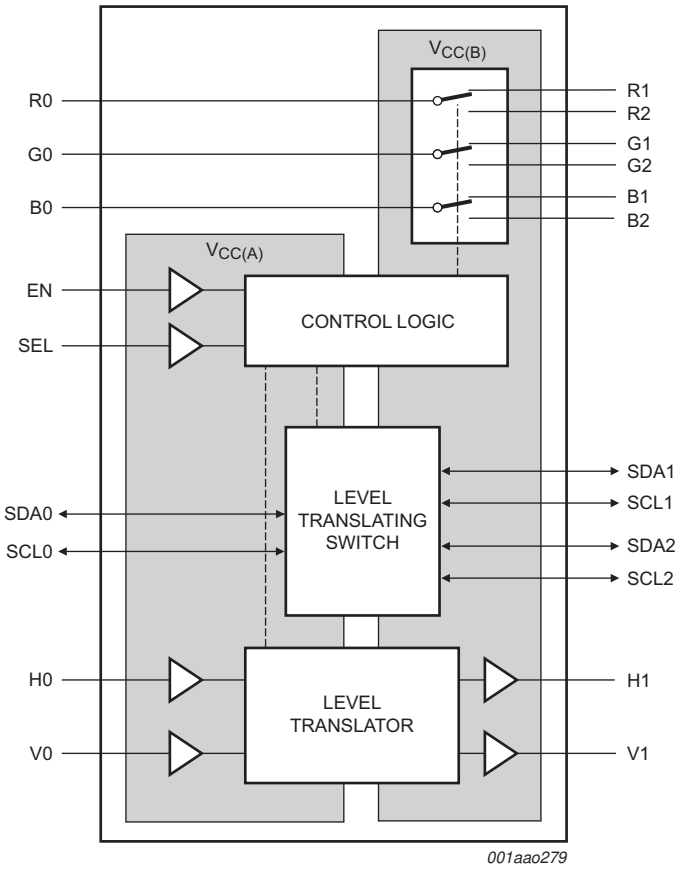
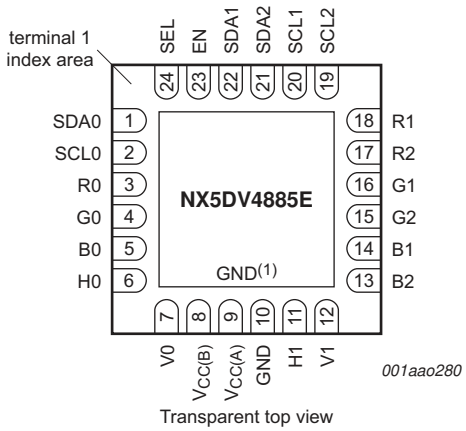


Fig 1. Logic symbol

7. Pinning information

7.1 Pinning



(1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad however if it is soldered the solder land should remain floating or be connected to GND.

Fig 2. Pin configuration SOT616-3 (HVQFN24)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
R0, G0, B0	3, 4, 5	RGB input or output
GND	10	ground (0 V)
$V_{CC(A)}$	9	supply voltage A
H0	6	horizontal sync input
V0	7	vertical sync input
EN	23	enable input (active HIGH)
SDA0	1	SDA0 input or output
SCL0	2	SCL0 input or output
SDA1, SDA2	22, 21	SDA input or output
SCL1, SCL2	20, 19	SCL input or output
$V_{CC(B)}$	8	supply voltage B
V1	12	vertical sync output
H1	11	horizontal sync output
R1, G1, B1, R2, G2, B2	18, 16, 14, 17, 15, 13	RGB input or output
SEL	24	select input

8. Functional description

The NX5DV4885E integrates high-bandwidth SPDT switches, level-translating buffers and level translating SPDT switches to provide a complete solution for 1-to-2 switching of VGA signals. An enable input (EN) is used to enable or disable the device and a select input (SEL) is used to determine which output is selected. When EN = LOW the device is disabled; all switches will be off and H1, V1 will be forced LOW.

8.1 RGB switches

The NX5DV4885E provides three identical single pole double throw high-bandwidth switches to route standard VGA RGB signals (see Table 4).

Table 4. Function table RGB

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Input		Switch
EN	**SEL**	
H	L	R0 to R1; G0 to G1; B0 to B1
H	H	R0 to R2; G0 to G2; B0 to B2
L	X	switches Rn, Gn, Bn off

8.2 H-Sync/V-Sync level translator

The horizontal and vertical synchronization buffers have inputs (H0, V0) referenced to $V_{CC(A)}$ and outputs (H1 and V1) that are referenced to $V_{CC(B)}$. This allows level translation of synchronization signals from as low as 2.0 V up to 5.5 V and supports low-voltage CMOS or TTL-compatible graphics controllers meeting the VESA specification for output drive of ±8 mA. The EN input also controls the level shifter (See Table 5).

Table 5. Function table HV

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Input	Switch
EN	
H	H1 = H0; V1 = V0
L	H1, V1 = L

8.3 Display-Data Channel Multiplexer

The NX5DV4885E provides two identical SPDT active-level translating switches to route DDC signals (See Table 6). The switch outputs are limited to a diode drop below the voltage applied on $V_{CC(A)}$. To provide VESA I^2C-compatible signals 3.3 V should be applied to $V_{CC(A)}$. If voltage translation is not required $V_{CC(A)}$ should be connected to $V_{CC(B)}$.

Table 6. Function table DDC

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Input		Switch
EN	**SEL**	
H	L	SDA0 to SDA1, SCL0 to SCL1
H	H	SDA0 to SDA2, SCL0 to SCL2
L	X	switches SDAn, SCLn off

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			−0.5	+6	V
$V_{CC(B)}$	supply voltage B			−0.5	+6	V
V_I	input voltage		[1]	−0.5	+6	V
V_{SW}	switch voltage		[1]	−0.5	+6	V
I_{IK}	input clamping current	$V_I < -0.5$ V		−50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V		−50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		−50	-	mA
I_O	output current	$V_O = 0$ V to $V_{CC(B)}$		-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			−100	-	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V or $V_{SW} < 6$ V; source or sink current		-	±30	mA
		$V_{SW} > -0.5$ V or $V_{SW} < 6$ V; pulsed at 1 ms duration, < 10 % duty cycle; peak current		-	±90	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	[2]	-	300	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For HVQFN24 package: above 134.5 °C the value of P_{tot} derates linearly with 19.3 mW/K.

10. Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{CC(A)}$	supply voltage A			2	3.3	5.5	V
$V_{CC(B)}$	supply voltage B			4.5	5.0	5.5	V
T_{amb}	ambient temperature	operating in free-air		−40	+25	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC(A)}$ = 2.3 V to 2.7 V	[1]	-	20	-	ns/V
		$V_{CC(A)}$ = 3 V to 3.6 V	[1]	-	10	-	ns/V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	[1]	-	5	-	ns/V

[1] Applies to control signal levels.

11. Static characteristics

Table 9. Static characteristics

$V_{CC(B)}$ = 4.5 V to 5.5 V; $V_{CC(A)}$ = 2 V to 5.5 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		T_{amb} = −40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
General							
$I_{CC(A)}$	supply current A	$V_{CC(A)}$ = 3.3 V; EN = $V_{CC(A)}$ or GND; for H1, V1: I_O = 0 A		-	-	2.0	μA
$I_{CC(B)}$	supply current B	$V_{CC(B)}$ = 5.0 V; EN = $V_{CC(A)}$ or GND; for H1, V1: I_O = 0 A		-	-	2.0	μA
HV buffer							
V_{IH}	HIGH-level input voltage	$V_{CC(A)}$ = 3 V to 3.6 V		2	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC(A)}$ = 3 V to 3.6 V		-	-	0.8	V
V_H	hysteresis voltage			-	50	-	mV
I_I	input leakage current	$V_{CC(B)}$ = $V_{CC(A)}$ = 5.5 V; V_I = GND to $V_{CC(A)}$		-	-	±1	μA
V_{OH}	HIGH-level output voltage	I_O = −8 mA		$V_{CC(B)}$ − 0.5	-	-	V
V_{OL}	LOW-level output voltage	I_O = 8 mA		-	-	0.5	V
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 5.5 V		-	-	±1	μA
RGB switches							
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC(B)}$ = 5.5 V; V_I = 0.3 V or 5.5 V; V_O = 0 V to $V_{CC(B)}$; EN = $V_{CC(A)}$ or GND; See Figure 3		-	-	±1	μA
$I_{S(ON)}$	ON-state leakage current	$V_{CC(B)}$ = 5.5 V; V_I = 0.3 V or 5.5 V; V_O = 0 V to $V_{CC(B)}$; EN = $V_{CC(A)}$; See Figure 4		-	-	±1	μA
R_{ON}	ON resistance	V_I = 0.7 V; I_{SW} = −10 mA; See Figure 5 and Figure 6	[4]	-	4	-	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = GND to 0.7 V; I_{SW} = −10 mA	[2]	-	0.5	-	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_I = GND to 0.7 V; I_{SW} = −10 mA	[3]	-	0.5	-	Ω

Table 9. Static characteristics *...continued*

$V_{CC(B)}$ = 4.5 V to 5.5 V; $V_{CC(A)}$ = 2 V to 5.5 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
$C_{S(OFF)}$	OFF-state capacitance			-	4.5	-	pF
$C_{S(ON)}$	ON-state capacitance			-	12	-	pF
SDA, SCL							
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC(B)}$ = 5.5 V; $V_{CC(A)}$ = 3.6 V; SCL0, SDA0, SCL1, SCL2, SDA1, SDA2 = $V_{CC(A)}$ or GND; V_O = 0 V to $V_{CC(B)}$; EN = GND; See Figure 3	[5]	-	-	±1	μA
R_{ON}	ON resistance	$V_{CC(A)}$ = 2 V; V_I = 0.4 V; I_{SW} = ±2 mA; See Figure 5 and Figure 7		-	9	-	Ω
$C_{S(ON)}$	ON-state capacitance			-	15	-	pF
Control Logic (SEL, EN)							
V_{IH}	HIGH-level input voltage	$V_{CC(A)}$ = 2.3 V to 2.7 V		1.7	-		V
		$V_{CC(A)}$ = 3.0 V to 3.6 V		2.0	-		V
		$V_{CC(A)}$ = 4.5 V to 5.5 V		$0.7V_{CC(A)}$	-		V
V_{IL}	LOW-level input voltage	$V_{CC(A)}$ = 2.3 V to 2.7 V		-	-	0.7	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V		-	-	0.8	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V		-	-	$0.3V_{CC(A)}$	V
V_H	hysteresis voltage			-	50	-	mV
I_I	input leakage current	$V_{CC(A)}$ = 5.5 V; V_I = GND to $V_{CC(A)}$		-	-	±1	μA

[1] All typical values are measured at $V_{CC(B)}$ = 5 V, $V_{CC(A)}$ = 3.3 V and T_{amb} = 25 °C unless otherwise specified.

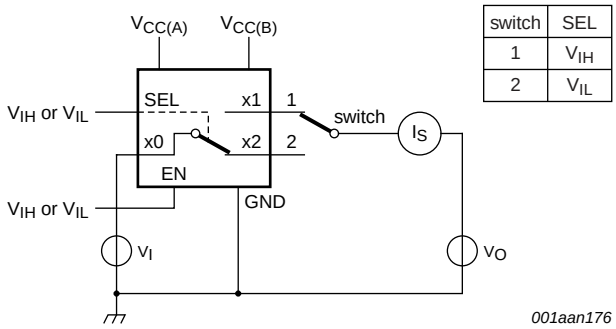
[2] Measured at identical V_{CC}, temperature and input voltage.

[3] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

[4] Guarantees the LOW level.

[5] Guarantees the HIGH level.

11.1 Test circuits and waveforms



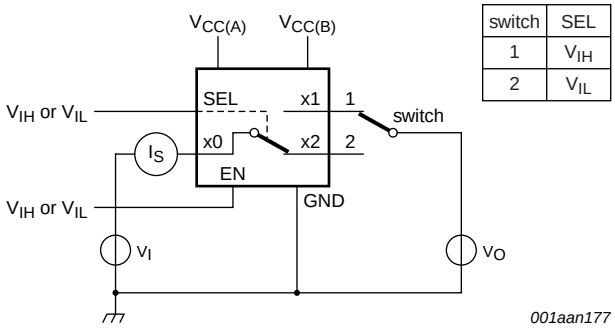
switch	SEL
1	V_{IH}
2	V_{IL}

x0 refers to R0, G0, B0, SCL0 or SDA0

x1 refers to R1, G1, B1, SCL1 or SDA1

x2 refers to R2, G2, B2, SCL2 or SDA2

Fig 3. Test circuit for measuring OFF-state leakage current



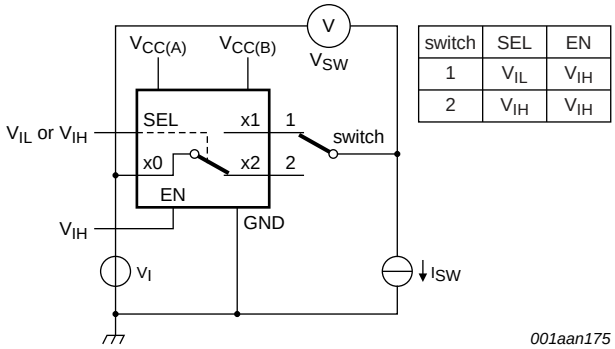
switch	SEL
1	V_{IH}
2	V_{IL}

x0 refers to R0, G0, B0, SCL0 or SDA0

x1 refers to R1, G1, B1, SCL1 or SDA1

x2 refers to R2, G2, B2, SCL2 or SDA2

Fig 4. Test circuit for measuring ON-state leakage current



switch	SEL	EN
1	V_{IL}	V_{IH}
2	V_{IH}	V_{IH}

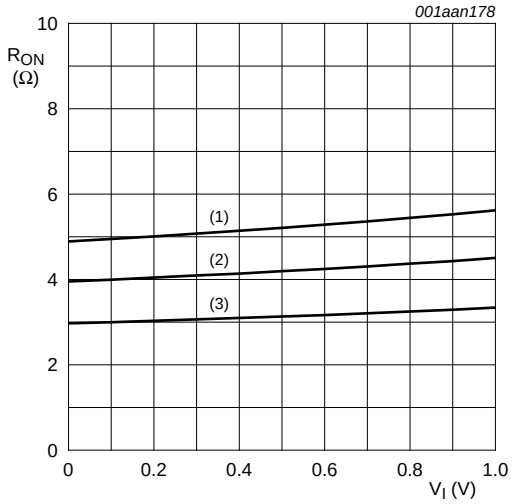
x0 refers to R0, G0, B0, SCL0 or SDA0

x1 refers to R1, G1, B1, SCL1 or SDA1

x2 refers to R2, G2, B2, SCL2 or SDA2

$R_{ON} = V_{SW} / I_{SW}$.

Fig 5. Test circuit for measuring ON resistance

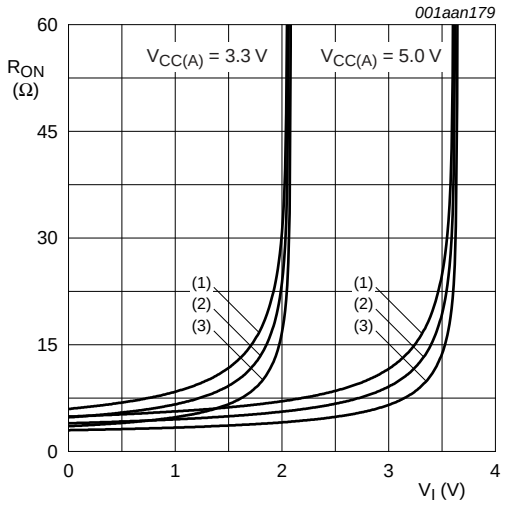


(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40°C

Fig 6. ON resistance as a function of input voltage (RGB switches)



(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40°C

Fig 7. ON resistance as a function of input voltage (DDC switches)

12. Dynamic characteristics

Table 10. Dynamic characteristics

At recommended operating conditions; Voltages are referenced to GND (ground = 0 V; $V_{CC(B)}$ = 4.5 V to 5.5 V; $V_{CC(A)}$ = 2 V to 5.5 V.

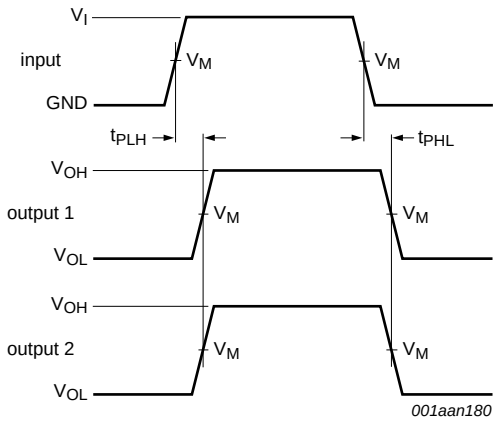
Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
t_{pd}	propagation delay	H0 to H1 and V0 to V1; See Figure 8 and Figure 9	[2]	-	3	-	ns
t_{en}	enable time	EN and SEL to all other outputs; See Figure 10 and Figure 11		-	15	-	ns
t_{dis}	disable time	EN and SEL to all other outputs; See Figure 10 and Figure 11		-	5	-	ns
t_{b-m}	break-before-make time	See Figure 12		-	10	-	ns
$t_{sk(o)}$	output skew time	Skew between any Rn, Gn and Bn ports; see Figure 8	[3]	-	50	-	ps

[1] All typical values are measured at $V_{CC(B)}$ = 5 V; $V_{CC(A)}$ = 3.3 V; T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Guaranteed by design.

12.1 Test circuits and waveforms



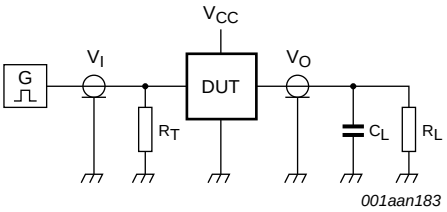
Measurement points are given in Table 11.

$t_{sk(o)} = |t_{PLH1} - t_{PLH2}|$.

Fig 8. Test circuit for measuring propagation delay times

Table 11. Measurement points

Input		Output	
V_M	V_I	V_X	V_M
$0.5V_{CC(A)}$	GND to $V_{CC(A)}$	$0.9V_{OH}$	$0.5V_{CC(B)}$



Test data is given in Table 12.

Definitions:

DUT = Device Under Test.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

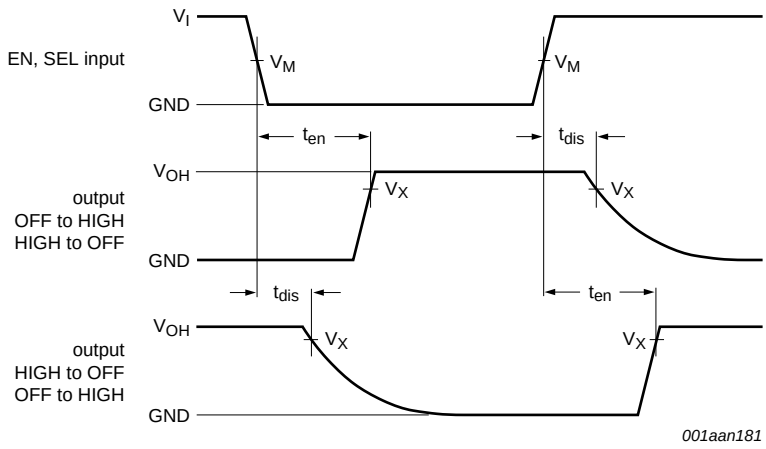
C_L = Load capacitance including test jig and probe.

R_L = Load resistance.

Fig 9. Test circuit for measuring propagation delay times

Table 12. Test data

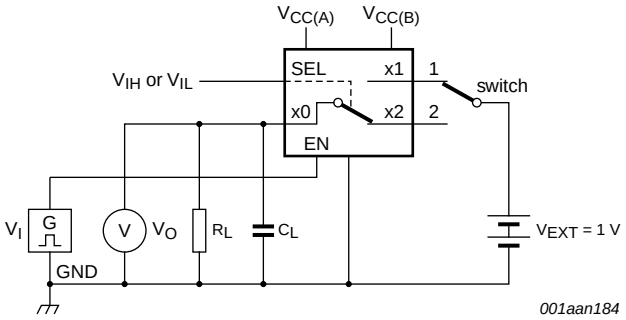
Input	Load	
t_r, t_f	C_L	R_L
≤ 2.5 ns	10 pF	1 kΩ



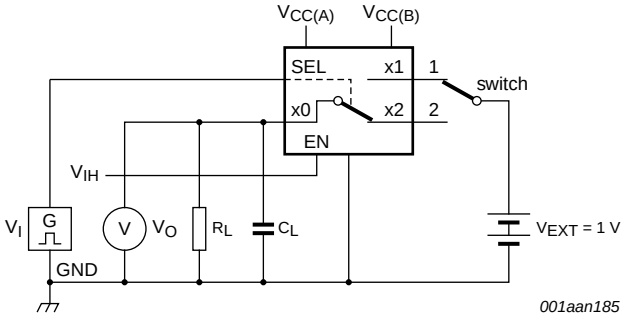
Measurement points are given in Table 11.

Logic level: V_{OH} is typical output voltage level that occurs with the output load.

Fig 10. Enable and disable times



a. EN to switch outputs



b. SEL to switch outputs

Test data is given in Table 13.

x0 refers to R0, G0, B0, SCL0 or SDA0

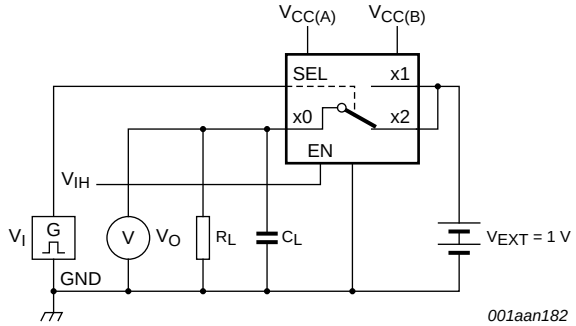
x1 refers to R1, G1, B1, SCL1 or SDA1

x2 refers to R2, G2, B2, SCL2 or SDA2

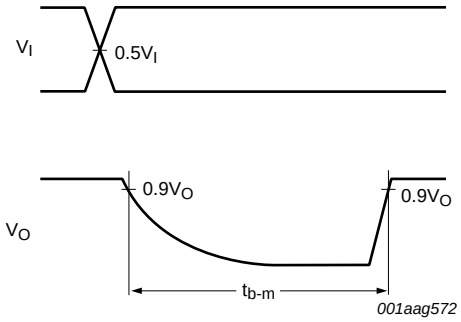
Fig 11. Test circuit for measuring enable and disable times

Table 13. Test data

Input		Load	
t_r, t_f	V_I	C_L	R_L
≤ 2.5 ns	GND to $V_{CC(A)}$	10 pF	100 Ω



a. Test circuit



b. Input and output measurement points

Test data is given in Table 13.

x0 refers to R0, G0, B0, SCL0 or SDA0

x1 refers to R1, G1, B1, SCL1 or SDA1

x2 refers to R2, G2, B2, SCL2 or SDA2

Fig 12. Test circuit for measuring break-before-make timing

13. Additional dynamic characteristics

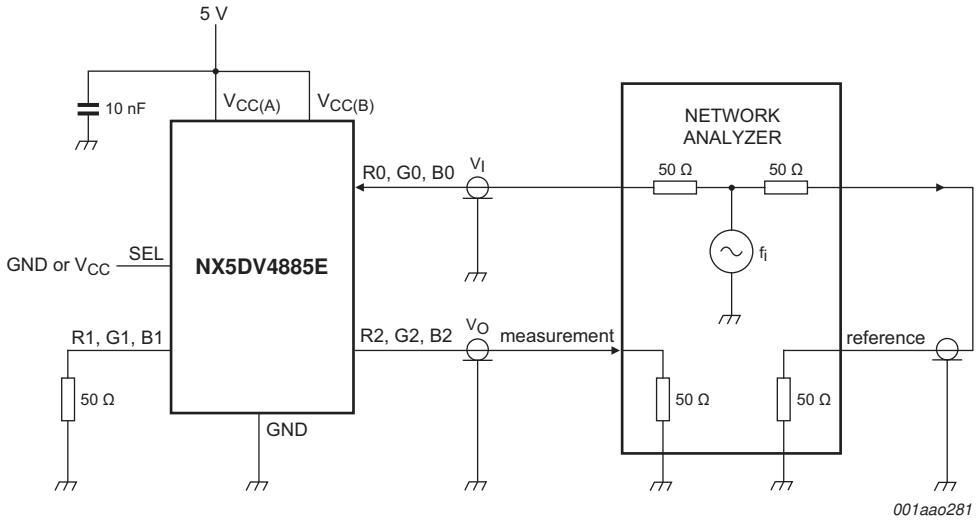
Table 14. Additional dynamic characteristics

$V_{CC(B)}$ = 5.0 V ± 10 %, $V_{CC(A)}$ = 2 V to 5.5 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			Unit
				Min	Typ	Max	
$f_{(-3dB)}$	–3 dB frequency response	R_L = 50 Ω; see Figure 13	[1]	-	850	-	MHz
α_{ins}	Insertion loss	f_i = 1 MHz; R_L = R_S = 50 Ω; see Figure 13		-	0.6	-	dB
Xtalk	crosstalk	between switches; f_i = 50 MHz; R_L = 50 Ω; see Figure 13	[1]	-	–50	-	dB

[1] f_i is biased at $0.5V_{CC}$.

13.1 Test circuits



Insertion loss is measured between R0 and R1 or R2 on each switch; crosstalk is measured from one channel to the other channel.

Fig 13. Test circuit for measuring crosstalk and insertion loss

14. Application information

The NX5DV4885E provides the level shifting necessary to drive two standard VGA ports from a graphic controller as low as 2.2 V. Internal buffers drive the HSYNC and VSYNC signals to VGA standard TTL levels. The DDC multiplexer provides level shifting by clamping signals to a diode drop below the voltage applied on $V_{CC(A)}$ (See figure Figure 14). Connect $V_{CC(A)}$ to 3.3 V for normal operation, or to $V_{CC(B)}$ to disable voltage clamping for DDC signals

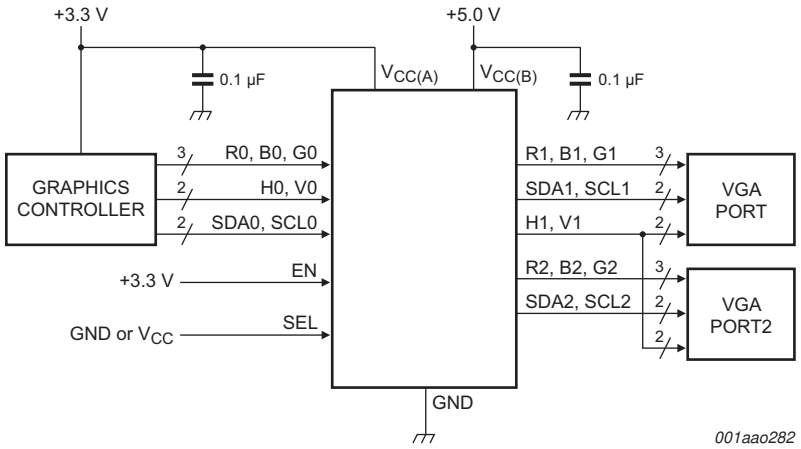
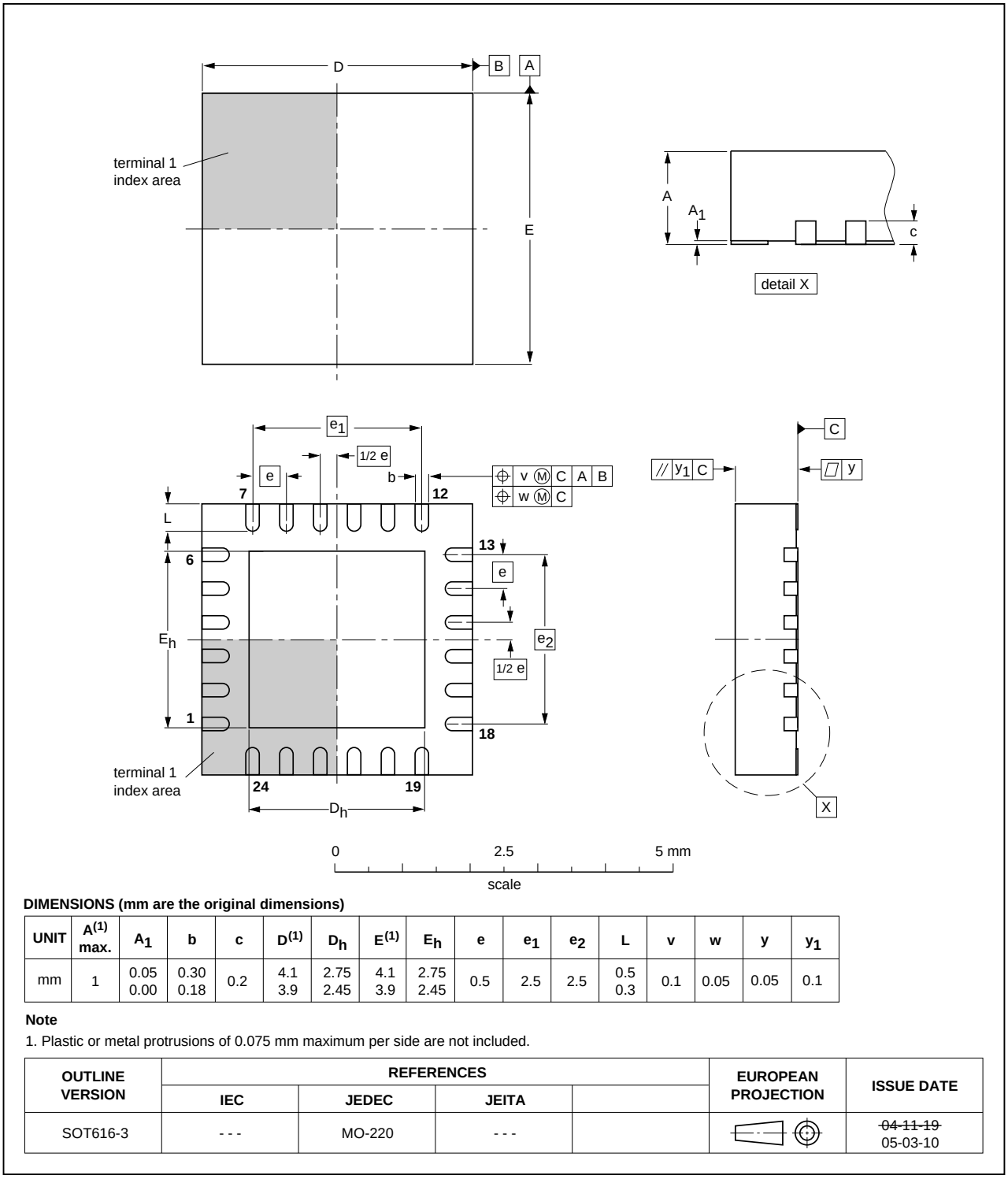


Fig 14. Typical operating circuit

15. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	4.1 3.9	2.75 2.45	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-3	- - -	MO-220	- - -			~~04-11-19~~ 05-03-10

Fig 15. Package outline SOT616-3 (HVQFN24)

16. Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
DDC	Display Data Channel
ESD	ElectroStatic Discharge
HBM	Human Body Model
KVM	Keyboard Video Mouse
MM	Machine Model
RGB	Red Green Blue
SPDT	Single Pole Double Throw
TTL	Transistor-Transistor Logic
VESA	Video Electronics Standards Association

17. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5DV4885E v.2	20111104	Product data sheet	-	NX5DV4885E v.1
Modifications:	• Legal pages updated.			
NX5DV4885E v.1	20110719	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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