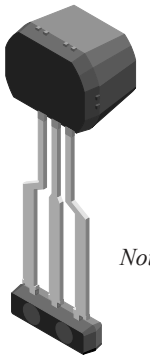
ATS344

High-Precision Linear Hall-Effect Sensor IC
with Two-Wire Current-Mode PWM Output and Integrated Rare-Earth Pellet Package

FEATURES AND BENEFITS

- Magnetic sensor IC with integrated rare-earth pellet
- Two-wire current mode PWM (pulse-width modulation) output
- Customer-programmable position range selection and offset, bandwidth, output clamps, and temperature compensation
- Sensitivity temperature coefficient and offset drift preset at Allegro
- Temperature-stable, mechanical stress immune, and low noise device output via proprietary active stress compensation and four-phase chopper stabilization design techniques
- Wide ambient temperature range: –40°C to 150°C
- Operates with 3.75 to 9.5 V supply voltage
- Differential linear signal processing
- AEC-Q100 qualified

PACKAGE: 3-pin SIP (suffix SP)



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DESCRIPTION

The ATS344 device is a high-precision, back-biased programmable Hall-effect linear sensor integrated circuit (IC) with a configurable current-mode pulse-width-modulated output, for both automotive and non-automotive applications. Integrated within the ATS344 are two Hall-effect sensing elements, signal processing circuitry, and a rare-earth magnetic pellet. The magnetic pellet provides a common-mode magnetic bias while the outputs of the two sensing elements are subtracted, amplified, and processed to produce an output proportional to the differential magnetic input signal. The differential magnetic input signal is typically produced from influence of a ferromagnetic target. The ATS344 is well-suited for applications that require axial position sensing of a rotating target.

The signal path of the ATS344 provides flexibility through external programming that allows the generation of an accurate, and customized output response from a ferromagnetic target perturbation. The ATS344 provides up to 10 bits of resolution. This part is calibrated at the factory to ensure the most stable response over specified conditions.

The BiCMOS monolithic integrated circuit incorporates two Hall sensor elements and precision temperature-compensating circuitry to reduce the intrinsic sensitivity and offset drift or mismatch of the differential Hall elements. The amplification and analog-to-digital conversion path is designed to ensure optimal channel matching through the use of proprietary dynamic offset cancellation circuits, and advanced active stress compensation to reduce lifetime drift.

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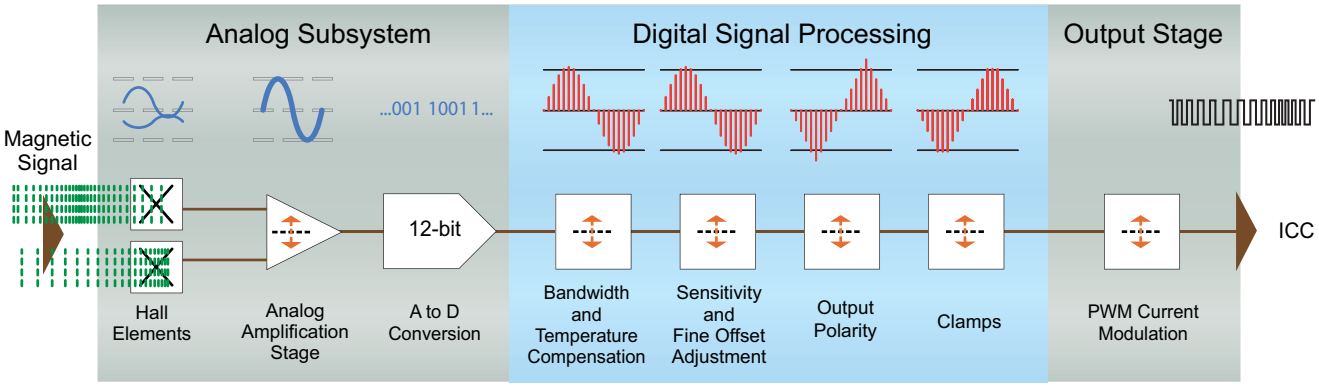

Figure 1: ATS344 Signal Processing Path.
Functions with programmable parameters indicated by double-headed arrows.

DESCRIPTION (continued)

With on-board EEPROM and advanced signal processing functions, the ATS344 provides an unmatched level of customer reprogrammable options for characteristics such as gain and offset, bandwidth, and output clamps. In addition, the device supports separate hot and cold temperature compensation.

The ATS344 in the 3-pin SIP package (SP suffix) complies with the requirements of EU Directive 2002/95/EC (RoHS) and 2011/65/EU (RoHS II), amended by 2015/863/EU, on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment. The package contains an integrated SmCo rare-earth pellet.

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SELECTION GUIDE

Part Number	Package	Packing [1]	Leadframe Plating
ATS344LSPTN-T	3-pin SIP	13-inch reel	100% matte tin

[1] Contact Allegro™ for additional packing options

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		20	V
Reverse Supply Voltage	V_{RCC}		–20	V
Forward Supply Current	I_{CC}		30	mA
Reverse Supply Current	I_{RCC}		–30	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [2]	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Single-sided PCB, copper limited to solder pads, 2 pins (center pin removed)	159	°C/W
		Single-sided PCB, copper limited to solder pads, 3 pins	146	°C/W

[2] Additional information is available on the Allegro website.

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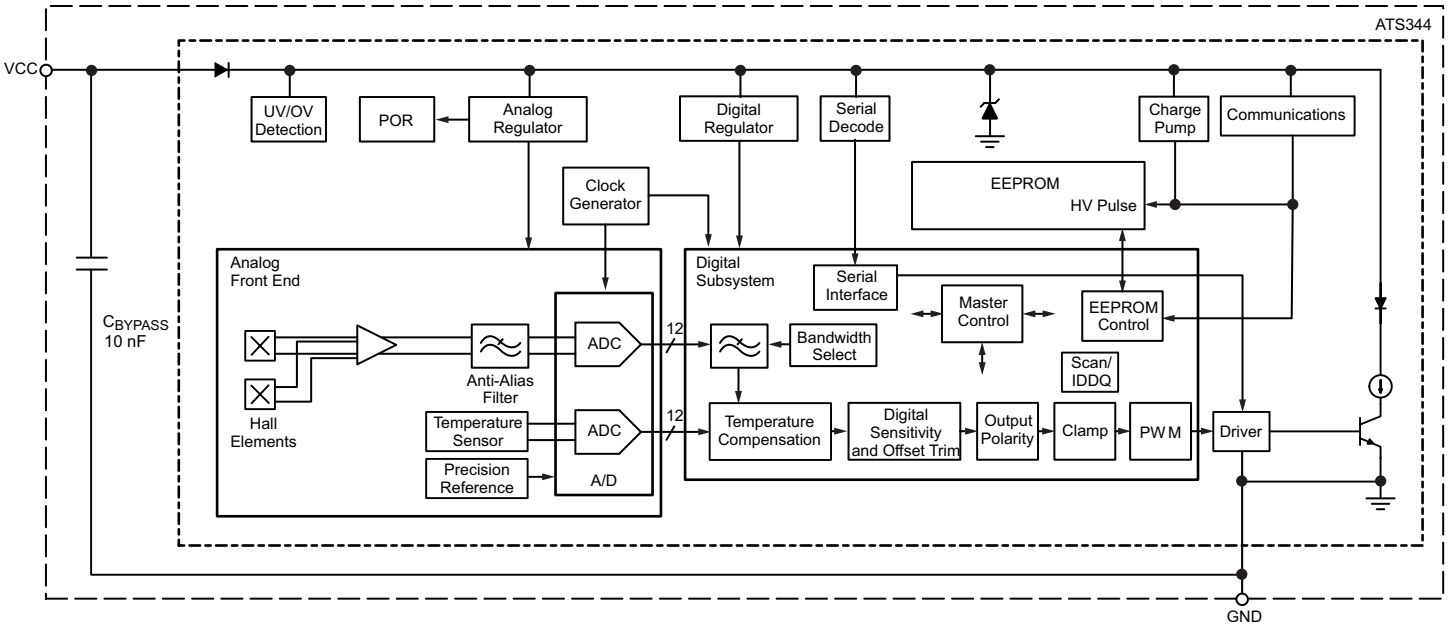
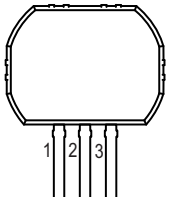
FUNCTIONAL BLOCK DIAGRAM



PINOUT DIAGRAM AND TERMINAL LIST TABLE



Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCC	Input power supply and current mode PWM output
2	Test	Pin used for production testing at Allegro
3	GND	Device ground

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ELECTRICAL CHARACTERISTICS: Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL ELECTRICAL CHARACTERISTICS						
Supply Voltage [1]	V_{CC}		3.75	–	9.5	V
Supply Current	$I_{CC(LOW)}$		6	–	10	mA
	$I_{CC(HIGH)}$		13.6	–	16	mA
	$I_{CC(HYS)}$		5.2	–	6.5	mA
Reverse Supply Current	I_{RCC}	V_{RCC} = –20 V, T_A = 25°C	–8	–	–	mA
Slew Rate [2]	SL	Refer to the application circuit in Figure 7	7	16	–	mA/µs
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	I_{CC} = I_{CC}(max) + 3 mA, T_A = 25°C	20	–	–	V
Hall Chopping Frequency	f_C	T_A = 25°C	–	128	–	kHz
Undervoltage Detection [3]	$V_{CC(UV)LOW}$		3.4	–	–	V
	$V_{CC(UV)HIGH}$		–	–	3.7	V
Overvoltage Detection [3]	$V_{CC(OV)LOW}$		10.5	–	–	V
	$V_{CC(OV)HIGH}$		–	–	13	V
Output PWM Frequency	f_{PWM}	EEPROM FPWM_DC code 3	850	1000	1150	Hz
Integrated Capacitor	C_{BYPASS}		–	10	–	nF
OUTPUT ELECTRICAL CHARACTERISTICS						
PWM Resolution	Res_{PWM}		–	12	–	bits
Power-On Time [4][5]	t_{PO}	BW setting = 500 Hz (EEPROM F3DB_DC = 4)	–	3	–	ms
Signal Path Propagation Delay [4][5]	t_{SDLY}	BW setting = 500 Hz (EEPROM F3DB_DC = 4)	–	3	–	ms
Full Scale Output Range	FSO		–	–	96	%DC

[1] Supply Voltage is the potential measured between the VCC and GND pins.
[2] Determined from design and lab characterization on a limited number of samples; not tested in production.
[3] Refer to section on Protection Features for more information on Undervoltage and Overvoltage Detection.
[4] Determined from design and lab characterization on a limited number of samples; not tested in production.
[5] See Definitions of Terms section.

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MAGNETIC CHARACTERISTICS: Valid at T_A = 25°C and V_{CC} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
INITIAL DEVICE VALUES (Before Customer Programming)						
Effective Resolution	Res_{eff}	Reference Target at maximum air gap with F3DB_DC setting = 500 Hz	–	9	–	bits
Input Signal Range	B_{SIG}	Differential magnetic input signal	–340	–	340	G
Initial Sensitivity	$Sens_{init}$	SENSDC = 0x0 [2]	–	0.404	–	%FSO/G
Initial Quiescent Output	$QOUT_{init}$	Infinite air gap	–	50	–	%FSO
Initial Output Clamp	$OUTCLP(H)_{init}$		97.7	98	98.3	%DC
	$OUTCLP(L)_{init}$		1.7	2	2.3	%DC
Initial Sensitivity Drift Through Temperature Range [3]	$\Delta Sens_{init}$	T_A = –40°C to 150°C	–4	0	+4	%
Initial Offset Output Drift Through Temperature Range [3]	$\Delta OUT(Q)_{init}$	T_A = –40°C to 150°C	–	±6	–	G

[1] *FSO* means Full Scale Output. See Definitions of Terms section.
[2] This corresponds to a sensitivity multiplier of “4” according to the table “SENSDC - values” on page 32.
[3] Initial Offset and Sensitivity drifts through temperature range may vary with influences from the application Target.

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PROGRAMMABLE CHARACTERISTICS: Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
INTERNAL BANDWIDTH PROGRAMMING						
Bandwidth Programming Bits	Bits(BW)		–	3	–	bit
Bandwidth Programming Range [2]	BW	T_A = 25°C; for programming values, see F3DB_DC in EEPROM Structure section	250	–	4000	Hz
Bandwidth Post-Programming Tolerance	ΔBW	T_A = 25°C, measured as a percentage of BW	–	±5	–	%
FINE QUIESCENT OUTPUT ADJUSTMENT						
Fine Quiescent Output Adjustment Bits	QVODC		–	12	–	bit
Fine Quiescent Output Adjustment Range	QOUT_FINE	T_A = 25°C, B_{DIFF} = 0 G	–50	–	49.98	%FSO
Fine Quiescent Output Adjustment Step Size	$Step_{QOUT\_FINE}$	T_A = 25°C, B_{DIFF} = 0 G	–	0.0244	–	%FSO
OUTPUT SENSITIVITY						
Output Sensitivity Programming Range [3]	$SENS_{MULT}$	T_A = 25°C	0	–	8	–
Sensitivity Programming Bits [4]	SENSDC		–	12	–	bit
Sensitivity Programming Step Size	$Step_{SENS\_OUT}$	T_A = 25°C	–	2^{-11}	–	–
Output Polarity Bit	OUTPUT_INVERT		–	1	–	bit

[1] *FSO* means Full Scale Output. See Definitions of Terms section.
[2] Determined from design; not tested in production.
[3] The Initial Sensitivity is adjustable by the SENSDC parameter. When reducing the initial Sensitivity check the input signal is within the range specified by BSIG.
[4] Sensitivity programming parameter SENSDC is a multiplier applied to the initial Sensitivity with step size defined by StepSENS_OUT parameter. Refer to the Programmable Parameter Reference section for more information.

Continued on the next page…

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PROGRAMMABLE CHARACTERISTICS (continued): Valid through full operating temperature range, T_A, and supply voltage, V_{CC}, C_{BYPASS} = 10 nF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
TEMPERATURE COMPENSATION (TC) FOR BACK-BIASED DEVICES						
1st Order Sensitivity TC Programming Bits		TC1_SENS_CLD, TC1_SENS_HOT	–	8	–	bits
1st Order Sensitivity TC Programming Range	$TC1_{SENS}$		–0.0976	–	0.291	%/°C
1st Order Sensitivity TC Programming Step Size	$Step_{TC1SENS}$		–	1.526	–	m%/°C
2nd Order Sensitivity TC Programming Bits		TC2_SENS_CLD, TC2_SENS_HOT	–	9	–	bits
2nd Order Sensitivity TC Programming Range	$TC2_{SENS}$		–1.526	–	1.52	%/(°C)^2
2nd Order Sensitivity TC Programming Step Size	$Step_{TC2SENS}$		–	0.00596	–	m%/(°C)^2
OUTPUT CLAMPING RANGE						
1st Order Magnetic Offset TC Programming Bits		DBOFFDC	–	8	–	bits
1st Order Magnetic Offset TC Programming Range	TC1_OFFSET[1]	Sens = 21 LSB/G, SENSDC = 0	–0.867	–	0.867	G
1st Order Magnetic Offset TC Programming Step Size	$Step_{TC1\_OFFSET}$	Sens = 21 LSB/G, SENSDC = 0	–	±0.0068	–	G
Clamp Programming Bits		CLAMP_HIGH	–	11	–	bits
		CLAMP_LOW	–	11	–	bits
Output Clamp Programming Range	$OUT_{CLP(H)}$	T_A = 25°C	51	–	100	%FSO
	$OUT_{CLP(L)}$	T_A = 25°C	0	–	49	%FSO
Clamp Programming Step Size	$Step_{CLP(H)}$	T_A = 25°C	–	0.0239	–	%FSO
	$Step_{CLP(L)}$	T_A = 25°C	–	0.0239	–	%FSO
ACCURACY (AFTER CUSTOMER PROGRAMMING)						
Sensitivity Drift Due to Package Hysteresis	$\Delta Sens_{PKG}$	Variation on final programmed Sensitivity value; measured at T_A = 25°C after temperature cycling	–	< ±1.5	–	%
Linearity Error [2]	ERR_{LIN}	Deviation from an ideal straight line sensor response at maximum air gap	–2	–	2	%FSO
Offset Drift Over Lifetime [3]	ERR_{OUT}	AEC-Q100 grade 0 qualification	–15	–	30	G
		Temperature cycle profile: –40°C to 130°C for 9 cycles, –40°C to 150°C for 1 cycle; dwell time of 15 minutes at min. and max. temperature; ramp rate of 7.8°C/minute from –40°C to 20°C; total of 1000 cycles	–12	–	12	G
Offset Drift Over Supply Voltage Range [4]	ERR_{VCC}		0	–	4	G

[1] TC1_OFFSET range can vary by ±10% with the initial factory settings.
[2] Does not include nonlinearity of the target shape. Determined from design; not tested in production.
[3] Offset drift from the custom temperature cycles characterized on product of same family using same package, same lead frame, and same die size with identical Hall location.
[4] Voltage calculated as Q_{OUT} at $V_{CC(max)}$ – Q_{OUT} at $V_{CC(min)}$.

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REFERENCE TARGET CHARACTERISTICS

This reference target is an example for linear displacement measurement in conjunction with the ATS344. The target displacement range and the air gap is determined by the size of the "V-groove" and the material. The groove can be machined on any ferrous part, even on rotating shafts that have an axial movement. Please contact Allegro directly for support on target shape selection; Allegro can provide examples of potential target solutions and in certain situations may provide custom target design support.

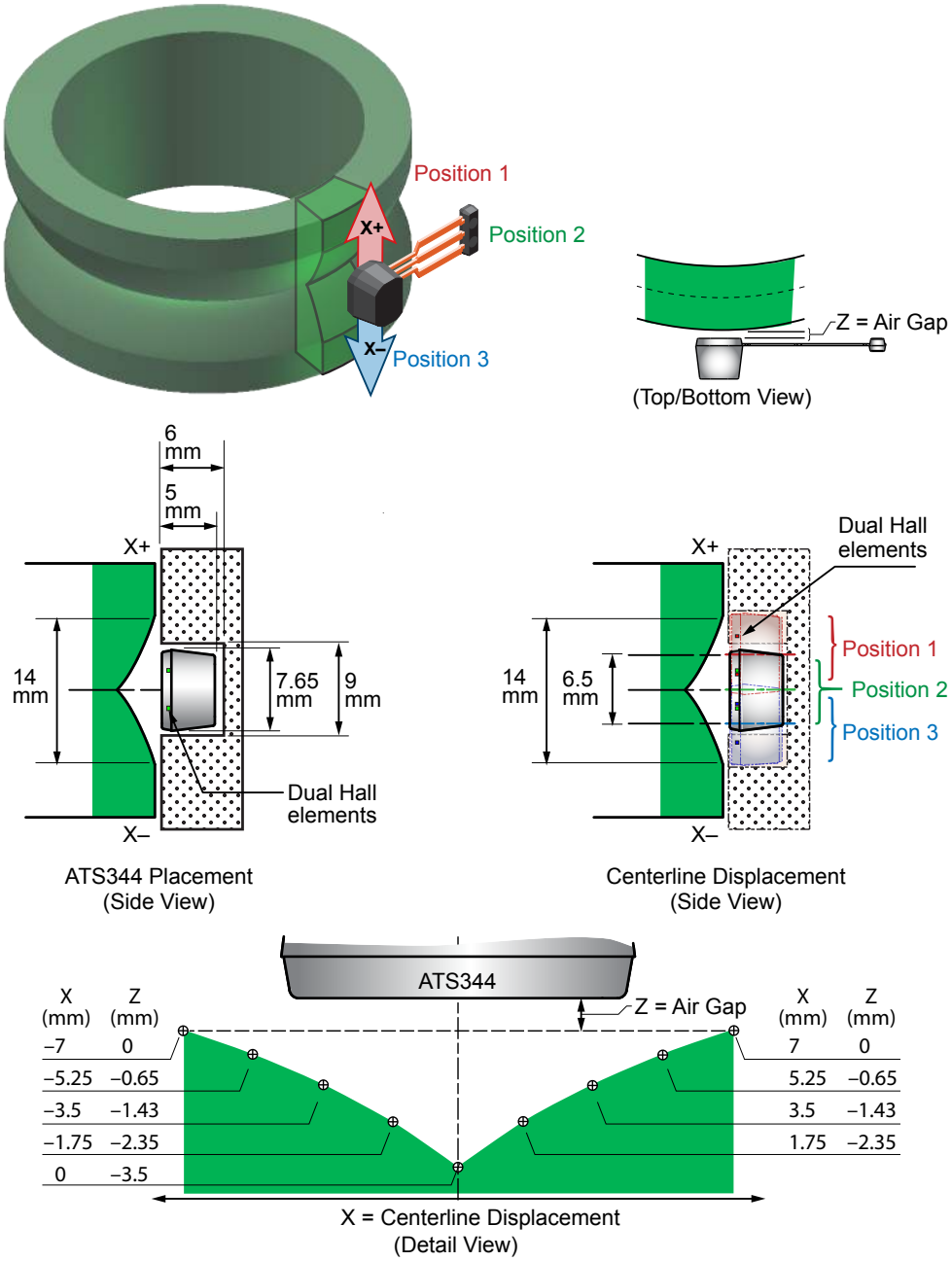

Figure 2: Reference Target Characteristics

Reference target material: 1018 CRS mild steel with nickel plating (electroless plating thickness 0.75-1.28 µm)

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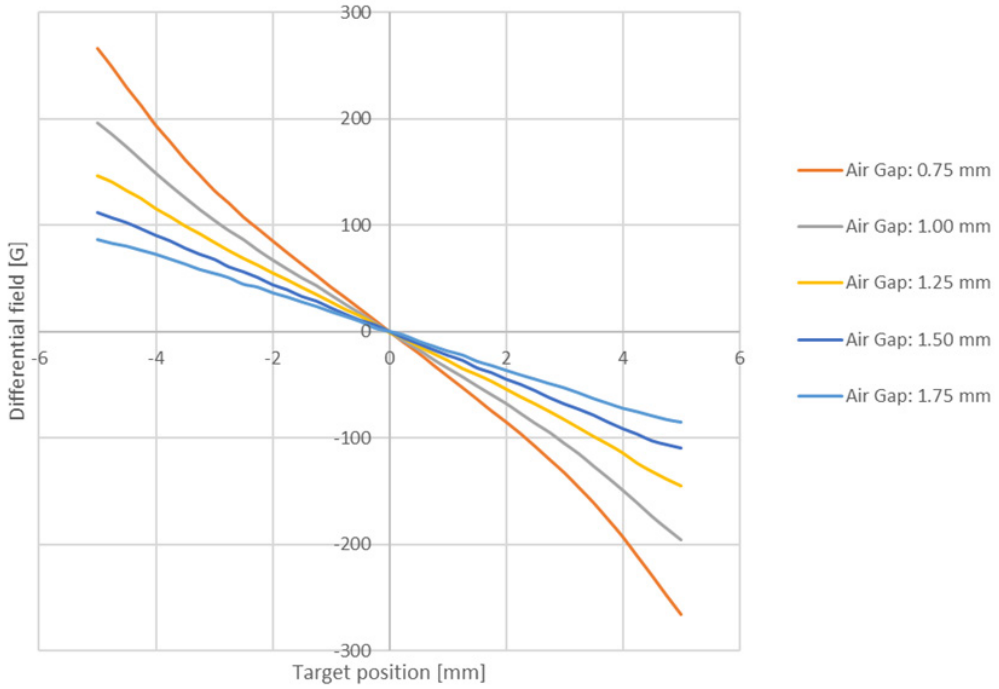

**Figure 3: ATS344LSP Reference Target –
Differential Input Signal versus Target Position**

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FUNCTIONAL DESCRIPTION

This section provides descriptions of the operating features and subsystems of the ATS344. For more information on specific terms, refer to the Definitions of Terms section. Tables of EEPROM parameter values are provided in the EEPROM Structure section and EEPROM Customer-Programmable Parameter Reference.

Digital Signal Processing

TEMPERATURE COMPENSATION

The magnetic properties of materials can be affected by changes in temperature, even within the rated ambient operating temperature range, T_A. Changes in the differential magnetic input signal due to temperature variation causes a proportional change in the device output. The ATS344 features integrated digital temperature compensation (TC) circuitry that is programmable to reduce influences of all reproducible externally induced variations. Temperature coefficients for Sensitivity and Offset are programmable using the corresponding EEPROM parameters.

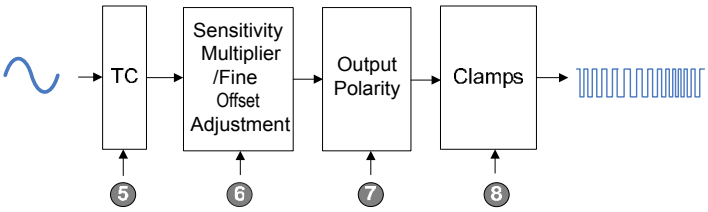

Figure 4: Signal Path for Digital Subsystem

The ATS344 uses 1st order Magnetic Offset TC to compensate for output offset drift across the ambient temperature range (see Figure 5). The programmable parameter, DBOFFDC, is used to adjust the Magnetic Offset TC. For more information on the programmable parameter, DBOFFDC, refer to the EEPROM Customer-Programmable Parameter Reference section.

In addition to the Magnetic Offset TC compensation, the ATS344 also contains features to compensate Sensitivity for variations of the differential magnetic input signal with temperature. This is accomplished with segmented 1st and 2nd order Sensitivity TC that dynamically adjusts the Sensitivity. There are two programmable Sensitivity TC segments: temperatures above 25°C, Hot, and temperatures below 25°C, Cold. Each segment is independently programmable with 1st and 2nd order coefficients. See Table 1 for a list of the programmable parameters and Figure 6 for illustrations of the Sensitivity TC. Refer to the EEPROM Customer-Programmable Parameter Reference section for more information.

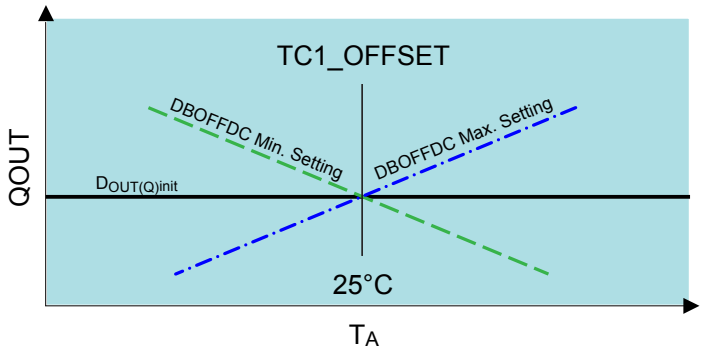

Figure 5: The Magnetic Offset Temperature Compensation Coefficient, TC1_OFFSET

Table 1: Sensitivity Temperature Compensation Parameters

	T_A Range	
	< 25°C	> 25°C
1st Order	TC1_SENS_CLD	TC1_SENS_HOT
2nd Order	TC2_SENS_CLD	TC2_SENS_HOT

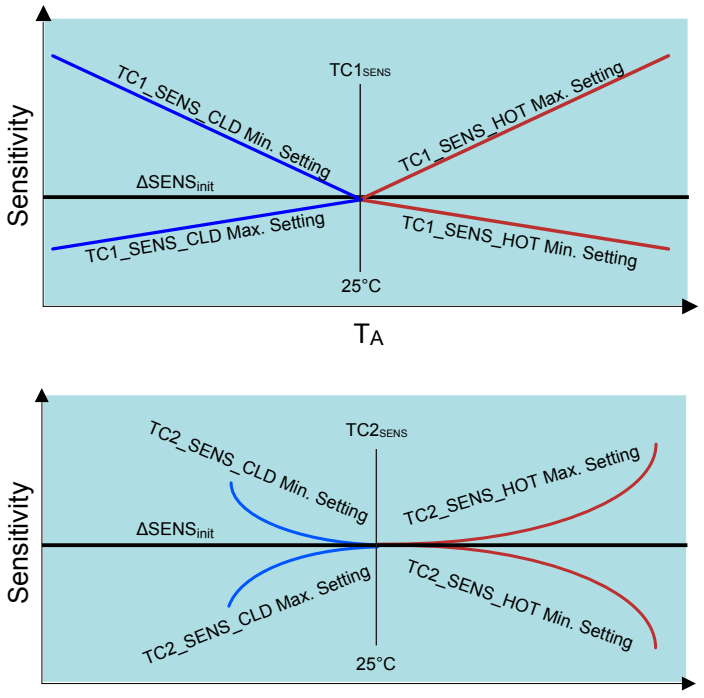

Figure 6: Sensitivity TC Function: (upper) first order, (lower) second order

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The programmable parameters determine the output temperature compensation, YTC, according to the following formula:

$$Y_{TC}\,(\%FSO) = Y_{AD}\,(\%FSO) + [(TC1_{SENS}\,(m\%/°C) \times \Delta T_A\,(°C) + (TC2_{SENS}\,(m\%/°C^2) \times \Delta T_A\,(°C)^2] \times Y_{AD}\,(\%FSO) + TC1\_OFFSET\,(G/°C) \times \Delta T_A\,(°C) \quad (1)$$

where:

Y_{AD} is the input from the analog subsystem via the A-to-D converter;

$TC1_{SENS}$ is the first-order Sensitivity temperature coefficient, set by either TC1_SENS_HOT, or TC1_SENS_CLD depending on T_A;

$TC2_{SENS}$ is the second-order Sensitivity temperature coefficient, set by either TC2_SENS_HOT, or TC2_SENS_CLD depending on T_A;

TC1_OFFSET is the first-order Offset temperature coefficient (to convert units from G/°C, divide the value by $Sens_{Init}$);

ΔT_A is the change in ambient temperature from 25°C (for example: at 150°C, ΔT_A = 150°C – 25°C = 125°C, or at –40°C, ΔT_A = –40°C – 25°C = –65°C).

FINAL SENSITIVITY (GAIN) ADJUSTMENT

The ATS344 has a programmable parameter to adjust Sensitivity, SENSDC. The programmable parameter SENSDC, is used in block 6 of Figure 4, for a fine adjustment of the Sensitivity. The value of this 12-bit parameter, applied in the digital subsystem, is multiplied to the factory Sensitivity value (see equation 3). For example, SENSDC = 0 has a multiplier value of 4, SENSDC = 2047 has multiplier value of 8, and SENSDC = 2048 has a multiplier value of approximately 0. Refer to the EEPROM Customer-Programmable Parameter Reference section for more information on parameter SENSDC.

OUTPUT OFFSET FINE ADJUSTMENT

The ATS344 DSP subsystem also includes a parameter to adjust the Quiescent Output, or offset. It is adjusted by the parameter QVODC that controls the QOUT_FINE value. This programmable parameter, QVODC, is used as a fine adjustment to the Quiescent Output and determines the value for QOUT_FINE, 6 in Figure 4. The value of QVODC is a percentage of the FSO. It is programmable to add or subtract as much as 50% of FSO. Refer to the EEPROM Customer-Programmable Parameter Reference section for more information on parameter QVODC. The QVODC parameter is programmed in the factory, in order to be calibrated to a reference target. The customer should reference and adjust this value.

The output of the digital subsystem, Y_{DA}, after applying the parameters for fine adjustment of Sensitivity and offset is shown in equation 3. This value is prior to the clamps.

$$Y_{DA}\,(\%FSO) = SENS\_MULT \times Y_{TC}\,(\%FSO) + QOUT\_FINE\,(\%FSO) \quad (2)$$

$$Sens\,(\%FSO/G) = SENSDC \times Factory\ Sensitivity \quad (3)$$

where SENS_MULT is the multiplication factor from 0 to 8 set by the parameter SENSDC. The initial Sensitivity, $Sens_{init}$, is defined with a SENS_MULT default of 4.

OUTPUT POLARITY SETTING

The OUTPUT_INVERT parameter sets the device output signal polarity with respect to the sensed magnetic response polarity. The default (0) is depicted in Figure 3, referenced to Figure 2, where the sensor is moving relative to the target. Setting the parameter to 1 inverts the output value.

OUTPUT CLAMPS SETTING

The ATS344 digital subsystem contains programmable clamp features, to adjust the normal operating output range; see 8 in Figure 4. The ATS344 output clamps are initially set to 0% and 100% of FSO, for low and high output clamp respectively. The programmable EEPROM parameters, CLAMP_HIGH and CLAMP_LOW are available to adjust limits for the normal operating output. The ATS344 Diagnostic outputs levels are not bound by these parameters.

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Protection Features

Supply voltage detection and clamping features protect the ATS344 internal circuitry and prevent spurious output when supply voltage is out of specification.

PREPROGRAMMED DEFAULT VALUES

Default values prevent system failures due to communication errors during real time customer reprogramming of EEPROM. The default values also can be used as defaults for normal operation, reducing the initial customer programming requirements.

UNDERVOLTAGE AND OVERVOLTAGE DETECTION

The ATS344 contains circuitry to detect a condition when the supply voltage drops below or exceeds specified operating limits. Hysteresis is designed into the circuits to prevent chattering around the threshold. This hysteresis is defined by $V_{CC(UV)HIGH} - V_{CC(UV)LOW}$ for undervoltage detection and $V_{CC(OV)HIGH} - V_{CC(OV)LOW}$ for overvoltage detection. As an example, initially V_{CC} is within the normal operating range. If V_{CC} drops below $V_{CC(UV)LOW}$, the output duty cycle is forced to a 100% duty cycle, with the output at approximately $I_{CC(HIGH)}$. Note, as V_{CC} further reduces below the specified operating range, the $I_{CC(HIGH)}$ level reduces, and the there is no PWM output signal transmitted. When V_{CC} returns above $V_{CC(UV)HIGH}$, the output returns to its normal operating state. The output will not respond with normal data until a delay of t_{PO} after an undervoltage event.

The ATS344 contains circuitry to detect a condition when the supply voltage rises above the specified operating limit. As an example, initially V_{CC} is within the normal operating range. If V_{CC} rises above $V_{CC(OV)HIGH}$, the output duty cycle is forced to 0% duty cycle, with the output at approximately $I_{CC(LOW)}$. When V_{CC} returns below $V_{CC(OV)LOW}$, V_{OUT} returns to its normal operating state.

EEPROM FAULT DETECTION

The ATS344 contains EEPROM with error checking and correction, ECC. The ECC corrects for a single-bit EEPROM error without effecting device performance. The ECC also detects a dual-bit EEPROM error and triggers an internal fault signal that disables the output to 0% duty cycle, or $I_{CC(LOW)}$ state.

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Typical Application

The device contains an on-chip regulator and can operate across a wide V_{CC} range. For devices that must operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFi protection may still be required. Contact Allegro for information on the circuitry required for compliance with various EMC specifications. Refer to Figure 7 for an example of a basic application circuit. Sense resistor minimum value is determined by the desired signal-to-noise ratio of the current interface, while its maximum value is determined by the supply voltage and the voltage drop across said resistor (headroom).

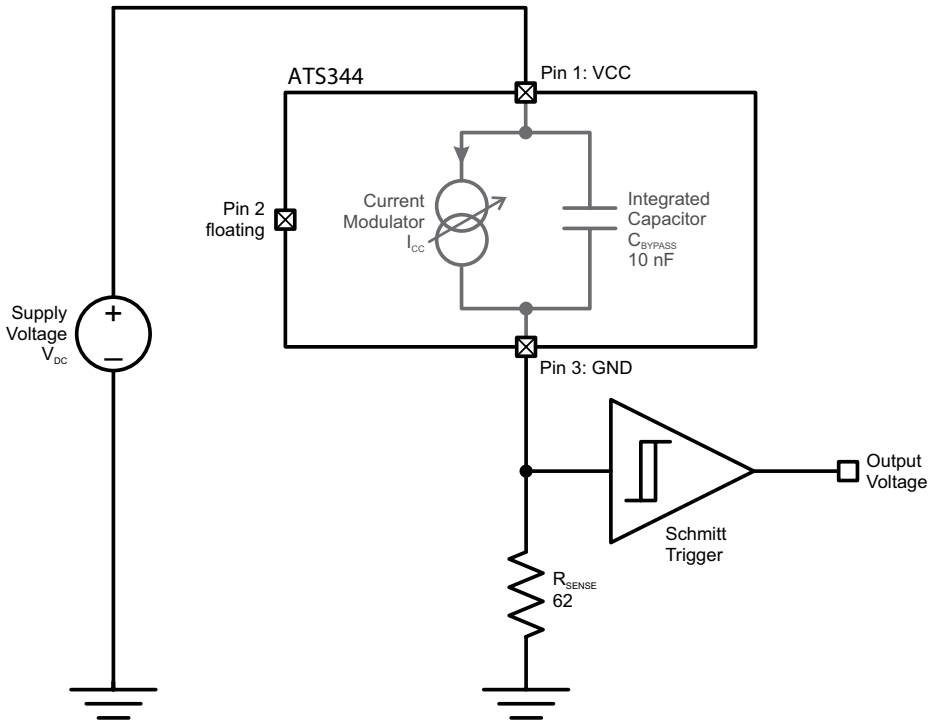

Figure 7: Typical Application Circuit

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PROGRAMMING SERIAL INTERFACE

The ATS344 incorporates a serial interface that allows an external controller to read and write registers in the ATS344 EEPROM and volatile memory. The ATS344 uses a point-to-point communication protocol, based on Manchester encoding per G. E. Thomas (a rising edge indicates 0 and a falling edge indicates 1), with address and data transmitted MSB first. Commands are sent to the device via modulation of V_{CC} (refer to $V_{CC(OV)HIGH}$ and $V_{CC(OV)LOW}$ thresholds); the device responds by modulation of I_{CC}.

Transaction Types

Each transaction is initiated by a command from the controller; the ATS344 does not initiate any transactions. Two commands are recognized by the ATS344: Write and Read. There also is a special function Write command: Write Access Code. One response frame type is generated by the ATS344, Read Acknowledge. If the command is Read, the ATS344 responds by transmitting the requested data in a Read Acknowledge frame. If the command is any other type, the ATS344 does not acknowledge.

As shown in Figure 8, The ATS344 receives all commands via the VCC pin. It responds to Read commands via the ICC. This implementation of Manchester encoding requires the communication pulses to cross the overvoltage detection thresholds ($V_{CC(OV)HIGH}$, $V_{CC(OV)LOW}$).

Writing the Access Code

If the external controller intents to write or to read from the ATS344 memory during the current session, it must establish serial communication with the ATS344 by sending a Write command including the Access Code within t_{ACC} after powering up the ATS344. If this deadline is missed, all write and read access is disabled until the next power-up.

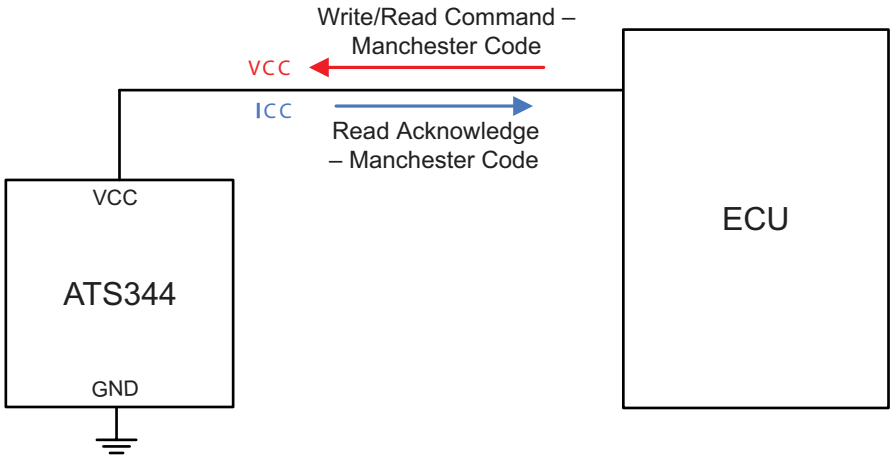

Figure 8: Top-Level Programming Interface

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Reading from EEPROM

A Read command with the register number is sent from the controller to the ATS344. The device responds with a Read Acknowledge frame. Output is automatically disabled after the Read command from the controller is received and output is enabled after a Read Acknowledge command is sent.

Error Checking

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check). The CRC algorithm is based on the polynomial

$$g(x) = x^3 + x + 1$$

and the calculation is represented graphically in Figure 9. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111.The trailing 3 bits of a message frame comprise the CRC token.

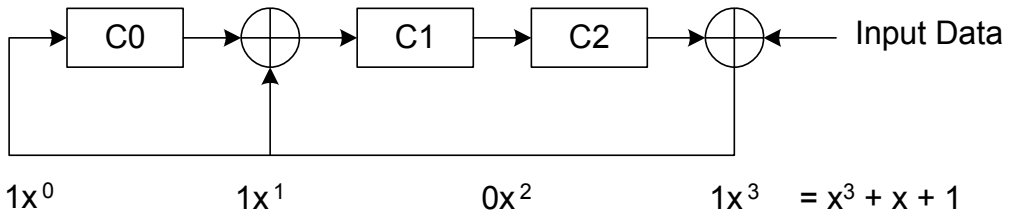

Figure 9: CRC Calculation

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TIMING DIAGRAMS

Serial Write to Volatile Memory

The write sequence is initiated by pulsing VCC above the over-voltage detection threshold, which will cause disabling of the PWM output (ICC = ICC_LOW).

Following this, Manchester data can be sent in on VCC. Once the write is complete, PWM output will start the next PWM frame. This is shown in Figure 10.

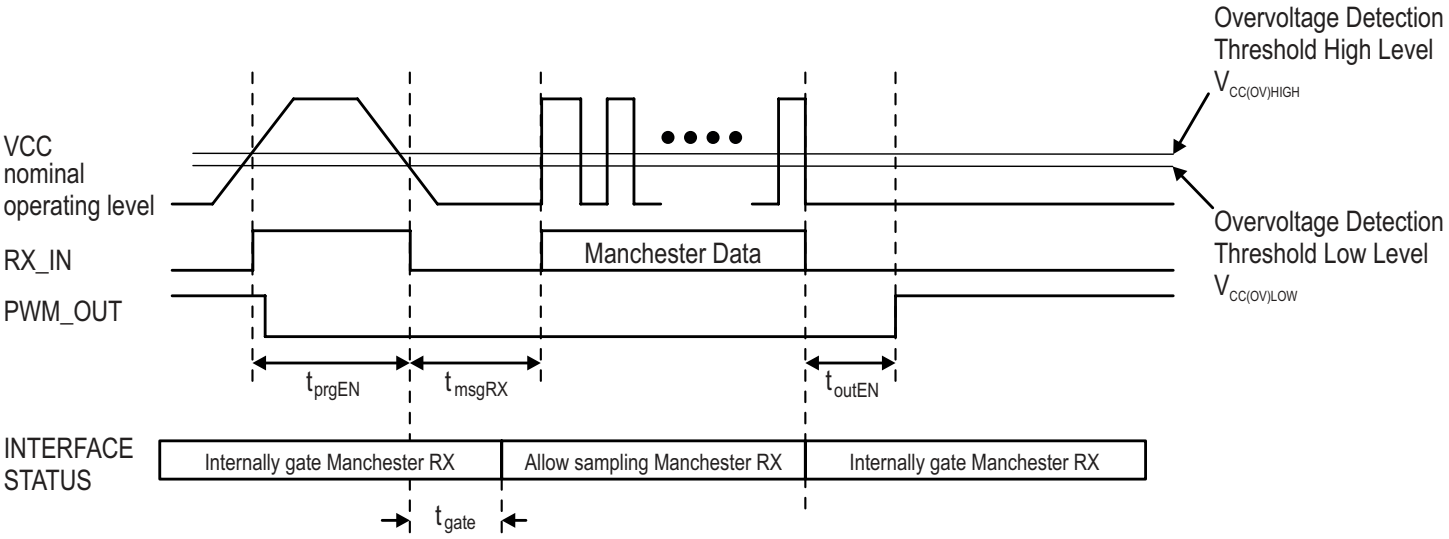

Figure 10: Serial Write to Volatile Memory

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Serial Write to EEPROM

The write sequence is initiated by pulsing VCC above the overvoltage detection threshold, which will cause disabling of the PWM output (ICC = ICC_LOW). Following this, Manchester data can be sent in on VCC. The EEPROM and charge pump controllers will then handle the write to EEPROM. Once the write is complete, PWM output will start the next PWM frame. This is shown in Figure 11. The minimum waiting time after initiating communication is t_{gate}. The maximum time is t_{msgRX}. Transmission of Manchester code has to start within that time window.

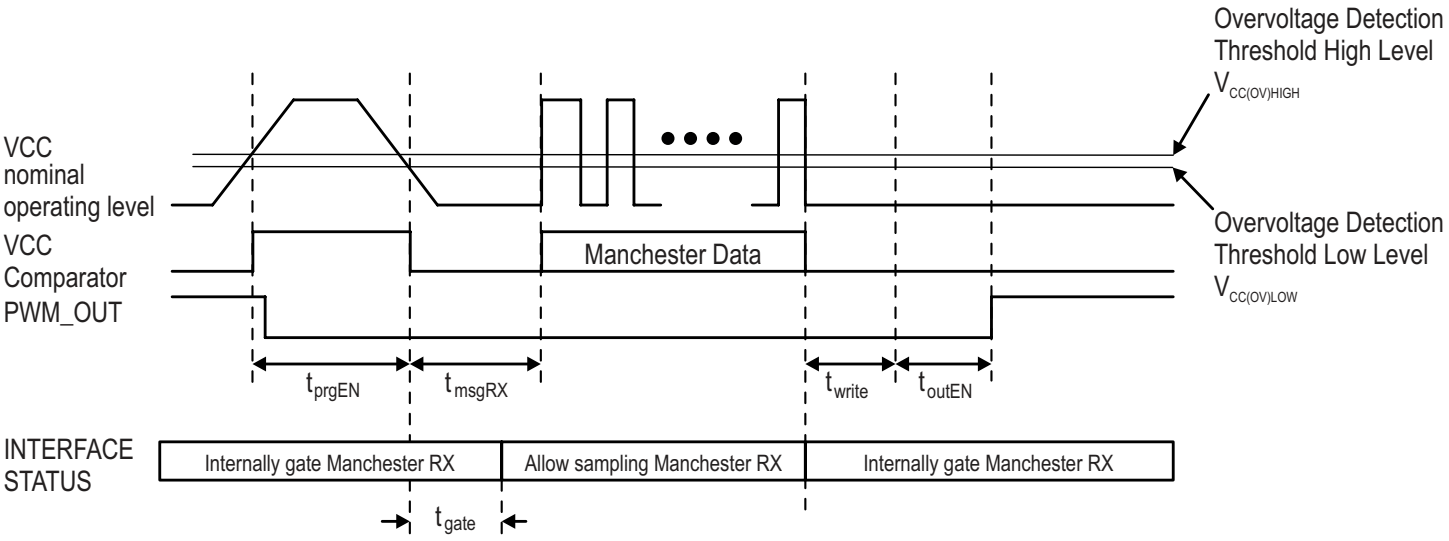

Figure 11: Serial Write to EEPROM

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Serial Read from EEPROM

The write sequence is initiated by pulsing VCC above the over-voltage detection threshold, which will cause disabling of the PWM output (ICC = ICC_LOW). Following this, Manchester data can be sent in on VCC. Manchester data will be output on ICC. Once the read is complete (Manchester data transmitted), PWM output will start the next PWM frame. This is shown in Figure 12.

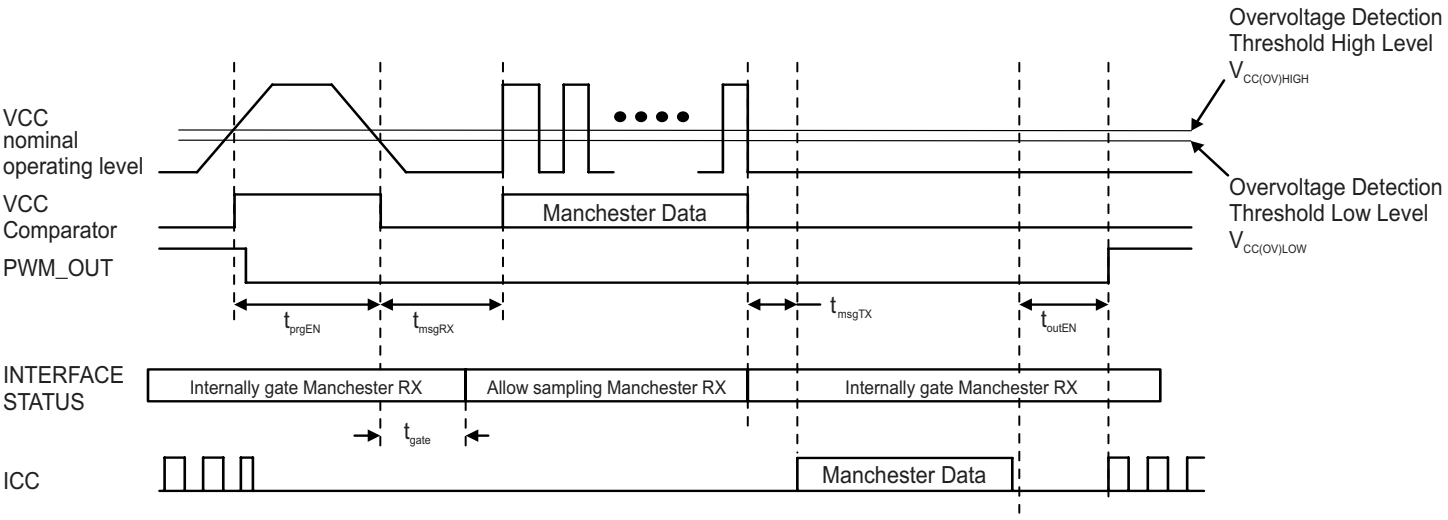

Figure 12: Serial Read

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Serial Access Timeout

Any attempt at a Manchester transaction has a timeout associated with the falling edge of the initial pulse on VCC and the start of Manchester data. If that timeout period expires, then PWM_OUT_ENABLE will go high and PWM output will start the next PWM frame. This is shown in Figure 13.

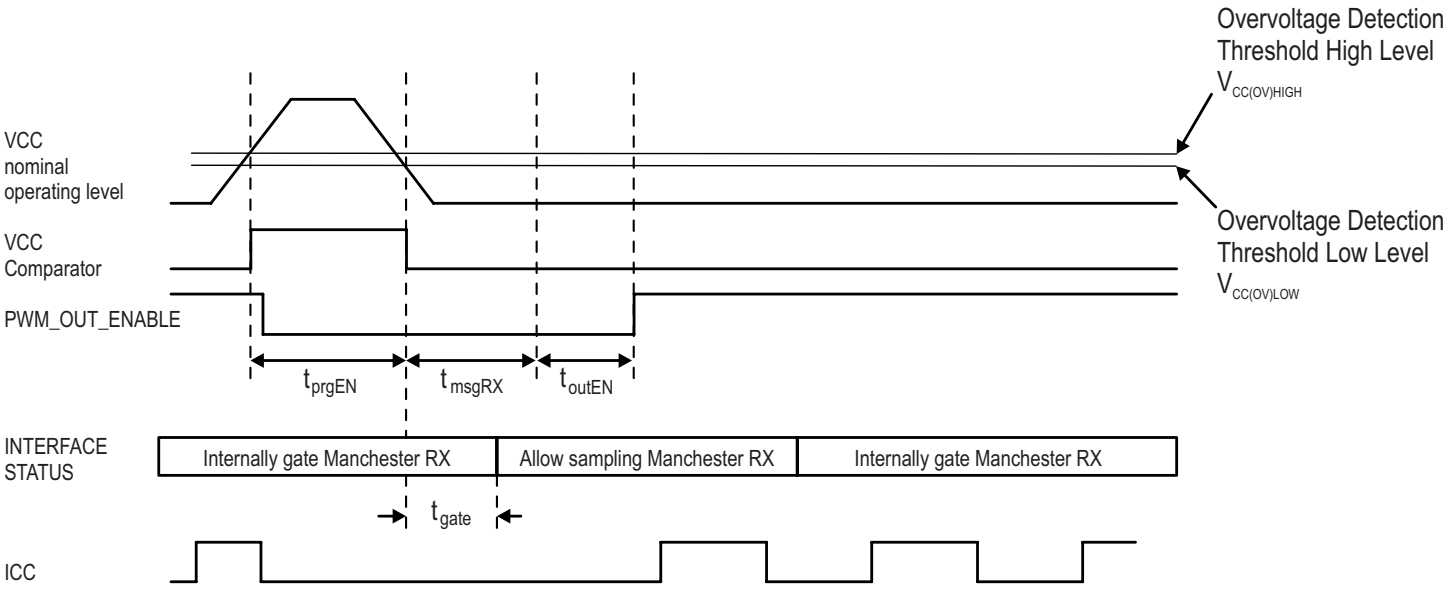

Figure 13: Serial Access Timeout

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Table 2: Serial Interface Timing Parameters

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
Access Code Timeout	t_{ACC}	Customer Access Code should be fully transmitted in less than t_{ACC}, measured from when VCC crosses $V_{CC(OV\_high)}$.	–	–	70	ms
Bit Rate		Defined by the input message bit rate sent from the external controller	4	–	100	kbps
Bit Time Error	err_{tbit}	Deviation for a single bit defined by Manchester encoding	–11	–	11	%
Time to Enable Programming	t_{prgEn}		55.6	–	n/a	µs
Time Before Transmitting Manchester Data to Device	t_{msgRx}		5.6	–	862	µs
Time Before Device Will Listen to RX	t_{gate}		0.8	–	1.1	µs
Time for Output to Start	t_{outEn}		0.05	–	0.1375	µs
Time for EEPROM Write	t_{write}		–	25	–	ms
Time Before Device will Respond with Read Acknowledge	t_{msgTX}		300	475	700	µs

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SERIAL INTERFACE MESSAGE STRUCTURE

The general format of a command message frame is shown in Figure 14: General Format for Serial Interface Commands. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.

The bits are described in Table 3.

The following command messages can be exchanged between the device and the external controller:

- Read
- Read Acknowledge
- Write
- Write Access Code

For EEPROM address information, refer to the EEPROM structure section.

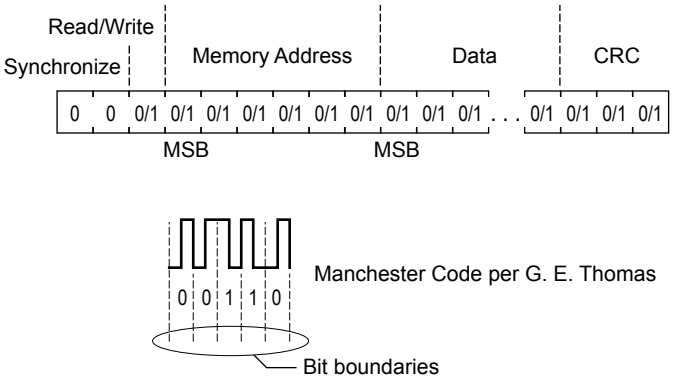

Figure 14: General Format for Serial Interface Commands

Table 3: Serial Interface Command General Format

Bits	Parameter Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
30	Data	0/1	[As required]
3	CRC	0/1	Incorrect value indicates errors

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Table 4: Read Command

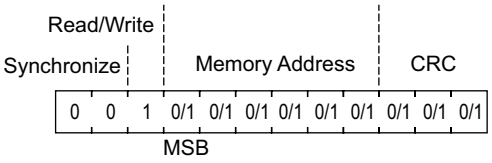
Function	Provides the address in ATS344 memory to be accessed to transmit the contents to the external controller in the next Read Acknowledge command.
Syntax	Sent by the external controller on the ATS344 VCC pin
Related Commands	Read Acknowledge
Pulse Sequence	
Options	
Example	Read Address 0x08 Read/Write = 1 Memory Address = 001000 CRC bits = 110

Table 5: Read Acknowledge

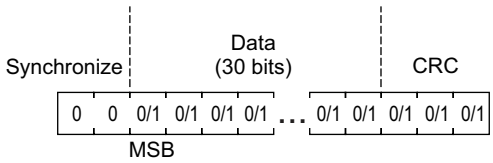
Function	Transmits to the external controller data retrieved from the ATS344 memory in response to the most recent read command.
Syntax	Sent by the ATS344 by ICC modulation. Sent after a Read command
Related Commands	Read
Pulse Sequence	
Options	The 6 MSBs are EEPROM data error checking bits. Refer to the EEPROM structure section for more information
Example	–

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Table 6: Write Command

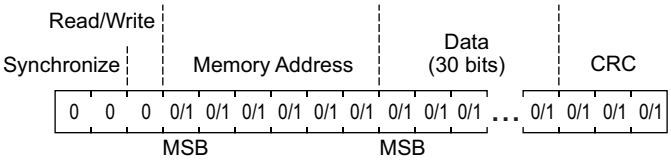
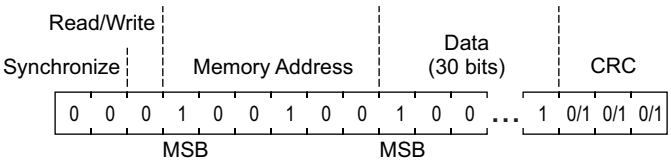
Function	Transmits to the ATS344 data prepared by the external controller
Syntax	Sent by the external controller on the ATS344 VCC pin.
Related Commands	
Pulse Sequence	
Options	
Example	

Table 7: Write Access Code Command

Function	Transmits the access code to the ATS344; data prepared by the external controller, but must match the internal 30-bit code in the ATS344 memory.
Syntax	Sent by the external controller on the ATS344 VCC pin. Sent within 70 ms of A1343 power-on and before any other command.
Related Commands	
Pulse Sequence	
Options	
Example	Standard Customer Access Code: 0x2781_1F77 to address 0x24 Read/Write = 0 Memory Address = 100100 Data bits = 10 0111 1000 0001 0001 1111 0111 0111 CRC bits = 001

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OUTPUT PROTOCOL

The operating output of the ATS344 is a pulse-width modulated current output signal that transfers information proportionally to the applied magnetic input signal.

PWM Output

PWM involves using a current modulation where the state of the pulse is defined by high or low current consumption. These levels are specified as $I_{CC(LOW)}$ and $I_{CC(HIGH)}$ in the Electrical Characteristics table. The duration at which the part is operating at $I_{CC(LOW)}$ or $I_{CC(HIGH)}$ is pulse-width modulated to achieve the output designated signal. The percentage of $I_{CC(HIGH)}$ versus the period duration designates the target position.

- CALIBRATE_PWM parameter can be set to enable calibration of the output 50% duty cycle level at power-on.

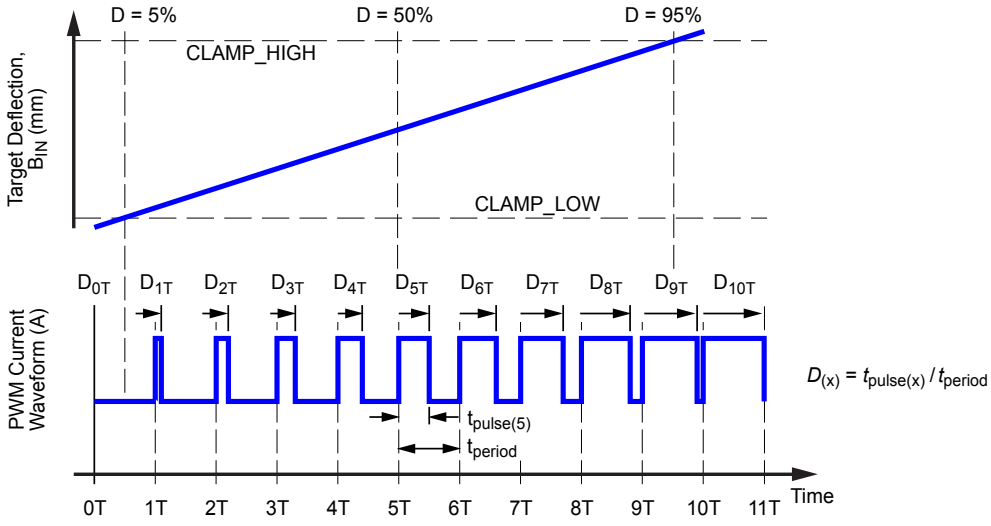

Figure 15: PWM outputs a duty-cycle-based waveform that can be read by the external controller as a cumulatively changing continuous current.

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EEPROM STRUCTURE

Programmable values are stored in an onboard EEPROM, including both volatile and non-volatile registers. Although it is separate from the digital subsystem, it is accessed by the digital subsystem EEPROM Controller module.

Because EEPROM can be read by multiple devices, an arbiter controls access to EEPROM. In the case of simultaneous accesses to EEPROM, priority is assigned as follows:

1. Static Registers (highest)
2. Temperature Compensation
3. Linearization
4. Serial Interface (lowest)

The EEPROM is organized as 30-bit-wide words, and by default each word has 24 data bits and 6 ECC (Error Checking and Correction) check bits, stored as shown in Figure 16.

EEPROM Bit	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15
Contents	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	C5	D10

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D9	D8	D7	D6	D5	D4	C4	D3	D2	D1	C3	D0	C2	C1	C0

Figure 16: EEPROM Word Bit Sequence; C# – Check Bit, D# – Data Bit

Table 8: EEPROM Register Map of Customer-Programmable Parameters

Parameter Name	Address	Bits	Description
TC2DC_HOT	0x08 [23:15]	9	2nd order sensitivity TC, T_A > 25°C
TC2DC_CLD	0x08 [14:6]	9	2nd order sensitivity TC, T_A < 25°C
TC1DC_HOT	0x09 [23:16]	8	1st order sensitivity TC, T_A > 25°C
TC1DC_CLD	0x09 [15:8]	8	1st order sensitivity TC, T_A < 25°C
DBOFFDC	0x09 [7:0]	8	1st order magnetic offset drift
SCRATCH_C_0	0x0A [23:12]	12	Customer scratch area 0
SENSDC	0x0A [11:0]	12	Sensitivity
Unused	0x0B-0x19 {23:12]	12	Unused memory locations
Reserved	0x1A [11:0]	12	Factory access only
Unused	0x1B [23]	1	
OUTPUT_INVERT	0x1B [22]	1	Invert output
Unused	0x1B [21]	1	
ID_C	0x1B [20:12]	9	Customer ID
CLAMP_HIGH	0x1C [23:18]	6	Clamp upper bound
CLAMP_LOW	0x1C [17:12]	6	Clamp lower bound
F3DB_DC	0x1C [2:0]	3	Filter bandwidth select
SCRATCH_C_1	0x1D [23:12]	12	Customer scratch area 1
QVODC	0x1D [11:0]	12	Offset
OUTDRV_CFG	0x1E [20:18]	3	OUTDRV_CFG Output driver rise, fall time or slew rate control setting
CALIBRATE_PWM	0x1E [3]	1	Enable 50% duty cycle calibration at startup
PWM_CFG	0x1E [2:0]	3	PWM configuration parameters
SCRATCH_C_2	0x1F [23:0]	24	Customer scratch area 2
CLAMP_OUT [1]	0x29 [11:10]	2	Output of clamp block

[1] Read only.

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EEPROM Customer-Programmable Parameter Reference

Table 9: F3DB_DC: Address 0x1C, bits 2:0

Function	Filter Bandwidth Selects the filter bandwidth (3-dB frequency) for the digitized applied magnetic field signal, applied when passed to the digital system after analog front-end processing. This selection also sets the internal update rate.		
Syntax	Quantity of bits: 3		
Related Comments			
Values (typical)	Code	Bandwidth (Hz)	Internal Update Rate (kHz)
	0 1 2 3 4 5 6 7	2000 4000 2000 1000 500 250 Not recommended Not recommended	8 16 8 4 2 1 – –
Options	–		
Examples	–		

Table 10: CALIBRATE_PWM: Address 0x1E, bit 3

Function	PWM Calibration When CALIBRATE_PWM is set to logic 1, the device outputs a 50% duty cycle PWM output for 800 ms after power on.
Syntax	Quantity of bits: 1
Related Commands	PWM_MODE (see EEPROM Structure Section)
Values	0: Disable calibration (Default) 1: Enable calibration
Options	
Examples	The 50% duty cycle output after power on can be used to synchronize or calibrate the PWM output reading with an external controller.

Table 11: CLAMP_HIGH: Address 0x1C, bit 23:18

Function	Clamp Upper Limit Sets the percentage of the upper half of the Full Scale Output signal passed through at the end of the Digital Signal Processing stage.
Syntax	Quantity of bits: 6
Related Commands	CLAMP_LOW
Values	0x0: Default (Maximum specified value, $OUT_{CLP(H)}$) 0x3F: (Minimum specified value, $OUT_{CLP(H)}$)
Options	The factory-programmed default, $OUT_{CLP(H)init}$, is used if this parameter is not set.
Examples	

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Table 12: CLAMP_LOW: Address 0x1C, bit 17:12

Function	Clamp Lower Limit Sets the percentage of the lower half of the Full Scale Output signal passed through at the end of the Digital Signal Processing stage.
Syntax	Quantity of bits: 6
Related Commands	CLAMP_HIGH
Values	0x0: Default (Minimum specified value, $OUT_{CLP(L)}$) 0x3F: (Maximum specified value, $OUT_{CLP(L)}$)
Options	The factory-programmed default, $OUT_{CLP(L)init}$, is used if this parameter is not set.
Examples	

Table 13: PWM_CFG: Address 0x1E, bits 2:0

Function	PWM Carrier Frequency Sets the carrier frequency for PWM mode normal output (voltage response to applied magnetic field). Selected frequency determines maximum output resolution.		
Syntax	Quantity of bits: 3		
Related Comments			
Values (typical)	Code	PWM Frequency (kHz)	Maximum Output Resolution (bits)
	0 1 2 3 4 5 6 7	0.125 0.25 0.5 1 2 4 0.125 0.125	12 12 12 11 10 9 12 12
Options	–		
Examples	–		

Table 14: ID_C: Address 0x1B, bit 20:12

Function	Customer Identification Number Available register for identifying the ATS344.
Syntax	Quantity of bits: 9
Related Commands	SCRATCH_C
Values	Free-form
Options	Values do not affect device operation.
Examples	

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Table 15: OUTDRV_CFG: Address 0x1E, bit 20:18

Function	Output Signal Configuration Sets configuration of the output signal slew-rate control. Sets the ramp rate on the gate of the output driver, thereby changing slew rate at the output.		
Syntax	Quantity of bits: 3		
Related Commands			
Values			
Options	**Code**	**Typical Rise Time (ns)**	**Typical Fall Time (ns)**
	0	323	331
	1	327	389
	2	327	389
	3	354	560
	4	327	389
	5	354	560
	6	354	560
	7	478	761
Examples			

Table 16: OUTPUT_INVERT: Address 0x1B, bit 22

Function	Output Polarity Inversion Inverts the polarity of the device output.
Syntax	Quantity of bits: 1
Related Commands	
Values	0:Positive output polarity. Left channel minus Right channel greater than zero. 1:Negative output polarity. Left channel minus Right channel less than zero.
Options	
Examples	

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Table 17: QVODC: Address 0x1D, bit 11:0

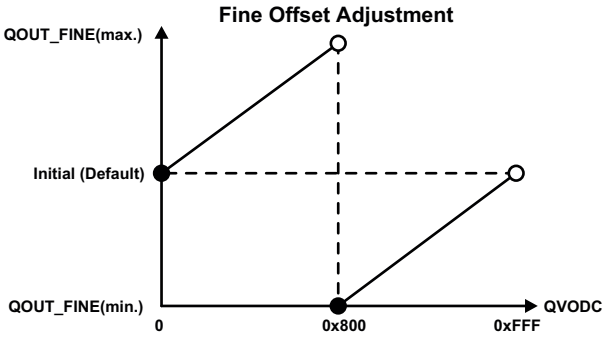
Function	Quiescent Output (QVO) Adjusts the device normal output (digital response to applied magnetic field) to set the baseline output level: for a quiescent applied magnetic field (differential input field ≈ 0 G).
Syntax	Quantity of bits: 12 Code stored in two's complement format
Related Commands	SENSDC
Values	
Options	
Examples	

Table 18: SCRATCH_C_0: Address 0x0A, bits 23:12
SCRATCH_C_1: Address 0x1D, bits 23:12
SCRATCH_C_2: Address 0x1F, bits 23:0

Function	Customer Scratchpad For optional customer use in storing values in the device.
Syntax	Quantity of bits: SCRATCH_C_0, 12 SCRATCH_C_1, 12 SCRATCH_C_2, 24
Related Commands	IC
Values	Free-form field
Options	Values do not affect device operation
Examples	

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Table 19: DBOFFDC: Address 0x09, bits 7:0

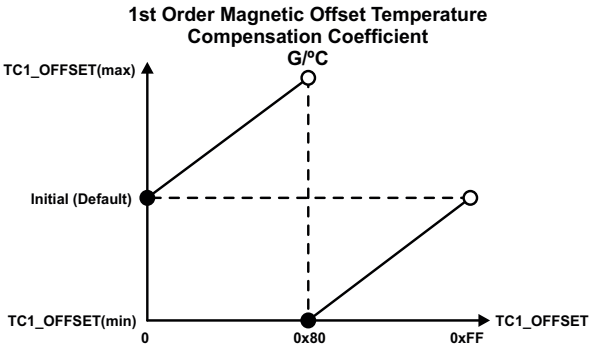
Function	1st Order Magnetic Offset Temperature Compensation coefficient See Temperature Compensation section for more details.
Syntax	Quantity of bits: 8 Code stored in two's complement format.
Related Commands	TC1_SENS_CLD, TC1_SENS_HOT, TC2_SENS_CLD, TC2_SENS_HOT
Values	
Options	
Examples	

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Table 20: TC1_SENS_CLD: Address 0x09, bits 15:8
TC1_SENS_HOT: Address 0x09, bits 23:16

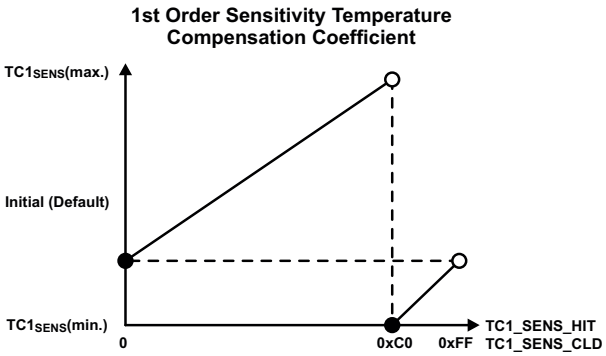
Function	1st Order Magnetic Offset Temperature Compensation coefficient See Temperature Compensation section for more details.
Syntax	Quantity of bits: 8 Code stored in shifted two's complement format.
Related Commands	TC1_SENS_CLD, TC1_SENS_HOT, TC2_SENS_CLD, TC2_SENS_HOT
Values	
Options	
Examples	The factory-programmed default, $\Delta Sens_{init}$, is used if neither these parameters, nor the TC2_SENS_HOT, TC2_SENS_CLD parameters, are set.

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Table 21: TC2_SENS_CLD: Address 0x08, bits 14:6
TC2_SENS_HOT: Address 0x08, bits 23:15

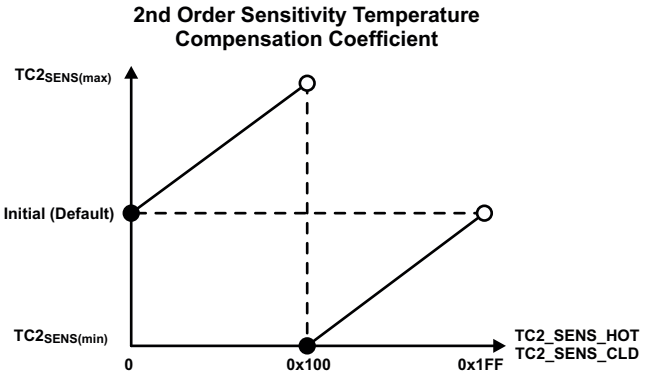
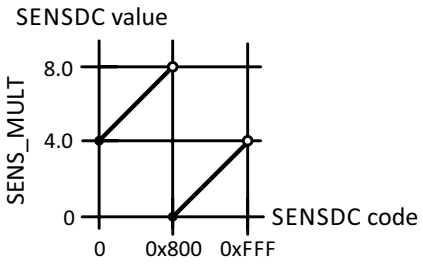
Function	2nd Order Sensitivity Temperature Coefficient. Refer to Temperature Compensation section for more details. Two different parameters are set, one for increasing values relative to T_A = 25°C, and the other for decreasing values, as follows: TC2_SENS_HOT: ΔT_A (from 25°C) > 0 TC2_SENS_CLD: ΔT_A (from 25°C) < 0
Syntax	Quantity of bits: 9 Code stored in two's complement format.
Related Commands	TC1_SENS_HOT, TC1_SENS_CLD
Values	
Options	
Examples	The factory-programmed default, $\Delta Sens_{init}$, is used if neither these parameters, nor the TC1_SENS_HOT, TC1_SENS_CLD parameters, are set.

Table 22: SENSDC: Address 0x0A, bits 11:0

Function	Customer Sensitivity Setting
Syntax	Quantity of bits: 12 Code stored in two's complement format.
Related Commands	
Values	
Options	SENS_MULT values in the figure represent a Sensitivity multiplier relative to the initial Sensitivity, $Sens_{init}$, and are not absolute Sensitivity values.
Examples	

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DEFINITIONS OF TERMS

General Programming
  Programming Range
  Full-Scale Output, FSO
Timing
  Power-On Time, t_{PO}
  Signal Response Time
Quiescent Field Response Baseline
  Offset Output, QOUT
  Clamp Programming Range
Device Response to Target Deflection
  Sensitivity, Sens
Device Accuracy
  Quiescent Output Drift Through Temperature Range
  Sensitivity Drift Through Temperature Range

General Programming

PROGRAMMING RANGE

The values of a programmable parameter that are within a central range bounded by the distributions of the values that could result from programming the minimum and maximum codes available for that parameter (see Figure 17). Because the endpoints of a programmable range have normal distributions, they are excluded from the range of values. The limits of the range are indicated by the minimum and maximum values in the Operating Characteristics table. For customer-programmable parameters, the typical default initial value lies within the programming range, and usually serves as the reference point for setting value ranges.

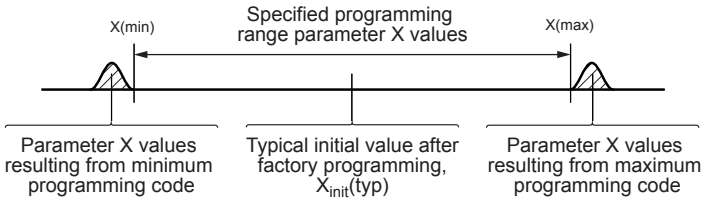

Figure 17: Definition of a Programming Range

FULL-SCALE OUTPUT, FSO

The available output range of the ATS344 is defined as the full scale output, FSO. The default FSO is region bound by $OUT_{CLP(L)(min.)}$ and $OUT_{CLP(H)(max.)}$. See Figure 18.

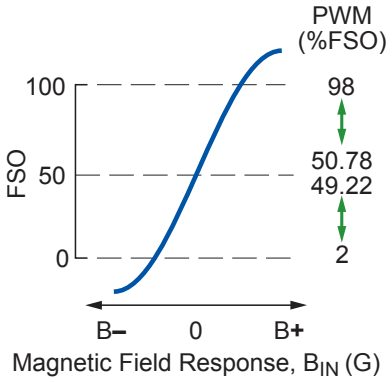

Figure 18: Full-Scale Output (FSO)

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Timing

POWER-ON-TIME, t_{PO}

The time required for device output to begin the transmission of the first valid duty cycle (PWM mode), after the power supply has reached its minimum specified operating voltage, V_{CC}(min). When the supply is ramped to its operating voltage, the device requires a finite time to power internal circuits before supplying a valid output value.

SIGNAL RESPONSE TIME

Typically Signal Response Time is defined as propagation delay, t_{SDLY}, plus length of the PWM message. However if filter bandwidth is chosen such that the corresponding internal output update rate (see BW parameter in EEPROM) is slower than the output digital message length, it might take a couple of output messages to update the user.

Quiescent Field Response Baseline

OFFSET OUTPUT, QOUT

The output value in the quiescent state (when no target deflection is applied; that is, magnetic response, $B_{SIG} = 0$).

CLAMP PROGRAMMING RANGE

The range of values that device digital processing is customer-programmed (EEPROM parameters CLAMP_HIGH and CLAMP_LOW) to optimize what segment of the processed Full Scale Input is scaled to the Full Scale Output. This determines the extent of truncation of the high and low peaks of the output of the Digital Signal Processing stage before input to the PWM engine in the output stage. (Note: This function is not related to the supply Zener clamp, for $V_{ZSUPPLY}$, and the output Zener clamp, for V_{ZOUT}, which are hardware overvoltage protection features.)

Device Response to Target Deflection

SENSITIVITY, SENS

Sensitivity is defined as the change in % duty cycle versus change in differential magnetic input signal, equation 4:

$$\text{Sens} = \frac{\text{Output}_A\,(\%D) - \text{Output}_B\,(\%D)}{B_{SIGA}\,(G) - B_{SIGB}\,(G)} \quad . \qquad (4)$$

Sensitivity is programmed in the factory to reflect the target operating range of +4 mm to –4 mm of deflection.

Device Accuracy

QUIESCENT OUTPUT DRIFT THROUGH TEMPERATURE RANGE

Due to internal component tolerances and thermal considerations, the temperature coefficient used to determine Quiescent Output may drift from its typical initial value, $QOUT_{init}$, when changes occur in the operating ambient temperature, T_A. For purposes of specification, the Quiescent Output Drift Through Temperature Range, $\Delta QOUT_{(\Delta T)}$, is defined as:

$$\Delta QOUT_{(\Delta T)} = QOUT_{(TA)} - QOUT_{(25°C)} \qquad (5)$$

where $QOUT_{(TA)}$ is the QOUT at a given T_A and $QOUT_{(25°C)}$ is the QOUT at a T_A of 25°C. Note that $\Delta QOUT_{(\Delta T)}$ should be calculated using actual measured values.

SENSITIVITY DRIFT THROUGH TEMPERATURE RANGE

Due to internal component tolerances and thermal considerations, the temperature coefficient used to determine Sensitivity may drift from its typical initial value, $Sens_{TCinit}$, and the expected value after customer programming (EEPROM parameters TC_SENS_CLD and TC_SENS_HOT), when changes occur in the operating ambient temperature, T_A. For purposes of specification, the Sensitivity Drift Through Temperature Range, $\Delta Sens_{TC}$, is defined as:

$$\Delta\text{Sens}_{TC} = \frac{\text{Sens}_{TA} - \text{Sens}_{EXPECTED(TA)}}{\text{Sens}_{EXPECTED(TA)}} \times 100\ (\%) \quad . \qquad (6)$$

where $Sens_{TA}$ is the actual Sens at the current ambient temperature, and $Sens_{EXPECTED(TA)}$ is the Sens calculated based on programmed parameters.

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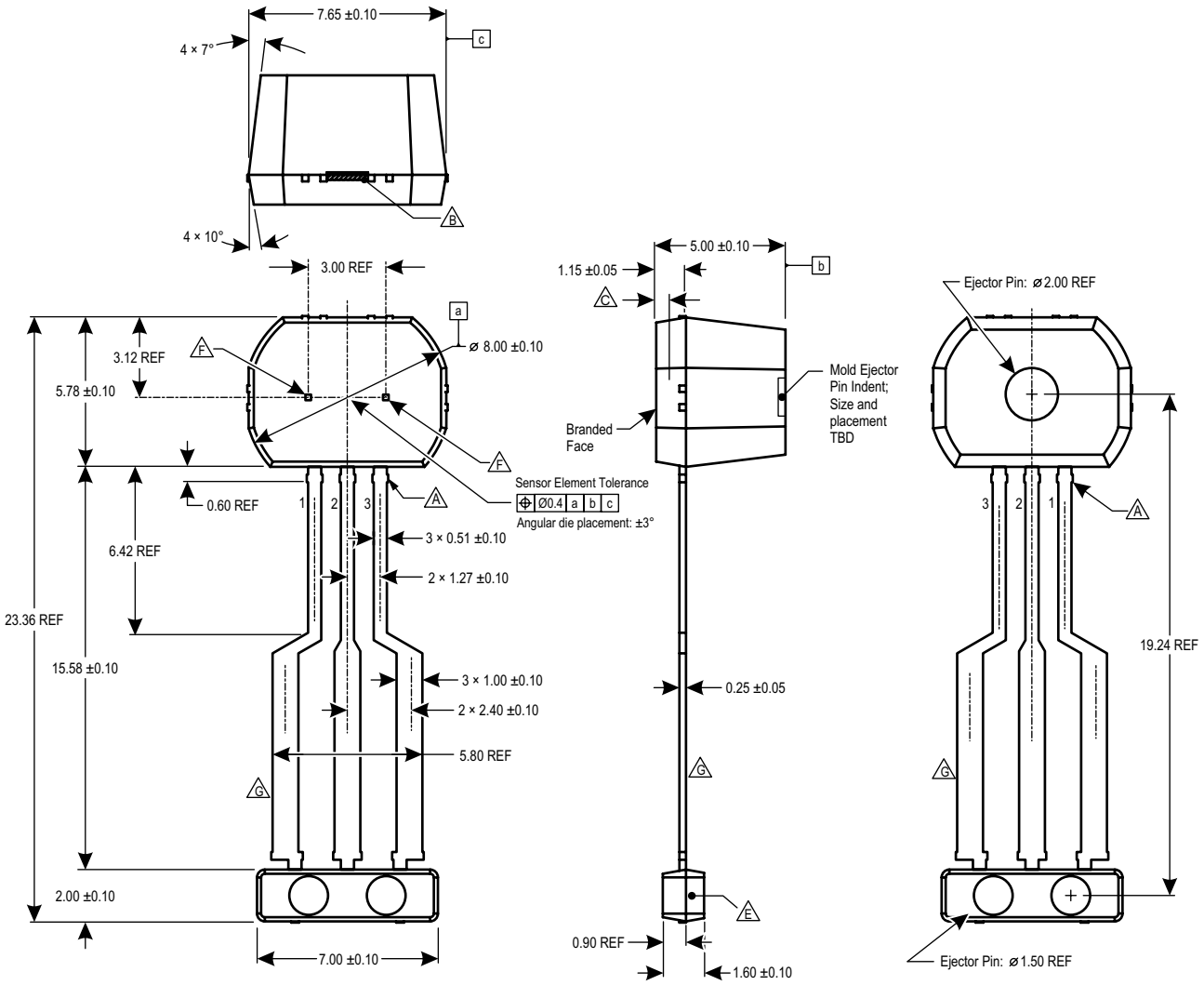
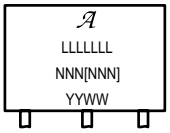
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





D Standard Branding Reference View

= Supplier emblem
L = Lot identifier
N = Last three numbers of device part number and optional subtype codes
Y = Last two digits of year of manufacture
W = Week of manufacture

A Dambar removal protrusion (12×)
B Gate and tie burr area
C Active Area Depth, 0.40 ±0.05 mm
D Branding scale and appearance at supplier discretion
E Thermoplastic Molded Lead Bar for alignment during shipment
F Hall elements (not to scale)
G 100% matte tin plating, thickness = 300 – 800 micro-inches. There may not be tin plating ion areas that are trimmed.

Figure 19: Package SP, 3-Pin SIP

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Revision History

Number	Date	Description
–	December 8, 2017	Initial release
1	August 8, 2018	Updated Offset Drift Over Lifetime (page 7)
2	August 22, 2019	Minor editorial updates

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