01115

Am9334

8-Bit Addressable Latch

Distinctive Characteristics

- All eight outputs available
- Serial-to-parallel storage
- Addressable data entry
- Active LOW common clear
- One-of-eight decoder
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am9334 is an 8-bit addressable latch featuring four separate modes of operation. These are: addressable latch, memory, eight-channel demultiplexer and clear. The Am9334 contains eight separate latches with active-LOW common clear and active-LOW input enable on the single data input.

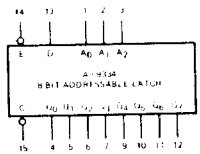
ADDRESSABLE LATCH: When the enable is LOW and the clear is HIGH, the addressed latch output follows the data input. The addressed latch stores the last data input when the enable goes HIGH. The seven non-addressed latches remain unchanged. The three address lines should remain unchanged while the enable is LOW in this mode.

MEMORY: When the enable and clear are HIGH, all eight latches retain their previous state and are unaffected by either the data or address inputs. To avoid transient wrong address codes, this mode should be used while changing the address inputs when operating the Am9334 as an addressable latch.

DEMULTIPLEXER: With the enable and clear both LOW, the addressed latch output follows the data input. The seven non-addressed outputs remain LOW. Thus, when the data input is HIGH, the addressed latch output is uniquely HIGH.

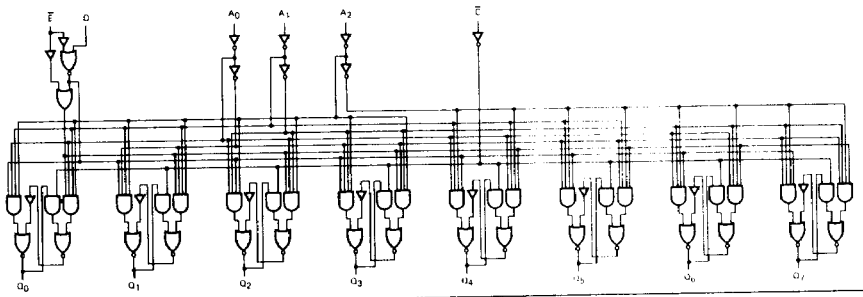
CLEAR: When the enable is HIGH and the clear is brought LOW, all eight latch outputs are forced LOW regardless of other inputs.

LOGIC SYMBOL



V_{CC} - Pin 16
GND - Pin 8

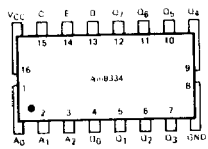
LOGIC DIAGRAM



Am9334 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded Plastic DIP	0°C to +75°C	9334PC
Hermetic DIP	0°C to +75°C	9334DC
Dice	0°C to +75°C	9334XC
Hermetic DIP	-55°C to +125°C	9334DM
Hermetic Flat Pak	-55°C to +125°C	9334FM
Dice	-55°C to +125°C	9334XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM INGS (Above which the useful life may be impaired)

Storage Temp.	
Temperature (Ambient) Under Bias	−65°C to +150°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−55°C to +125°
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +7
DC Input Voltage	−0.5V to +V_{CC} max
Output Current, Into Outputs	−0.5V to +5.5
DC Input Current	30 m
	−30 mA to +5.0 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am9334XC T_A = 0°C to +75°C V_{CC} = 5.0 V ± 5%
Am9334XM T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10%

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.72 mA, V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 9.6 mA, V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		4.0	40	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−30	−65	−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		56	86	mA

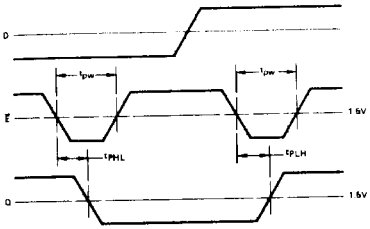
Notes: 1. Typical Limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Switching Characteristics (T_A = 25°C)

Parameters	Description	Test Conditions	Limits Min.	Typ.	Max.	Units
t_{PLH}	Turn-Off Delay Enable to Output	V_{CC} = 5.0 V, C_L = 15 pF, (See Figure 1)		16	23	ns
t_{PHL}	Turn-On Delay Enable to Output			15	24	
t_{PLH}	Turn-Off Delay Data to Output	V_{CC} = 5.0 V, C_L = 15 pF, (See Figure 2)		28	35	ns
t_{PHL}	Turn-On Delay Data to Output			16	24	
t_{PLH}	Turn-Off Delay Address to Output	V_{CC} = 5.0 V, C_L = 15 pF, (See Figure 3)			35	ns
t_{PHL}	Turn-On Delay Address to Output				35	
t_{PHL}	Turn-On Delay Clear to Output	V_{CC} = 5.0 V, C_L = 15 pF, (See Figure 5)		21		ns
t_s(H)	Set-up Time HIGH Data to Enable	V_{CC} = 5.0 V, (See Figure 4)	20	13		ns
t_h(H)	Hold Time HIGH Data to Enable (See Note 5)		0	−10		
t_s(L)	Set-up Time LOW Data to Enable		17	10		ns
t_h(L)	Hold Time LOW Data to Enable (See Note 5)		0	−13		
t_s(A-$\overline{E}$)	Set-up Time Address to Enable (See Note 3)	V_{CC} = 5.0 V, (See Figure 6)	5	0		ns
t_{pw}($\overline{E}$)	Enable Pulse Width	V_{CC} = 5.0 V, (See Figure 1)	17	11		ns

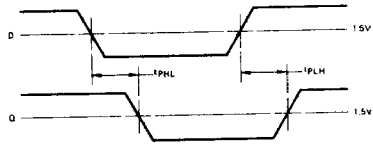
Notes: 3. The Address to enable set-up time is the time before the HIGH-to-LOW enable transition that the address must be stable so that the correct latch is addressed and the other latches are not affected.
4. The cross hatched areas indicate when the inputs are permitted to change for predictable output performance.
5. Another way of specifying a negative hold time is to specify a positive release time. When specified, the release time falls within the set-up interval time thereby giving the equivalent of a negative hold time.

SWITCHING TEST TIME WAVEFORMS



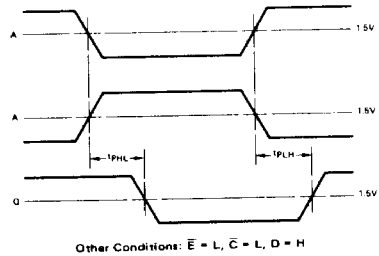
Other Conditions: $\overline{C}$ = H, A = Stable

Figure 1. Turn-On & Turn-Off Delays Enable to Output and Enable Pulse Width



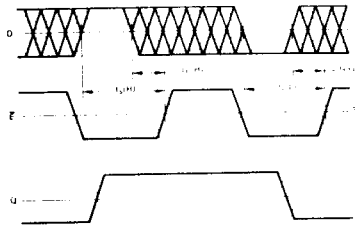
Other Conditions: $\overline{E}$ = L, $\overline{C}$ = H, A = Stable

Figure 2. Turn-On & Turn-Off Delays Data to Output



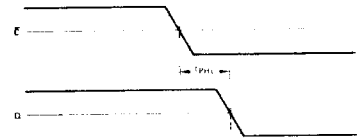
Other Conditions: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Figure 3. Turn-On & Turn-Off Delays Address to Output



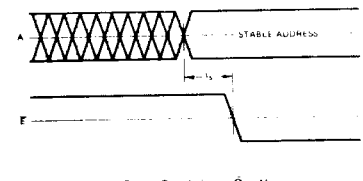
Other Conditions: $\overline{C}$ = H, A = Stable

Figure 4. Set-up & Hold Time Data to Enable (See Notes 4 & 5)



Other Conditions: $\overline{E}$ = H

Figure 5. Turn-On Delay Clear to Output



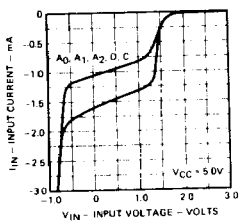
Other Conditions: $\overline{C}$ = H

Figure 6. Set-up Time Address to Enable (See Note 4)

PERFORMANCE CURVES

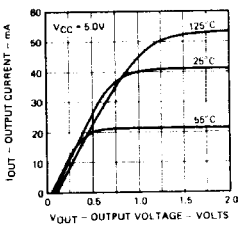
INPUT/OUTPUT CHARACTERISTICS

Input

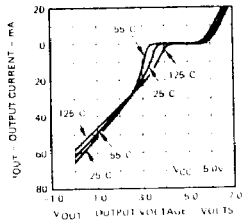


Output

Low State



High State



DEFINITION OF TERMS

SUBSCRIPT TER.

H HIGH, applyin. HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS

A_{0-2} Write address field. Data on D is written into the location specified by the A address field.

$\overline{E}$ On going from a HIGH logic level to a LOW logic level (clear HIGH), the addressed latch output will follow the information on the D input. When the enable input goes from a LOW logic level to a HIGH logic level, the data on the D input is stored in the addressed latch.

$\overline{C}$ The clear input is used in conjunction with the enable input to select the operating mode of the device. See the mode selection table for definition of states.

D Information on the D input is written into the latch specified by the A address field when the enable goes from a LOW logic level to a HIGH logic level.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to 40μA at 2.4 V and in the LOW state it is equal to −1.6mA at 0.4 V.

Q_{0-7} The eight individual latch outputs.

OPERATIONAL TERMS

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{CC} The current drawn by the device from V_{CC} power supply with input and output terminals open.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{IN} Input voltage applied in I_{IL}, I_{IH} tests.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS

t_{PLH} Propagation delay time for LOW-to-HIGH output transition. The time between the specified reference points on the input and output voltage waveforms (TTL = 1.5 volts) with the output changing from the LOW level to the HIGH level.

t_{PHL} Propagation delay time for HIGH-to-LOW output transition. The time between the specified reference points on the input and output voltage waveforms (TTL = 1.5 volts) with the output changing from the HIGH level to the LOW level.

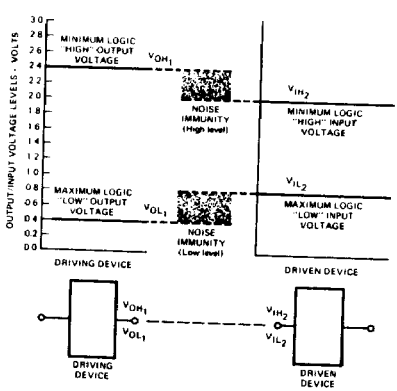
t_h Hold time. The time interval for which a signal is retained at a specified level for a specified input terminal after an active transition occurs at another specified input terminal.

t_s Set-up time. The time interval for which a signal must be applied and maintained at a specified level for a specified input terminal before an active transition occurs at another specified input terminal.

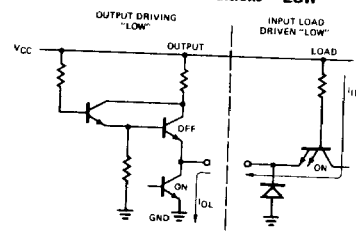
t_{pw} The minimum LOW enable pulse width required to write data into the addressed latch. Refer to Figure 1.

INPUT/OUTPUT INTERFACE CONDITIONS

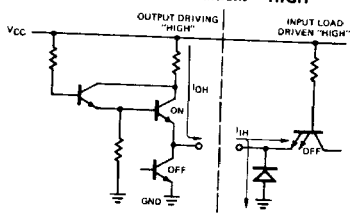
Voltage Interface Conditions – LOW & HIGH



Current Interface Conditions – LOW



Current Interface Conditions – HIGH



MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400 Series	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Output LOW
A_0	1	1		
A_1	2	1		
A_2	3	1		
Q_0	4		18	6
Q_1	5		18	6
Q_2	6		18	6
Q_3	7		18	6
GND	8			
Q_4	9		18	6
Q_5	10		18	6
Q_6	11		18	6
Q_7	12		18	6
D	13	1		
$\bar{E}$	14	1.5		
$\bar{C}$	15	1		
V_{CC}	16			

FUNCTION TABLE

$\bar{E}$	$\bar{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

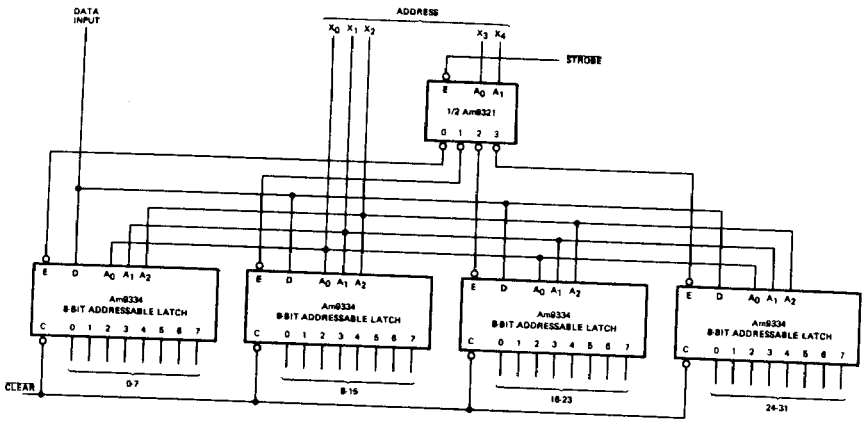
TRUTH TABLE

Input States						Present Output States								
$\bar{C}$	$\bar{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
.	.	.		.					.					
.	.	.		.					.					
L	L	L	H	H	H	L	L	L	L	L	L	L	L	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}								MEMORY
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}					ADDRESSABLE
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}						LATCH
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}						
.	.	.		.										
.	.	.		.										
.	.	.		.										
H	L	L	H	H	H	Q_{N-1}						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}						Q_{N-1}	H	

X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

APPLICATIONS

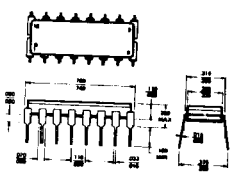
32-BIT ADDRESSABLE LATCH AND 1-OF-32 DECODER/DEMULTIPLEXER



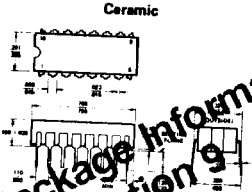
PHYSICAL DIMENSIONS

Dual-In-Line

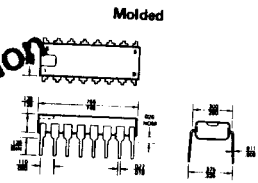
Hermetic



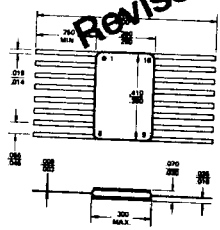
Ceramic



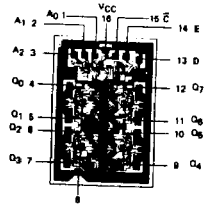
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE 0.065" x 0.096"

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

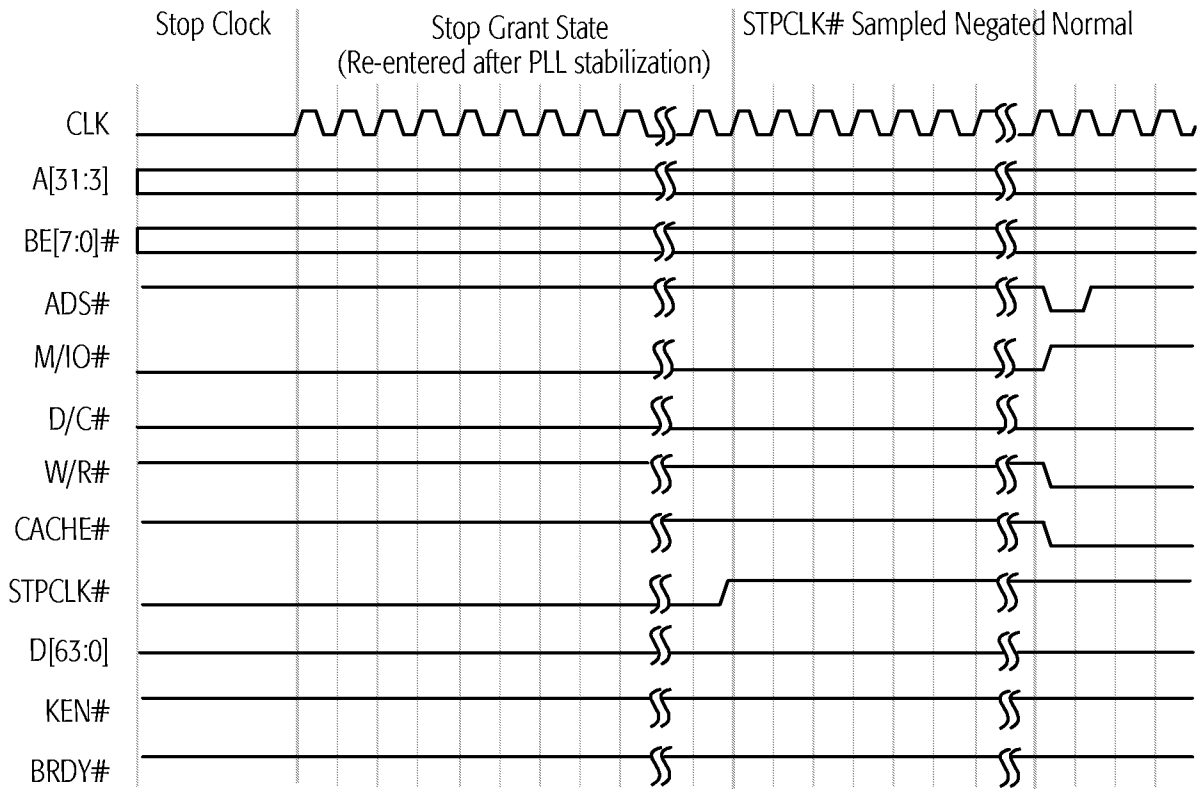


Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

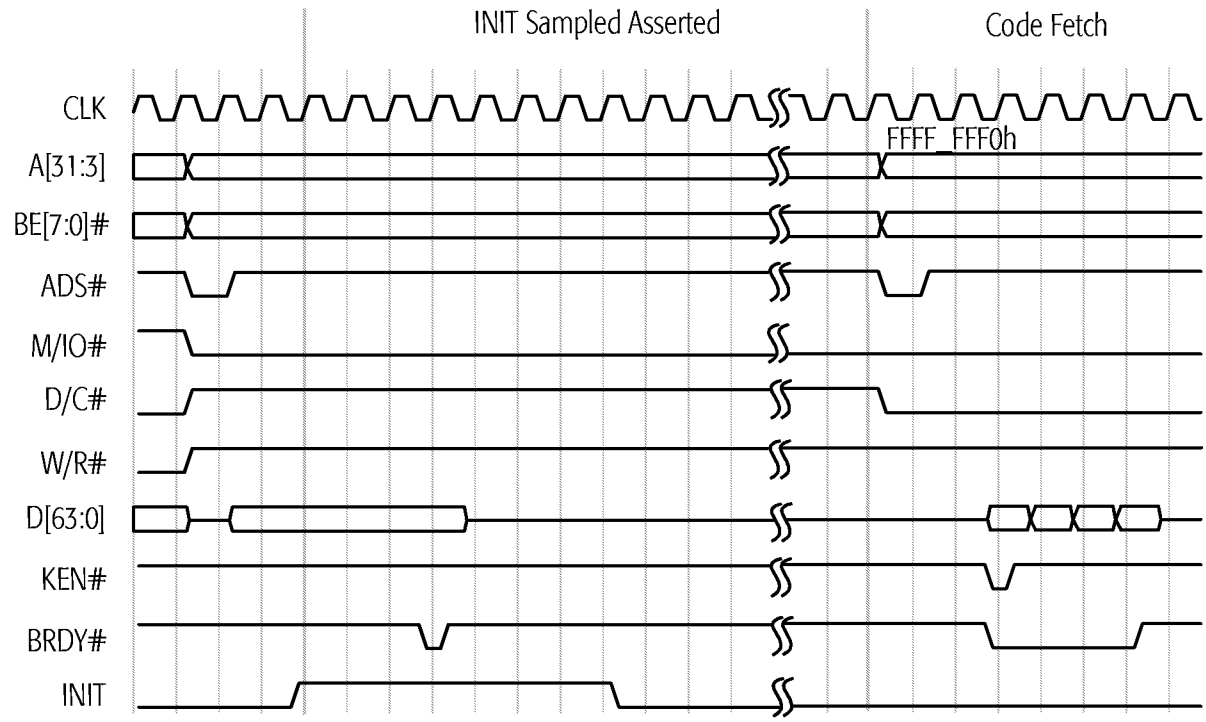


Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.