# S-8239A Series

## OVERCURRENT MONITORING IC FOR MULTI-SERIAL-CELL PACK

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Rev.1.6_00

The S-8239A Series is an overcurrent monitoring IC for multi-serial-cell pack including high-accuracy voltage detection circuits and delay circuits.
The S-8239A Series is suitable for protection of lithium-ion / lithium polymer rechargeable battery packs from overcurrent.

## ■ Features

- Built-in high-accuracy voltage detection circuit
  
  | | | |
  |---|---|---|
  | Overcurrent 1 detection voltage[1] | 0.04 V to 0.30 V (10 mV step) | Accuracy ±15 mV |
  | Overcurrent 2 detection voltage | 0.1 V to 0.7 V (100 mV step) | Accuracy ±100 mV |
  | Overcurrent 3 detection voltage | 1.2 V (Fixed) | Accuracy ±300 mV |

- Built-in three-step overcurrent detection circuit: Overcurrent 1, overcurrent 2, overcurrent 3
- Overcurrent 3 detection function:        Available, unavailable
- UVLO (under voltage lock out) function
  
  UVLO detection voltage        2.0 V (Fixed)        Accuracy ±100 mV
- High-withstand voltage:        VM pin, DO pin: Absolute maximum rating 28 V
- Delay times are generated only by an internal circuit (External capacitors are unnecessary).
- Low current consumption
  
  During normal operation:        7.0 μA max.
  During UVLO operation:        6.0 μA max.
- Output logic:        Active "L", Active "H"
- Wide operation temperature range:        Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

  *1. Overcurrent 1 detection voltage ≤ 0.06 V should be satisfied in the case of overcurrent 2 detection voltage = 0.1 V. Overcurrent 1 detection voltage ≤ 0.85 × overcurrent 2 detection voltage − 0.05 V should be satisfied in the case of overcurrent 2 detection voltage ≥ 0.2 V.
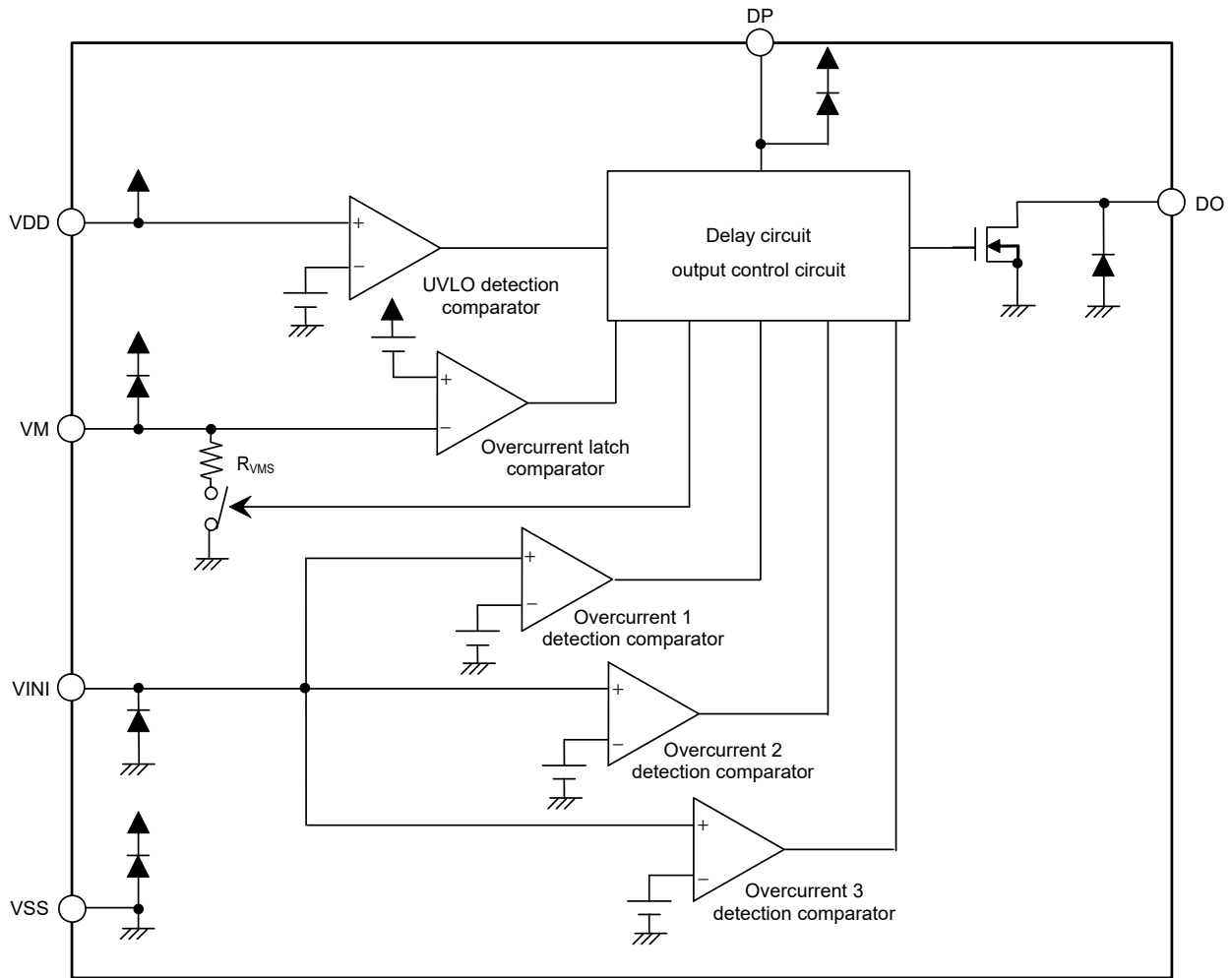
## ■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack
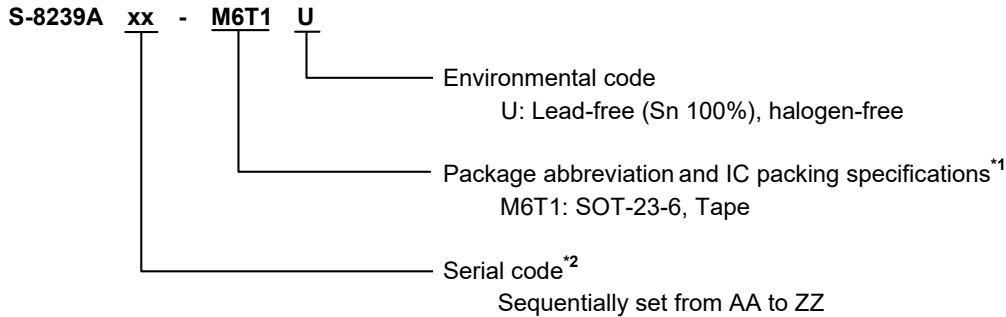
## ■ Package

- SOT-23-6

## ■ Block Diagram



**Remark** All the diodes shown in the figure are parasitic diodes.

**Figure 1**

# ■ Product Name Structure

## 1. Product name

S-8239A  xx  -  **M6T1**  **U**

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free

- Package abbreviation and IC packing specifications[1]
  - M6T1: SOT-23-6, Tape

- Serial code[2]
  - Sequentially set from AA to ZZ

**[1].** Refer to the tape drawing.
**[2].** Refer to "**3. Product name list**".

## 2. Package

**Table 1  Package Drawing Codes**

| Package Name | Dimension | Tape | Reel |
|---|---|---|---|
| SOT-23-6 | MP006-A-P-SD | MP006-A-C-SD | MP006-A-R-SD |

## 3. Product name list

**Table 2**

| Product Name | Overcurrent 1 Detection Voltage [$V_{DIOV1}$] | Overcurrent 2 Detection Voltage [$V_{DIOV2}$] | Overcurrent 1 Detection Delay Time [$t_{DIOV1}$] | Overcurrent 2 Detection Delay Time [$t_{DIOV2}$] | Overcurrent 3 Detection Function | Output Logic |
|---|---|---|---|---|---|---|
| S-8239AAA-M6T1U | 0.08 V | 0.4 V | 1150 ms | 1.12 ms | Unavailable | Active "L" |
| S-8239AAB-M6T1U | 0.10 V | 0.5 V | 1150 ms | 0.28 ms | Unavailable | Active "L" |
| S-8239AAC-M6T1U | 0.10 V | 0.3 V | 18.0 ms | 0.28 ms | Unavailable | Active "L" |
| S-8239AAD-M6T1U | 0.10 V | 0.2 V | 290 ms | 0.56 ms | Unavailable | Active "L" |
| S-8239AAE-M6T1U | 0.10 V | 0.7 V | 18.0 ms | 0.56 ms | Unavailable | Active "L" |
| S-8239AAF-M6T1U | 0.04 V | 0.3 V | 4600 ms | 0.28 ms | Unavailable | Active "L" |
| S-8239AAG-M6T1U | 0.10 V | 0.2 V | 1150 ms | 1.12 ms | Available | Active "L" |
| S-8239AAH-M6T1U | 0.06 V | 0.1 V | 290 ms | 0.56 ms | Unavailable | Active "L" |
| S-8239AAI-M6T1U | 0.10 V | 0.3 V | 290 ms | 0.28 ms | Unavailable | Active "L" |
| S-8239AAJ-M6T1U | 0.11 V | 0.3 V | 4600 ms | 2.24 ms | Available | Active "L" |
| S-8239AAK-M6T1U | 0.10 V | 0.3 V | 290 ms | 1.12 ms | Available | Active "H" |
| S-8239AAL-M6T1U | 0.06 V | 0.2 V | 290 ms | 1.12 ms | Unavailable | Active "L" |
| S-8239AAM-M6T1U | 0.06 V | 0.1 V | 1150 ms | 9.00 ms | Available | Active "L" |
| S-8239AAN-M6T1U | 0.07 V | 0.2 V | 290 ms | 0.56 ms | Available | Active "L" |
| S-8239AAO-M6T1U | 0.30 V | 0.6 V | 4600 ms | 143 ms | Available | Active "L" |
| S-8239AAP-M6T1U | 0.10 V | 0.2 V | 36 ms | 0.56 ms | Unavailable | Active "L" |

**Remark**  Contact our sales representatives for products other than the above.
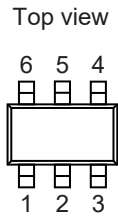
# ■ Pin Configuration

### 1. SOT-23-6

Top view

```
6  5  4
┌─────────┐
│         │
└─────────┘
1  2  3
```

**Figure 2**

**Table 3**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VINI | Voltage detection pin between VINI pin and VSS pin (Overcurrent detection pin) |
| 2 | VM | Overcurrent latch pin |
| 3 | DO | Connection pin of discharge control FET gate |
| 4 | DP[*1] | Test pin for delay time measurement |
| 5 | VDD | Input pin for positive power supply |
| 6 | VSS | Input pin for negative power supply |

***1.** The DP pin should be open.

■ **Absolute Maximum Ratings**

**Table 4**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Applied pin | Absolute Maximum Rating | Unit |
|---|---|---|---|---|
| Input voltage between VDD pin and VSS pin | $V_{DS}$ | VDD | $V_{SS} - 0.3$ to $V_{SS} +12$ | V |
| VM pin input voltage | $V_{VM}$ | VM | $V_{DD} - 28$ to $V_{DD} + 0.3$ | V |
| VINI pin input voltage | $V_{VINI}$ | VINI | $V_{SS} - 0.3$ to $V_{SS} + 12$ | V |
| DO pin output voltage | $V_{DO}$ | DO | $V_{SS} - 0.3$ to $V_{SS} + 28$ | V |
| Power dissipation | $P_D$ | – | 650[*1] | mW |
| Operation ambient temperature | $T_{opr}$ | – | $-40$ to $+85$ | °C |
| Storage temperature | $T_{stg}$ | – | $-55$ to $+125$ | °C |

**\*1.** When mounted on board

    [Mounted board]

      (1) Board size:     114.3 mm $\times$ 76.2 mm $\times$ t1.6 mm

      (2) Board name:     JEDEC STANDARD51-7

**Caution**   **1.** The DP pin should be open.

          **2.** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.
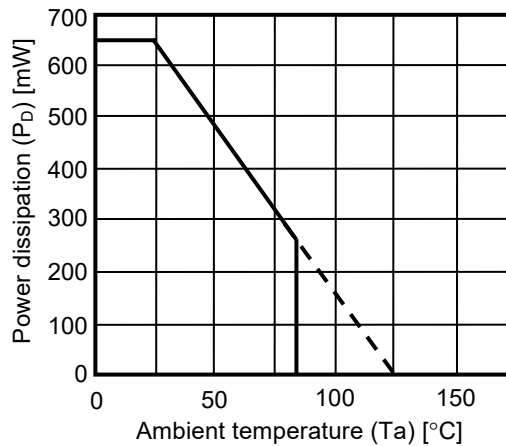


**Figure 3  Power Dissipation of Package (When Mounted on Board)**

## ■ Electrical Characteristics

### 1. Ta = +25°C

**Table 5**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| **Detection Voltage** | | | | | | | | |
| Overcurrent 1 detection voltage | $V_{DIOV1}$ | – | $V_{DIOV1}$ − 0.015 | $V_{DIOV1}$ | $V_{DIOV1}$ + 0.015 | V | 1 | 1 |
| Overcurrent 2 detection voltage[*1] | $V_{DIOV2}$ | – | $V_{DIOV2}$ − 0.100 | $V_{DIOV2}$ | $V_{DIOV2}$ + 0.100 | V | 1 | 1 |
| Overcurrent 3 detection voltage | $V_{DIOV3}$ | With overcurrent 3 detection function | 0.90 | 1.20 | 1.50 | V | 1 | 1 |
| UVLO detection voltage | $V_{UVLO}$ | – | 1.90 | 2.00 | 2.10 | V | 1 | 1 |
| **Release Voltage** | | | | | | | | |
| Overcurrent release voltage | $V_{RIOV}$ | $V_{DD}$ criteria, $V_{DD}$ = 3.5 V | 0.7 | 1.2 | 1.5 | V | 1 | 1 |
| **Input Voltage, Operation Voltage** | | | | | | | | |
| Operation voltage between VDD pin and VSS pin | $V_{DSOP}$ | Output logic is determined[*2] | 1.5 | – | 8 | V | – | – |
| **Current Consumption** | | | | | | | | |
| Current consumption during normal operation | $I_{OPE}$ | $V_{DD}$ = 3.5 V, $V_{VM}$ = 0 V | 1.0 | 3.5 | 7.0 | μA | 2 | 2 |
| Current consumption during UVLO operation | $I_{UVLO}$ | $V_{DD}$ = $V_{VM}$ = 1.5 V | 0.7 | 3.0 | 6.0 | μA | 2 | 2 |
| **Internal Resistance** | | | | | | | | |
| Internal resistance between VM pin and VSS pin | $R_{VMS}$ | $V_{DD}$ = $V_{VM}$ = 3.5 V | 210 | 300 | 390 | kΩ | 3 | 3 |
| **Output Resistance (Active "L")** | | | | | | | | |
| DO pin resistance "L" | $R_{DOL}$ | $V_{DD}$ = $V_{VINI}$ = 3.5 V, $V_{DO}$ = 0.5 V | 2.5 | 5 | 10 | kΩ | 4 | 4 |
| **Output Resistance (Active "H")** | | | | | | | | |
| DO pin resistance "L" | $R_{DOL}$ | $V_{DD}$ = 3.5 V, $V_{VINI}$ = 0 V $V_{DO}$ = 0.5 V | 2.5 | 5 | 10 | kΩ | 4 | 4 |
| **Delay Time** | | | | | | | | |
| Overcurrent 1 detection delay time | $t_{DIOV1}$ | – | $t_{DIOV1}$ × 0.6 | $t_{DIOV1}$ | $t_{DIOV1}$ × 1.4 | ms | 5 | 5 |
| Overcurrent 2 detection delay time | $t_{DIOV2}$ | – | $t_{DIOV2}$ × 0.6 | $t_{DIOV2}$ | $t_{DIOV2}$ × 1.4 | ms | 5 | 5 |
| Overcurrent 3 detection delay time | $t_{DIOV3}$ | With overcurrent 3 detection function | 168 | 280 | 392 | μs | 5 | 5 |
| UVLO detection delay time | $t_{UVLO}$ | – | 2.94 | 4.90 | 6.86 | s | 5 | 5 |

***1.** Even if overcurrent 1 detection voltage and overcurrent 2 detection voltage are in the same range, $V_{DIOV1}$ is lower than $V_{DIOV2}$.

***2.** It indicates that DO pin output logic is determined.

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## 2. Ta = −40°C to +85°C[*1]

**Table 6**

(Ta = −40°C to +85°C[*1] unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Condition | Test Circuit |
|------|--------|-----------|------|------|------|------|----------------|--------------|
| **Detection Voltage** | | | | | | | | |
| Overcurrent 1 detection voltage | $V_{DIOV1}$ | – | $V_{DIOV1}$ − 0.021 | $V_{DIOV1}$ | $V_{DIOV1}$ + 0.021 | V | 1 | 1 |
| Overcurrent 2 detection voltage[*2] | $V_{DIOV2}$ | – | $V_{DIOV2}$ − 0.130 | $V_{DIOV2}$ | $V_{DIOV2}$ + 0.130 | V | 1 | 1 |
| Overcurrent 3 detection voltage | $V_{DIOV3}$ | With overcurrent 3 detection function | 0.70 | 1.20 | 1.70 | V | 1 | 1 |
| UVLO detection voltage | $V_{UVLO}$ | – | 1.85 | 2.00 | 2.15 | V | 1 | 1 |
| **Release Voltage** | | | | | | | | |
| Overcurrent release voltage | $V_{RIOV}$ | $V_{DD}$ criteria, $V_{DD}$ = 3.5 V | 0.5 | 1.2 | 1.7 | V | 1 | 1 |
| **Input Voltage, Operation Voltage** | | | | | | | | |
| Operation voltage between VDD pin and VSS pin | $V_{DSOP}$ | Output logic is determined[*3] | 1.5 | – | 8 | V | – | – |
| **Current Consumption** | | | | | | | | |
| Current consumption during normal operation | $I_{OPE}$ | $V_{DD}$ = 3.5 V, $V_{VM}$ = 0 V | 0.7 | 3.5 | 8.0 | μA | 2 | 2 |
| Current consumption during UVLO operation | $I_{UVLO}$ | $V_{DD}$ = $V_{VM}$ = 1.5 V | 0.5 | 3.0 | 7.0 | μA | 2 | 2 |
| **Internal Resistance** | | | | | | | | |
| Internal resistance between VM pin and VSS pin | $R_{VMS}$ | $V_{DD}$ = $V_{VM}$ = 3.5 V | 150 | 300 | 450 | kΩ | 3 | 3 |
| **Output Resistance (Active "L")** | | | | | | | | |
| DO pin resistance "L" | $R_{DOL}$ | $V_{DD}$ = $V_{VINI}$ = 3.5 V, $V_{DO}$ = 0.5 V | 1.2 | 5 | 15 | kΩ | 4 | 4 |
| **Output Resistance (Active "H")** | | | | | | | | |
| DO pin resistance "L" | $R_{DOL}$ | $V_{DD}$ = 3.5 V, $V_{VINI}$ = 0 V $V_{DO}$ = 0.5 V | 1.2 | 5 | 15 | kΩ | 4 | 4 |
| **Delay Time** | | | | | | | | |
| Overcurrent 1 detection delay time | $t_{DIOV1}$ | – | $t_{DIOV1}$ × 0.2 | $t_{DIOV1}$ | $t_{DIOV1}$ × 1.8 | ms | 5 | 5 |
| Overcurrent 2 detection delay time | $t_{DIOV2}$ | – | $t_{DIOV2}$ × 0.2 | $t_{DIOV2}$ | $t_{DIOV2}$ × 1.8 | ms | 5 | 5 |
| Overcurrent 3 detection delay time | $t_{DIOV3}$ | With overcurrent 3 detection function | 56 | 280 | 504 | μs | 5 | 5 |
| UVLO detection delay time | $t_{UVLO}$ | – | 0.98 | 4.90 | 8.82 | s | 5 | 5 |

**\*1.** Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

**\*2.** Even if overcurrent 1 detection voltage and overcurrent 2 detection voltage are in the same range, $V_{DIOV1}$ is lower than $V_{DIOV2}$.

**\*3.** It indicates that DO pin output logic is determined.

# ■ Test Circuits

**Caution**   Unless otherwise specified, the output voltage levels "H" and "L" at the DO pin ($V_{DO}$) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the DO pin level with respect to $V_{SS}$.

## 1. Overcurrent 1 detection voltage, overcurrent 2 detection voltage, overcurrent release voltage, UVLO detection voltage
(Test condition 1, test circuit 1)

### 1. 1  Active "L"

The overcurrent 1 detection voltage ($V_{DIOV1}$) is defined as the voltage V2 whose delay time for changing $V_{DO}$ from "H" to "L" lies between the minimum and the maximum value of the overcurrent 1 detection delay time after the voltage V2 is increased instantaneously (within 10 μs) from the set conditions of V1 = V3 = 3.5 V, V2 = 0 V.

The overcurrent 2 detection voltage ($V_{DIOV2}$) is defined as the voltage V2 whose delay time for changing $V_{DO}$ from "H" to "L" lies between the minimum and the maximum value of the overcurrent 2 detection delay time after the voltage V2 is increased instantaneously (within 10 μs) from the set conditions of V1 = V3 = 3.5 V, V2 = 0 V.

The overcurrent release voltage ($V_{RIOV}$) is defined as the voltage V3 at which $V_{DO}$ goes from "L" to "H" after decreasing V2 to 0 V and the voltage V3 is increased gradually from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

The UVLO detection voltage ($V_{UVLO}$) is defined as the voltage V1 at which $V_{DO}$ goes from "H" to "L" after the voltages V1 and V3 are decreased gradually from the set conditions of V1 = V3 = 3.5 V, V2 = 0 V.

### 1. 2  Active "H"

The overcurrent 1 detection voltage ($V_{DIOV1}$) is defined as the voltage V2 whose delay time for changing $V_{DO}$ from "L" to "H" lies between the minimum and the maximum value of the overcurrent 1 detection delay time after the voltage V2 is increased instantaneously (within 10 μs) from the set conditions of V1 = V3 = 3.5 V, V2 = 0 V.

The overcurrent 2 detection voltage ($V_{DIOV2}$) is defined as the voltage V2 whose delay time for changing $V_{DO}$ from "L" to "H" lies between the minimum and the maximum value of the overcurrent 2 detection delay time after the voltage V2 is increased instantaneously (within 10 μs) from the set conditions of V1 = V3 = 3.5 V, V2 = 0 V.

The overcurrent release voltage ($V_{RIOV}$) is defined as the voltage V3 at which $V_{DO}$ goes from "H" to "L" after decreasing V2 to 0 V and the voltage V3 is increased gradually from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

The UVLO detection voltage ($V_{UVLO}$) is defined as the voltage V1 at which $V_{DO}$ goes from "L" to "H" after the voltages V1 and V3 are decreased gradually from the set conditions of V1 = V3 = 3.5 V, V2 = 0 V.

## 2. Overcurrent 3 detection voltage (With overcurrent 3 detection function)
(Test condition 1, test circuit 1)

### 2. 1  Active "L"

The overcurrent 3 detection voltage ($V_{DIOV3}$) is defined as the voltage V2 whose delay time for changing $V_{DO}$ from "H" to "L" lies between the minimum and the maximum value of the overcurrent 3 detection delay time after the voltage V2 is increased instantaneously (within 10 μs) from the set conditions of V1 = V3 = 3.5 V, V2 = 0 V.

### 2. 2  Active "H"

The overcurrent 3 detection voltage ($V_{DIOV3}$) is defined as the voltage V2 whose delay time for changing $V_{DO}$ from "L" to "H" lies between the minimum and the maximum value of the overcurrent 3 detection delay time after the voltage V2 is increased instantaneously (within 10 μs) from the set conditions of V1 = V3 = 3.5 V, V2 = 0 V.

## 3. Current consumption during normal operation, current consumption during UVLO operation
(Test condition 2, test circuit 2)

The current consumption during normal operation ($I_{OPE}$) is the current that flows through the VDD pin ($I_{DD}$) under the set conditions of V1 = 3.5 V, V2 = 0 V.

The current consumption during UVLO operation ($I_{UVLO}$) is $I_{DD}$ under the set conditions of V1 = V2 = 1.5 V.

## 4. Internal resistance between VM pin and VSS pin
(Test condition 3, test circuit 3)

The internal resistance between the VM pin and the VSS pin ($R_{VMS}$) is the resistance between the VM pin and the VSS pin under the set condition of V1 = V2 = V3 = 3.5 V.

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### 5. DO pin resistance "L"
### (Test condition 4, test circuit 4)

#### 5. 1 Active "L"

The DO pin resistance "L" ($R_{DOL}$) is the DO pin resistance under the set conditions of V1 = V2 = 3.5 V, V3 = 0.5 V.

#### 5. 2 Active "H"

The DO pin resistance "L" ($R_{DOL}$) is the DO pin resistance under the set conditions of V1 = 3.5 V, V2 = 0 V, V3 = 0.5 V.

### 6. Overcurrent 1 detection delay time
### (Test condition 5, test circuit 5)

#### 6. 1 Active "L"

##### 6. 1. 1 $V_{DIOV2}$ = 0.1 V

The overcurrent 1 detection delay time ($t_{DIOV1}$) is the time period from when the voltage V2 exceeds $V_{DIOV1}$ to when $V_{DO}$ goes to "L", after V2 is increased to 0.08V instantaneously (within 10 μs) under the set conditions of V1 = 3.5 V, V2 = 0 V.

##### 6. 1. 2 $V_{DIOV2} \geq$ 0.2 V

The overcurrent 1 detection delay time ($t_{DIOV1}$) is the time period from when the voltage V2 exceeds $V_{DIOV1}$ to when $V_{DO}$ goes to "L", after V2 is increased to $V_{DIOV1}$ max. + 0.01 V instantaneously (within 10 μs) under the set conditions of V1 = 3.5 V, V2 = 0 V.

#### 6. 2 Active "H"

##### 6. 2. 1 $V_{DIOV2}$ = 0.1 V

The overcurrent 1 detection delay time ($t_{DIOV1}$) is the time period from when the voltage V2 exceeds $V_{DIOV1}$ to when $V_{DO}$ goes to "H", after V2 is increased to 0.08V instantaneously (within 10 μs) under the set conditions of V1 = 3.5 V, V2 = 0 V.

##### 6. 2. 2 $V_{DIOV2} \geq$ 0.2 V

The overcurrent 1 detection delay time ($t_{DIOV1}$) is the time period from when the voltage V2 exceeds $V_{DIOV1}$ to when $V_{DO}$ goes to "H", after V2 is increased to $V_{DIOV1}$ max. + 0.01 V instantaneously (within 10 μs) under the set conditions of V1 = 3.5 V, V2 = 0 V.

### 7. Overcurrent 2 detection delay time, UVLO detection delay time
### (Test condition 5, test circuit 5)

#### 7. 1 Active "L"

The overcurrent 2 detection delay time ($t_{DIOV2}$) is the time period from when the voltage V2 exceeds $V_{DIOV2}$ to when $V_{DO}$ goes to "L", after V2 is increased to 0.9 V instantaneously (within 10 μs) under the set conditions of V1 = 3.5 V, V2 = 0 V.
The UVLO detection delay time ($t_{UVLO}$) is the time period from when the voltage V1 falls below $V_{UVLO}$ to when $V_{DO}$ goes to "L", after V1 is decreased to 1.8 V instantaneously (within 10 μs) under the set conditions of V1 = 3.5 V, V2 = 0 V.

#### 7. 2 Active "H"

The overcurrent 2 detection delay time ($t_{DIOV2}$) is the time period from when the voltage V2 exceeds $V_{DIOV2}$ to when $V_{DO}$ goes to "H", after V2 is increased to 0.9 V instantaneously (within 10 μs) under the set conditions of V1 = 3.5 V, V2 = 0 V.
The UVLO detection delay time ($t_{UVLO}$) is the time period from when the voltage V1 falls below $V_{UVLO}$ to when $V_{DO}$ goes to "H", after V1 is decreased to 1.8 V instantaneously (within 10 μs) under the set conditions of V1 = 3.5 V, V2 = 0 V.

**8. Overcurrent 3 detection delay time (With overcurrent 3 detection function)**
   **(Test condition 5, test circuit 5)**

### 8. 1  Active "L"

The overcurrent 3 detection delay time ($t_{DIOV3}$) is the time period from when the voltage V2 exceeds $V_{DIOV3}$ to when $V_{DO}$ goes to "L", after V2 is increased to 1.6 V instantaneously (within 10 μs) under the set conditions of V1 = 3.5 V, V2 = 0 V.

### 8. 2  Active "H"

The overcurrent 3 detection delay time ($t_{DIOV3}$) is the time period from when the voltage V2 exceeds $V_{DIOV3}$ to when $V_{DO}$ goes to "H", after V2 is increased to 1.6 V instantaneously (within 10 μs) under the set conditions of V1 = 3.5 V, V2 = 0 V.

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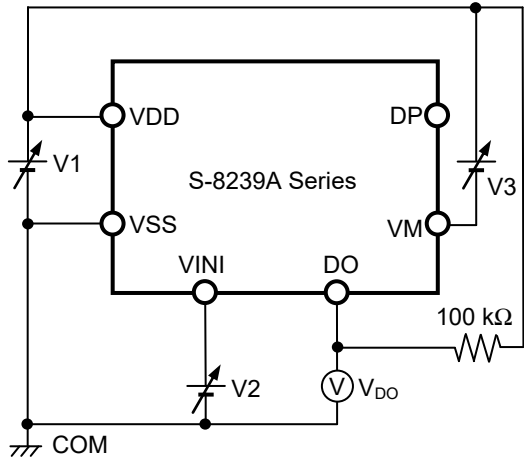
**Figure 4  Test Circuit 1**
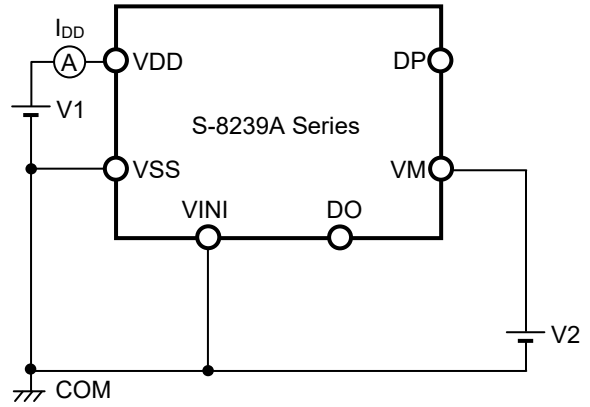


**Figure 5  Test Circuit 2**
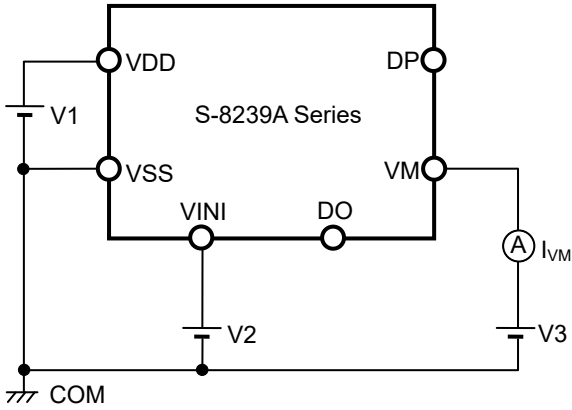


**Figure 6  Test Circuit 3**
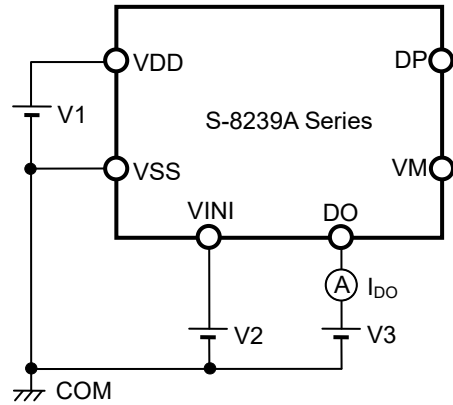


**Figure 7  Test Circuit 4**
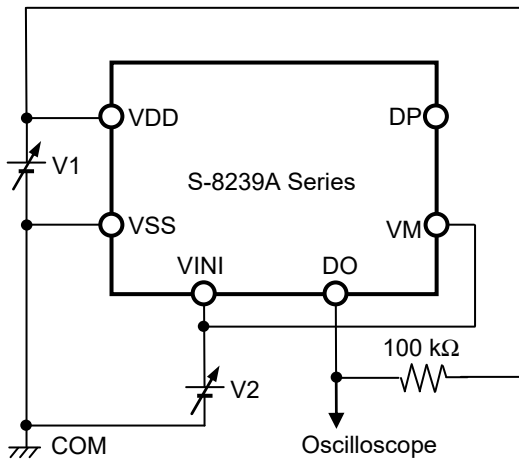


**Figure 8  Test Circuit 5**

# ■ Operation

### 1. Normal status

The S-8239A Series monitors the voltage between the VINI pin and the VSS pin to control discharging. When the VINI pin voltage is equal to or lower than the overcurrent 1 detection voltage ($V_{DIOV1}$), the DO pin becomes "High-Z" (Active "L") or $V_{SS}$ potential (Active "H"). This status is called the normal status.

**Caution** **When a battery is connected for the first time, the S-8239A Series may not be in the normal status. In this case, short the VM pin and VSS pin or connect the charger. The S-8239A Series then becomes the normal status.**

### 2. Overcurrent status (Overcurrent 1, overcurrent 2, overcurrent 3)

When a battery is in the normal status, if the VINI pin voltage is equal to or higher than the overcurrent detection voltage because the discharge current is equal to or higher than the specified value and the status continues for the overcurrent detection delay time or longer, the DO pin becomes $V_{SS}$ potential (Active "L") or "High-Z" (Active "H"). This status is called the overcurrent status. The overcurrent status is retained when the voltage between the VDD pin and the VM pin is equal to or lower than the overcurrent release voltage ($V_{RIOV}$).
In the overcurrent status, the VM pin and VSS pin are shorted by the internal resistor between the VM pin and the VSS pin ($R_{VMS}$) in the S-8239A Series. However, the VM pin is at $V_{DD}$ potential due to the external load as long as the external load is connected. When the external load is disconnected completely, the VM pin returns to $V_{SS}$ potential.
The overcurrent status is released when the voltage between the VDD pin and the VM pin is equal to or higher than $V_{RIOV}$.

### 3. UVLO status

The S-8239A Series includes a UVLO (under voltage lock out) function to prevent the IC malfunction due to the decrease of the battery voltage when detecting the overcurrent. When the battery voltage in the normal status is equal to or lower than the UVLO detection voltage ($V_{UVLO}$) and the status continues for the UVLO detection delay time ($t_{UVLO}$) or longer, the DO pin becomes $V_{SS}$ potential (Active "L") or "High-Z" (Active "H"). This status is called the UVLO status.
In the UVLO status, the VM pin and VSS pin are shorted by $R_{VMS}$ between the VM pin and the VSS pin in the S-8239A Series.
After that, the UVLO status is released if the battery voltage becomes equal to or higher than $V_{UVLO}$.

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## 4. Delay circuit

The detection delay times are determined by dividing a clock of approximately 3.5 kHz with the counter.

**Remark** The overcurrent 2 detection delay time ($t_{DIOV2}$) starts when the overcurrent 1 detection voltage ($V_{DIOV1}$) is detected. When the overcurrent 2 detection voltage ($V_{DIOV2}$) is detected over $t_{DIOV2}$ after the detection of $V_{DIOV1}$, the S-8239A Series becomes the overcurrent status within $t_{DIOV2}$ from the time of detecting $V_{DIOV2}$.
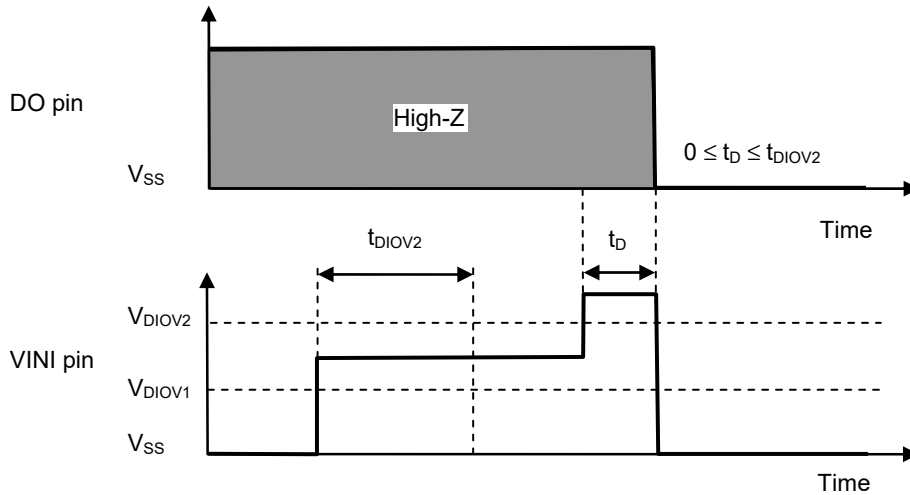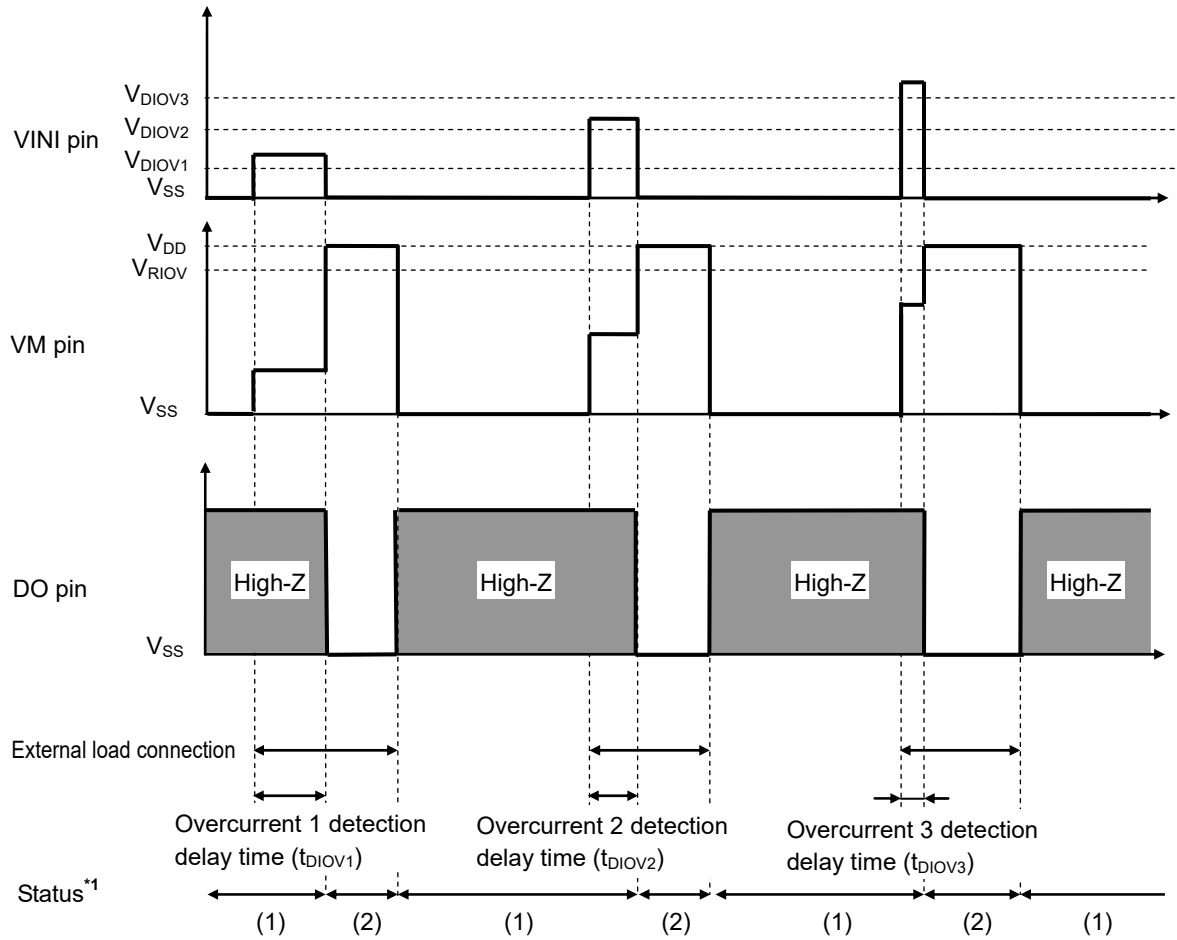


**Figure 9**

## 5. DP pin

The DP pin is a test pin for delay time measurement and it should be open in the actual application.
If a capacitor whose capacitance is 1000 pF or more or a resistor whose resistance is 1 MΩ or less is connected to this pin, error may occur in the delay times or in the detection voltages.

# ■ Timing Charts

## 1. Overcurrent detection

### 1. 1  Active "L"

#### 1. 1. 1  With overcurrent 3 detection function

VINI pin

$V_{DIOV3}$
$V_{DIOV2}$
$V_{DIOV1}$
$V_{SS}$

VM pin

$V_{DD}$
$V_{RIOV}$

$V_{SS}$

DO pin          High-Z        High-Z        High-Z        High-Z

$V_{SS}$

External load connection

Overcurrent 1 detection    Overcurrent 2 detection    Overcurrent 3 detection
delay time ($t_{DIOV1}$)        delay time ($t_{DIOV2}$)        delay time ($t_{DIOV3}$)

Status[1]      (1)      (2)      (1)      (2)      (1)      (2)      (1)

**[1].**  (1): Normal status
(2): Overcurrent status

**Figure 10**

### 1. 1. 2  Without overcurrent 3 detection function



**Figure 11**

*1. (1): Normal status
(2): Overcurrent status

### 1. 2 Active "H"

#### 1. 2. 1 With overcurrent 3 detection function



**Figure 12**

**\*1.** (1): Normal status
(2): Overcurrent status

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### 1. 2. 2  Without overcurrent 3 detection function



**Figure 13**

*1.  (1): Normal status
(2): Overcurrent status

## 2. UVLO detection

### 2. 1 Active "L"
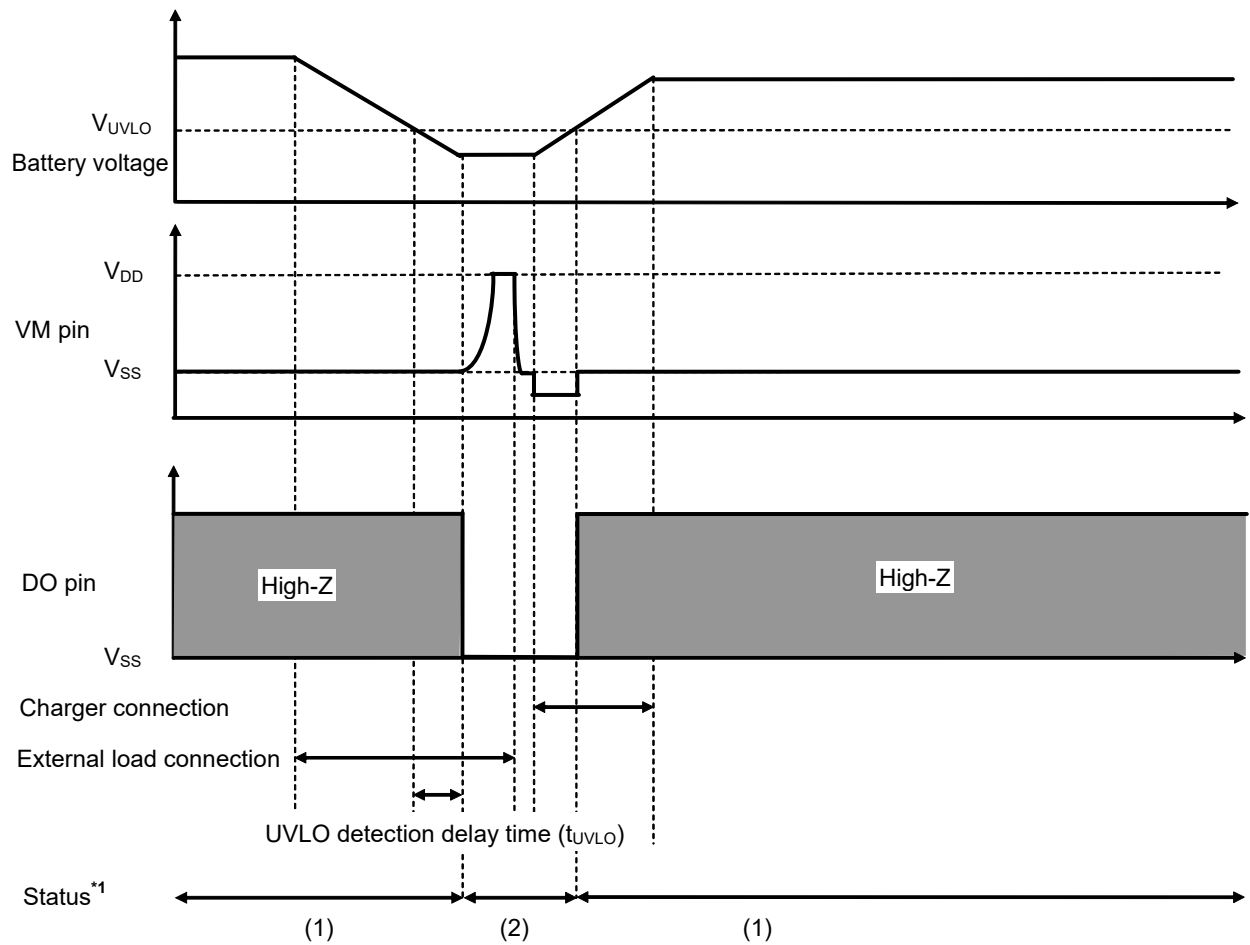


**Figure 14**

**\*1.** (1): Normal status
(2): UVLO status

**Remark**  The charger is assumed to charge with a constant current.

**2. 2 Active "H"**



$V_{UVLO}$

Battery voltage

$V_{DD}$

VM pin

$V_{SS}$

DO pin

High-Z

$V_{SS}$

Charger connection

External load connection

UVLO detection delay time ($t_{UVLO}$)

Status[*1]

(1)          (2)          (1)

**\*1.** (1): Normal status
(2): UVLO status

**Remark** The charger is assumed to charge with a constant current.

**Figure 15**

## ■ 5-serial-cell Protection Circuit Examples

**Figure 16** and **Figure 17** show the 5-serial-cell protection circuit examples used by the S-8239A Series and the S-8225A Series. Contact our sales representatives when using the circuit other than the following protection circuit examples.

### 1. Active "L"
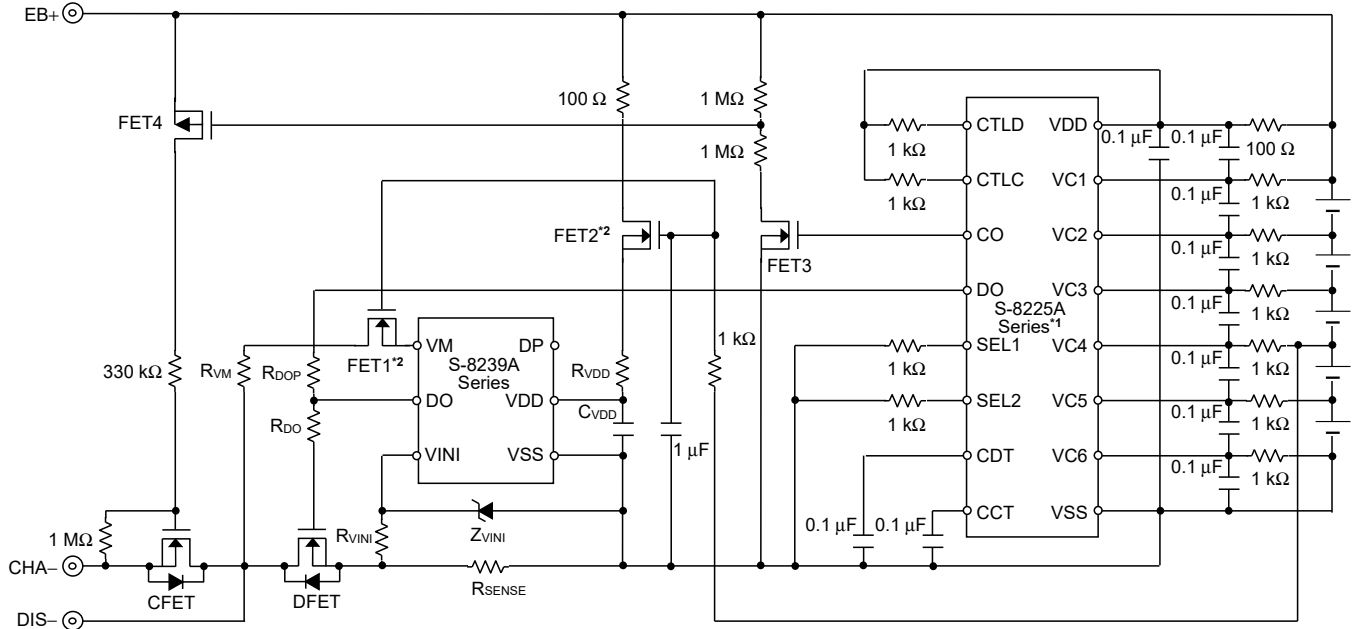


**Figure 16**

### 2. Active "H"



**Figure 17**

**ABLIC Inc.**
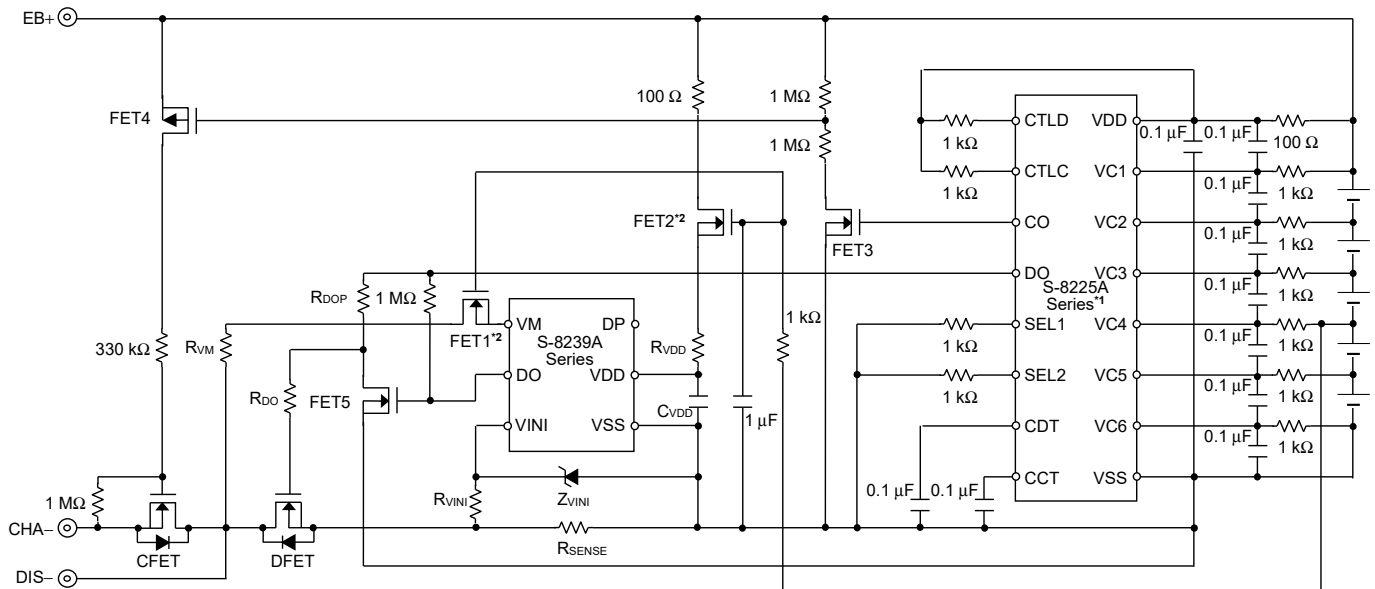
**Table 7  Constants for External Components**

| Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| $R_{VDD}$ | 300 | 470 | 1000 | Ω |
| $R_{VINI}$ | 1 | – | – | kΩ |
| $R_{SENSE}$ | 0 | – | – | mΩ |
| $R_{VM}$ | 1 | 5.1 | 51 | kΩ |
| $R_{DO}$[*3] | – | 5.1 | – | kΩ |
| $R_{DOP}$ | 330 | 510 | 2000 | kΩ |
| $C_{VDD}$ | 0.022 | 0.1 | 1 | μF |

***1.** Refer to the data sheet of the S-8225A Series for the recommended value for external components
of the S-8225A Series.
***2.** Use the products with the same model number for FET1 and FET2.
***3.** Set up the optimal constant according to the FET in use.

Caution 1.  **The constants may be changed without notice.**
2.  **It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**
3.  **The DP pin should be open.**

# ■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

# ■ Characteristics (Typical Data)

## 1. Current consumption

### 1. 1 $I_{OPE}$ vs. Ta
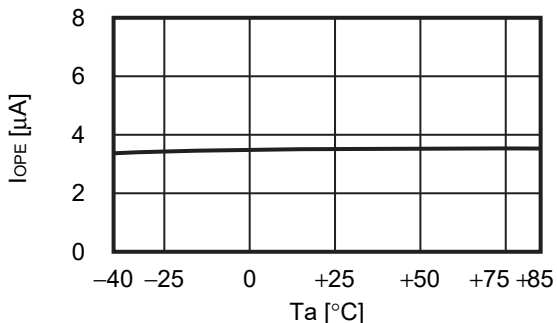


### 1. 2 $I_{OPE}$ vs. $V_{DD}$
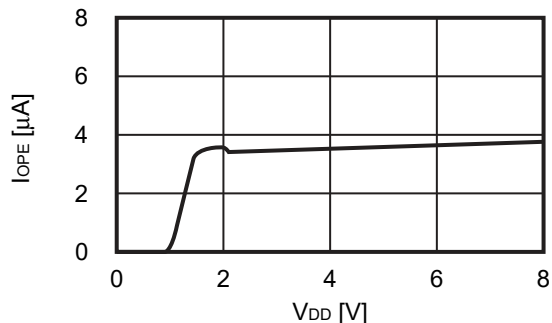


### 1. 3 $I_{UVLO}$ vs. Ta
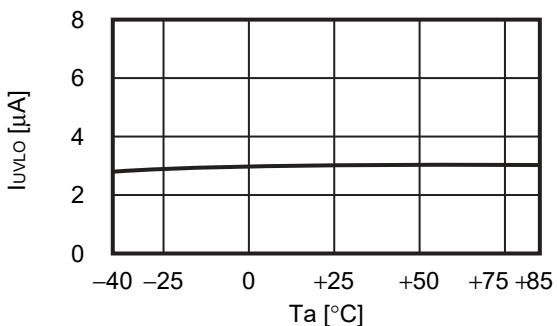


## 2. Overcurrent detection / release voltage, UVLO function and delay times

### 2. 1 $V_{DIOV1}$ vs. Ta

$V_{DIOV1}$ = 0.08 V



### 2. 2 $V_{DIOV2}$ vs. Ta

$V_{DIOV2}$ = 0.4 V
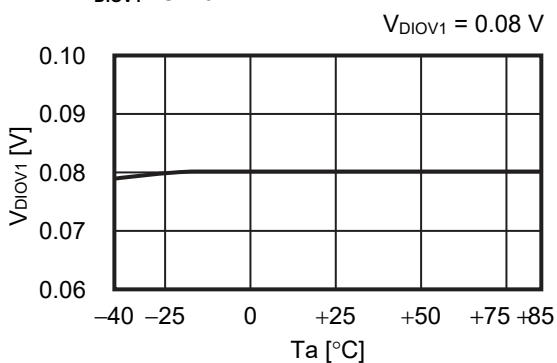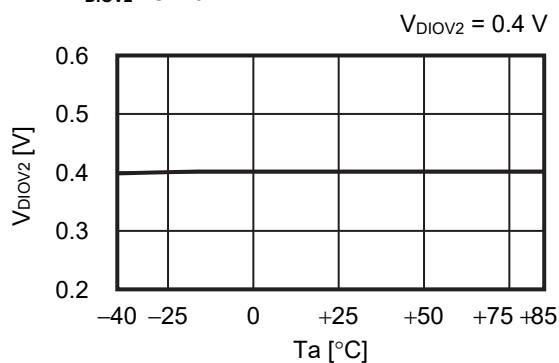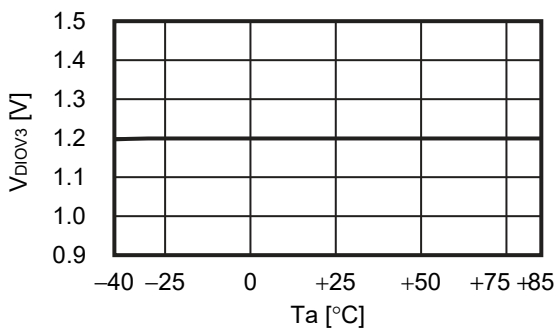


### 2. 3 $V_{DIOV3}$ vs. Ta



### 2. 4 $V_{RIOV}$ vs. Ta

**2. 5  $V_{DIOV1}$ vs. $V_{DD}$**

$V_{DIOV1}$ = 0.08 V



**2. 6  $V_{DIOV2}$ vs. $V_{DD}$**

$V_{DIOV2}$ = 0.4 V
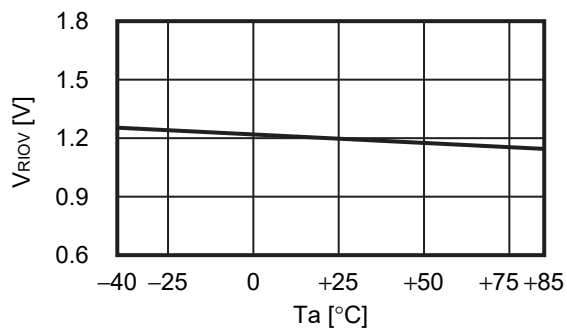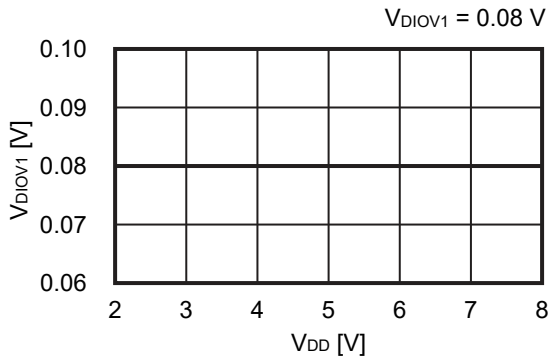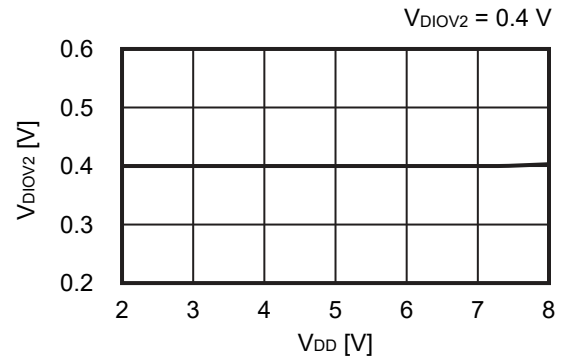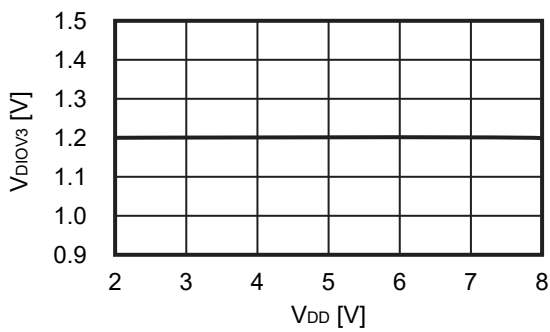


**2. 7  $V_{DIOV3}$ vs. $V_{DD}$**



**2. 8  $V_{RIOV}$ vs. $V_{DD}$**



**2. 9  $t_{DIOV1}$ vs. Ta**

$t_{DIOV1}$ = 1150 ms



**2. 10  $t_{DIOV2}$ vs. Ta**

$t_{DIOV2}$ = 1.12 ms
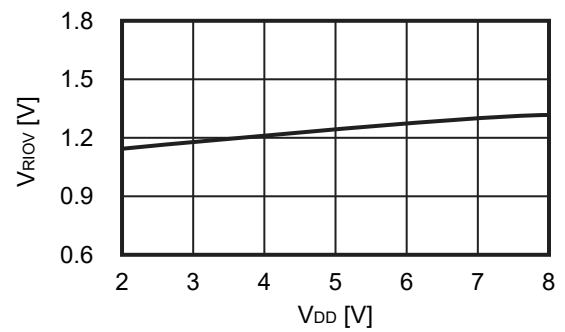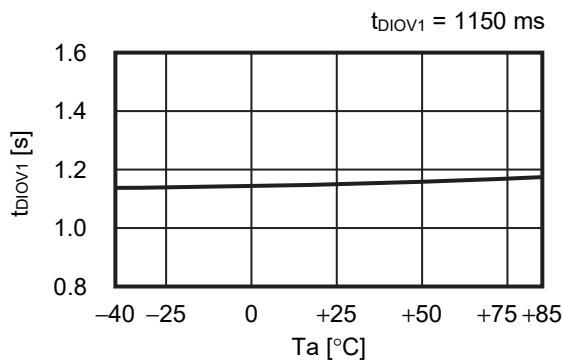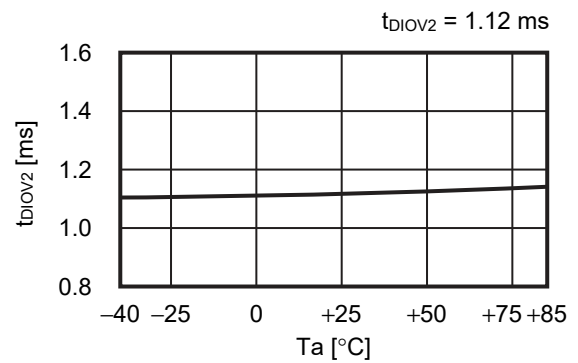


**2. 11  $t_{DIOV3}$ vs. Ta**



**2. 12  $t_{DIOV1}$ vs. $V_{DD}$**

$t_{DIOV1}$ = 1150 ms

**2. 13  $t_{DIOV2}$ vs. $V_{DD}$**

$t_{DIOV2}$ = 1.12 ms
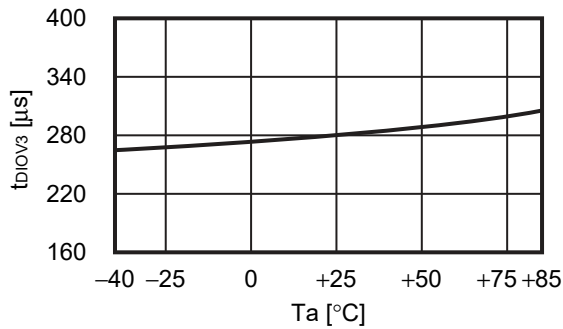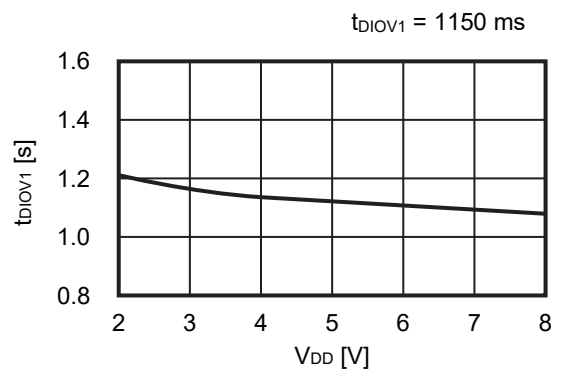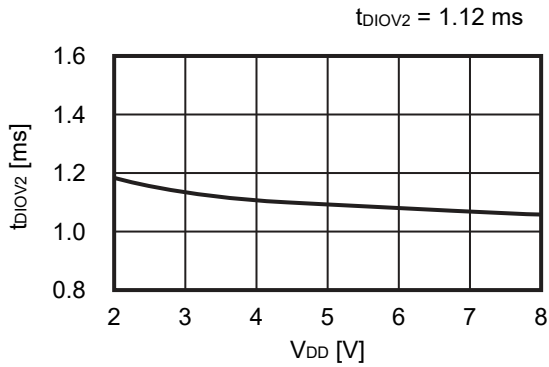
**2. 14  $t_{DIOV3}$ vs. $V_{DD}$**
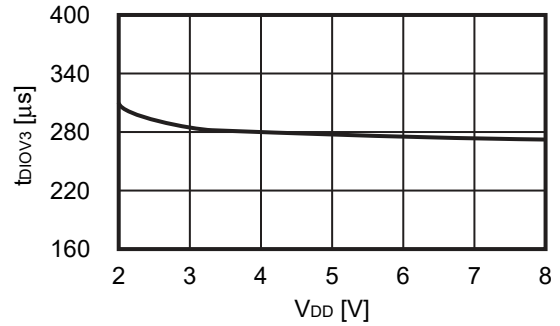
**2. 15  $V_{UVLO}$ vs. Ta**
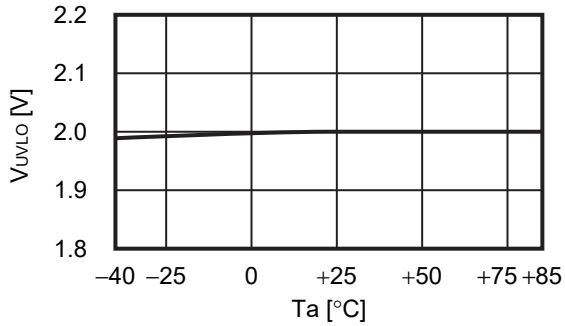
**2. 16  $t_{UVLO}$ vs. $V_{DD}$**
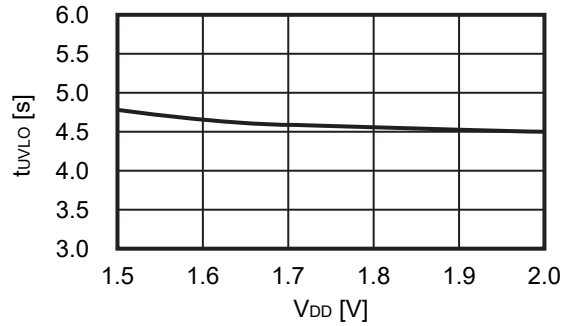
## 3.  Output Resistance

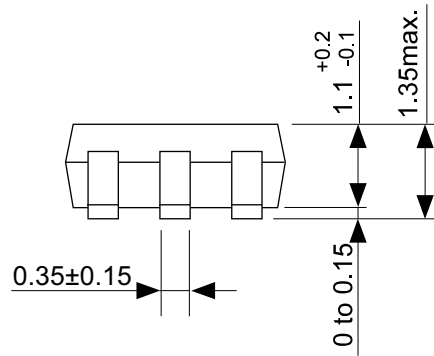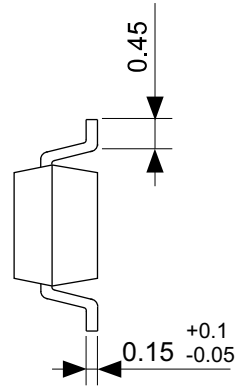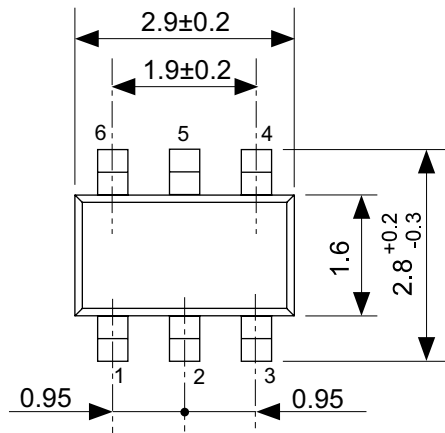**3. 1  $R_{DOL}$ vs. Ta**
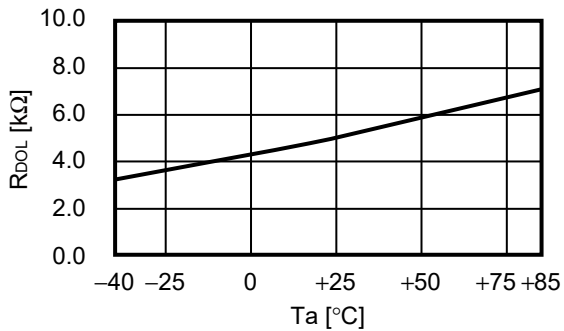
# ■ Marking Specification

### 1. SOT-23-6

Top view
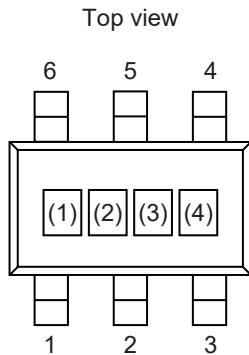


(1) to (3): Product code (Refer to **Product name vs. Product code**)
(4): Lot number

**Product name vs. Product code**

| Product Name | Product Code | | |
|---|---|---|---|
| | (1) | (2) | (3) |
| S-8239AAA-M6T1U | 3 | S | A |
| S-8239AAB-M6T1U | 3 | S | B |
| S-8239AAC-M6T1U | 3 | S | C |
| S-8239AAD-M6T1U | 3 | S | D |
| S-8239AAE-M6T1U | 3 | S | E |
| S-8239AAF-M6T1U | 3 | S | F |
| S-8239AAG-M6T1U | 3 | S | G |
| S-8239AAH-M6T1U | 3 | S | H |
| S-8239AAI-M6T1U | 3 | S | I |
| S-8239AAJ-M6T1U | 3 | S | J |
| S-8239AAK-M6T1U | 3 | S | K |
| S-8239AAL-M6T1U | 3 | S | L |
| S-8239AAM-M6T1U | 3 | S | M |
| S-8239AAN-M6T1U | 3 | S | N |
| S-8239AAO-M6T1U | 3 | S | O |
| S-8239AAP-M6T1U | 3 | S | P |

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2.9±0.2

1.9±0.2

6　5　4

1　2　3

0.95　　0.95

1.6

2.8 +0.2 -0.3

0.45

0.15 +0.1 -0.05

1.1 +0.2 -0.1

1.35max.

0.35±0.15

0 to 0.15

No. MP006-A-P-SD-2.1

| TITLE | SOT236-A-PKG Dimensions |
|---|---|
| No. | MP006-A-P-SD-2.1 |
| ANGLE | ⊕ ⊏ |
| UNIT | mm |
|  |  |

**ABLIC Inc.**

ø1.5 +0.1 -0

2.0±0.05

4.0±0.1(10 pitches:40.0±0.2)

1.75±0.1

0.25±0.1

3.5±0.05

8.0±0.2

3.25±0.15

ø1.0 +0.2 -0

4.0±0.1

1.4±0.2

3.2±0.2

3 2 1

4 5 6

Feed direction
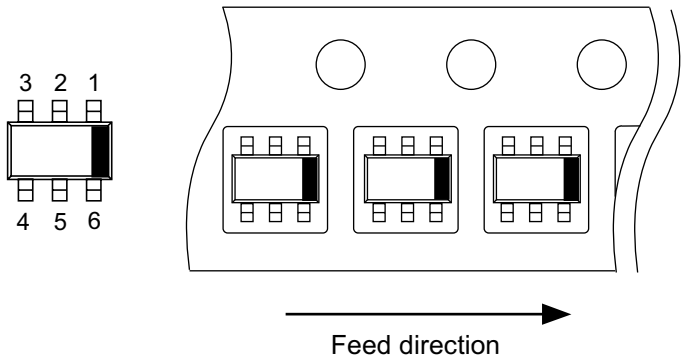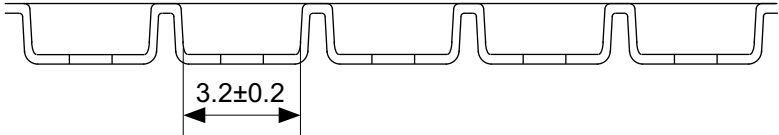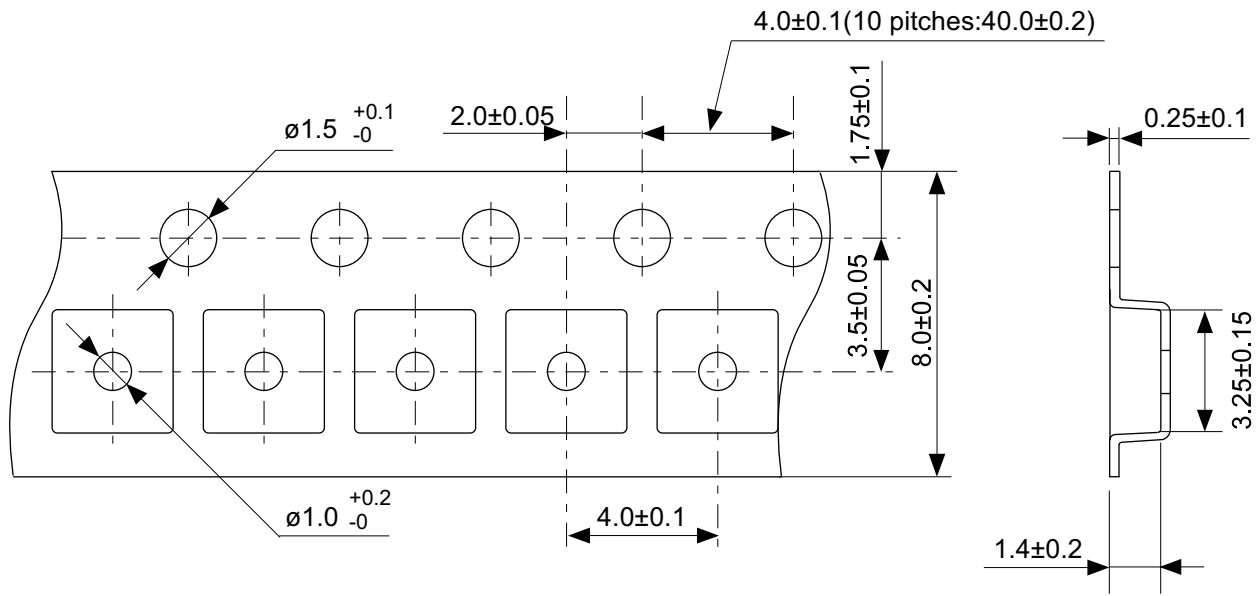
No. MP006-A-C-SD-3.1

| TITLE | SOT236-A-Carrier Tape |
|---|---|
| No. | MP006-A-C-SD-3.1 |
| ANGLE | |
| UNIT | mm |
| | |

**ABLIC Inc.**

12.5max.

$\phi 60 ^{+1}_{-0}$

$\phi 180 ^{+0}_{-3}$

9.0±0.3
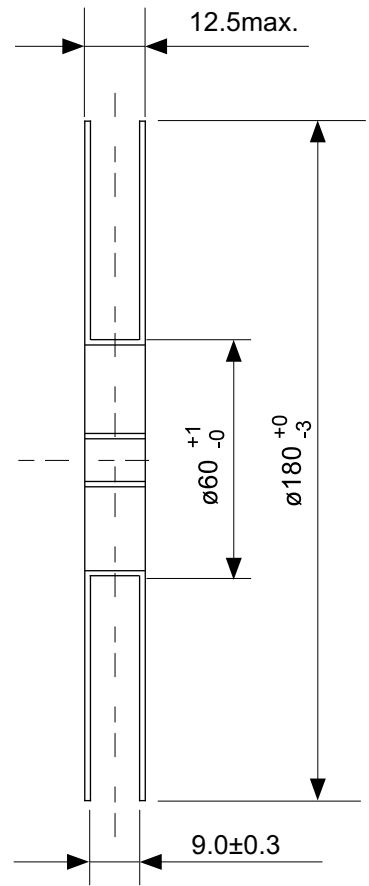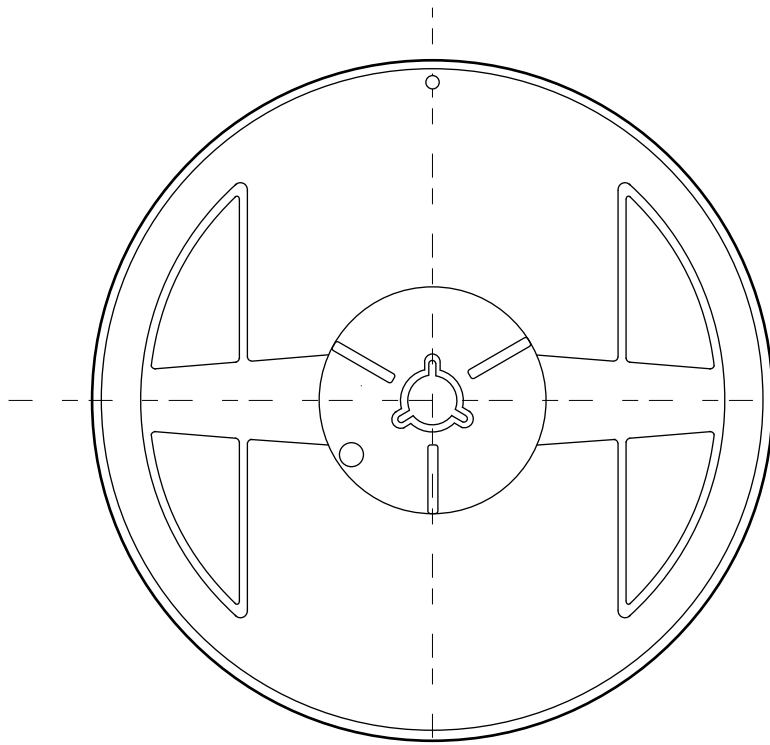
Enlarged drawing in the central part

$\phi 21±0.5$

$\phi 13±0.2$

2±0.2

(60°) (60°)
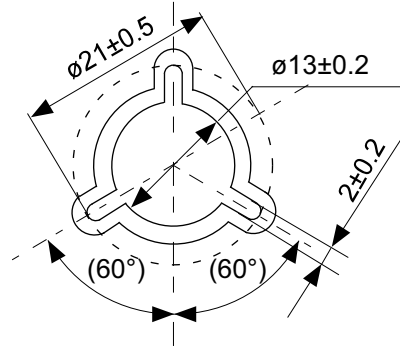
No. MP006-A-R-SD-2.1

| TITLE | SOT236-A-Reel | | |
|---|---|---|---|
| No. | MP006-A-R-SD-2.1 | | |
| ANGLE | | QTY | 3,000 |
| UNIT | mm | | |
| | | | |
| | **ABLIC Inc.** | | |

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2.4-2019.07

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