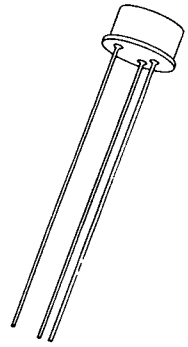
SCR

2N1595-99

The 2N1595 series of Silicon Controlled Rectifiers are planar-passivated, all-diffused, three junction, reverse blocking triode thyristors for low power switching and control applications. The 2N2322 series, which is also available, offers additional maximum specified electrical parameters.



- Painted external surface for maximum heat dissipation
- Single-ended package, ideal for printed circuit applications
- All-welded construction
- All-diffused, planar passivated
- Glass-to-metal seals

MAXIMUM ALLOWABLE RATINGS

TYPE	REPETITIVE PEAK OFF-STATE VOLTAGE, V_{DRM}(1)	PEAK POSITIVE ANODE VOLTAGE PFV	REPETITIVE PEAK REVERSE VOLTAGE, V_{RRM}
	T_C = −65°C to +125°C		
2N1595	50 Volts *	500 Volts	50 Volts *
2N1596	100 Volts *	500 Volts	100 Volts *
2N1597	200 Volts *	500 Volts	200 Volts *
2N1598	300 Volts *	500 Volts	300 Volts *
2N1599	400 Volts *	500 Volts	400 Volts *

(1) Applies for 1000 ohms maximum, connected gate-to-cathode.

RMS On-State Current, $I_{T(RMS)}$ ..... 1.6 Amperes (all conduction angles)
Average On-State Current, $I_{T(AV)}$ ..... Depends on conduction angle (see Charts 3, 4, 5 and 6)
Peak One-Cycle Surge (Non-rep) On-State Current, I_{TSM} ..... 15 Amperes*
Peak Gate Power Dissipation, P_{GM} ..... 0.1 Watts
Average Gate Power Dissipation, $P_{G(AV)}$ ..... 0.01 Watts
Peak Positive Gate Current, I_{GM} ..... 0.1 Amperes
Peak Positive Gate Voltage, V_{GM} ..... 6 Volts
Peak Negative Gate Voltage, V_{GM} ..... −6 Volts
Storage Temperature, T_{STG} ..... −65°C to +150°C*
Operating Temperature, T_J ..... −65°C to +150°C

* Indicates data included in JEDEC type number registration.

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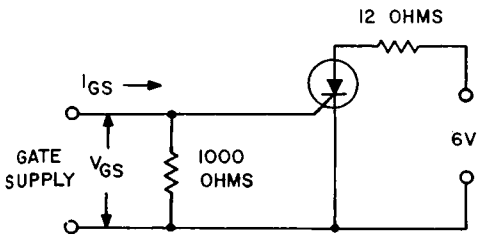
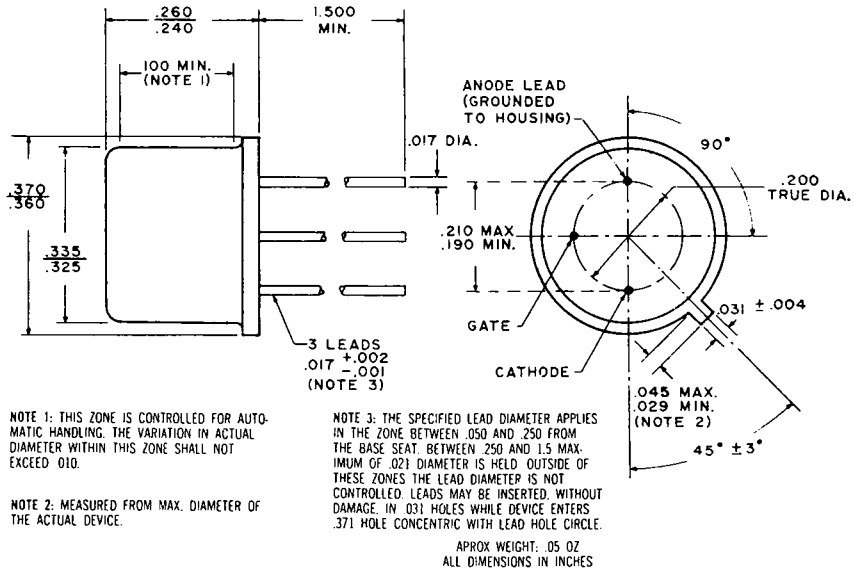
OUTLINE DRAWING
(Conforms to JEDEC TO-5 Package Outline)

2N1595-99





NOTE 1: THIS ZONE IS CONTROLLED FOR AUTOMATIC HANDLING. THE VARIATION IN ACTUAL DIAMETER WITHIN THIS ZONE SHALL NOT EXCEED 010.

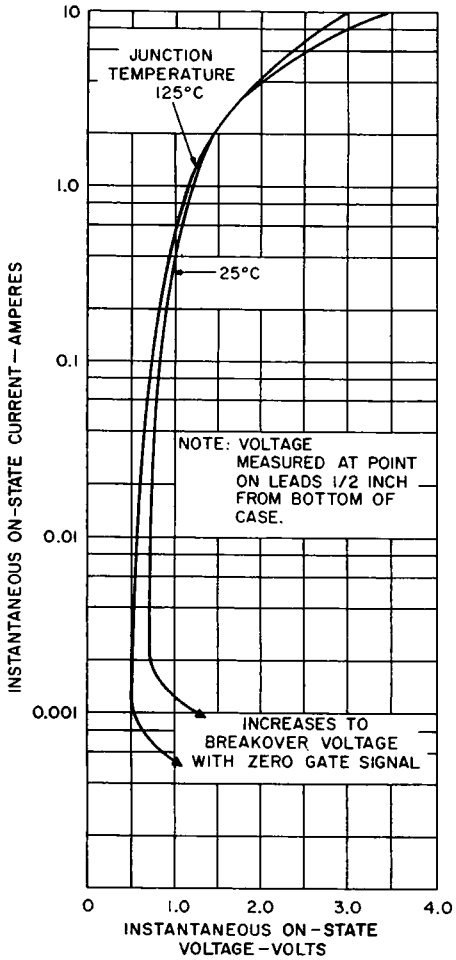
NOTE 2: MEASURED FROM MAX. DIAMETER OF THE ACTUAL DEVICE.

NOTE 3: THE SPECIFIED LEAD DIAMETER APPLIES IN THE ZONE BETWEEN .050 AND .250 FROM THE BASE SEAT. BETWEEN .250 AND 1.5 MAXIMUM OF .021 DIAMETER IS HELD OUTSIDE OF THESE ZONES THE LEAD DIAMETER IS NOT CONTROLLED. LEADS MAY BE INSERTED, WITHOUT DAMAGE, IN .031 HOLES WHILE DEVICE ENTERS .371 HOLE CONCENTRIC WITH LEAD HOLE CIRCLE.

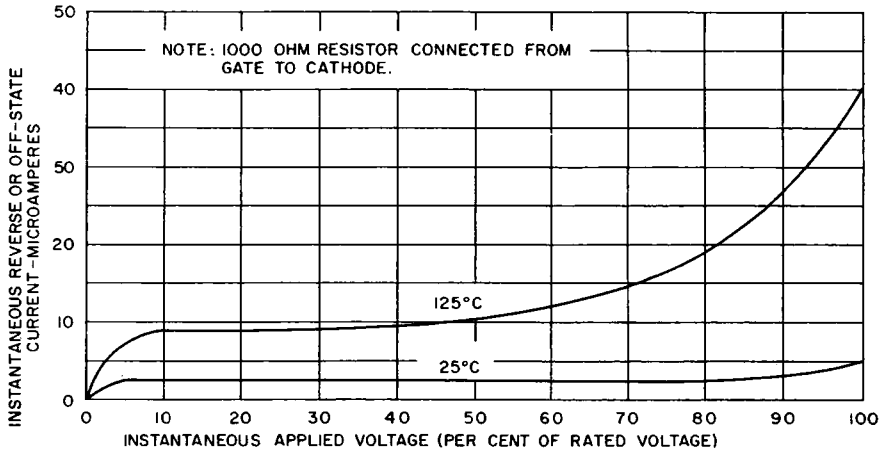
APROX WEIGHT: .05 OZ
ALL DIMENSIONS IN INCHES

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Off-State and Reverse Current	I_{DRM} & I_{RRM}	— —	2.0 100	10 1000*	μA	$V_{DRM} = V_{RRM}$ = Rated volts peak, R_{GK} = 1000 ohms. $T_C = +25°C$ $T_C = +125°C$
D.C. Gate Trigger Current	I_{GS} (1)	—	0.9	10*	mAdc	$T_C = +25°C$, $V_D = 6$ Vdc, $R_L = 12$ ohms
D.C. Gate Trigger Voltage	V_{GT}	—	0.6	3.0*	Vdc	$T_C = +25°C$, $V_D = 6$ Vdc, $R_L = 12$ ohms
Peak On-State Voltage	V_{TM}	—	1.25	2.0*	Volts	$T_C = +25°C$, $I_{TM} = 1.0$ A peak, 1 msec. wide pulse. Duty cycle $\leqq 2\%$.
Holding Current	I_H	—	1.0	—	mAdc	$T_C = +25°C$, Anode Source Voltage = 12 Vdc, $R_{GK} = 1000$ ohms.
Circuit Commutated Turn-Off Time	t_q	—	40	—	μsec	$T_C = +125°C$, $I_{TM} = 1.0$ A peak. Rectangular current pulse, 50 μsec duration. Rate of rise of current < 10A/μsec. Commutation rate $\leqq 5$ A/μsec. Peak reverse voltage = Rated V_{RRM} volts max. Reverse voltage at end of turn-off time interval 15 volts. Repetition rate = 60 pps. Rate of rise of re-applied off-state voltage (dv/dt) = 20 V/μsec. Off-state voltage = Rated V_{DRM} volts. Gate bias during turn-off time interval = 0 volts, 100 ohms.
Turn-On Time	$t_d + t_r$	—	1.2	—	μsec	$T_C = +25°C$, V_D = Rated V_{DRM} value. $I_{TM} = 1.0$ A. Gate trigger pulse = 6 volts, 300 ohms, 5 μsec wide, 0.1 μsec rise time. Gate bias = 0 volts, 300 ohms.

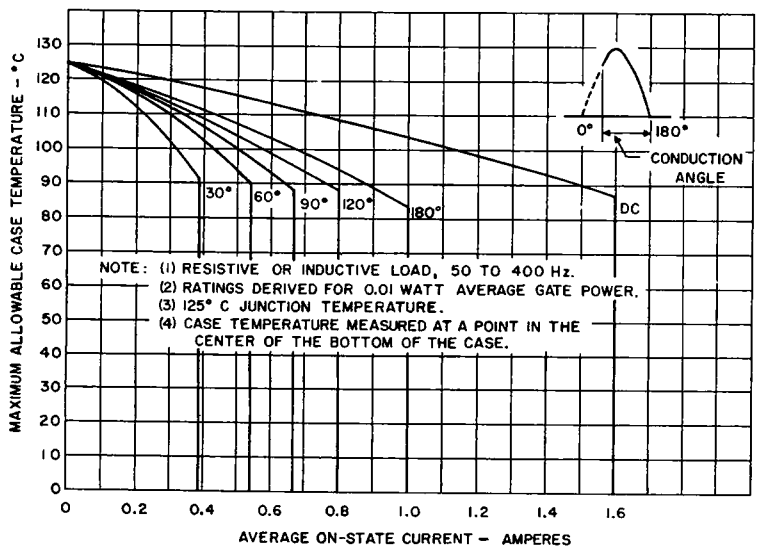
* Indicates data included in JEDEC type number registration.
NOTE: (1) I_{GS} is defined in the circuit below:



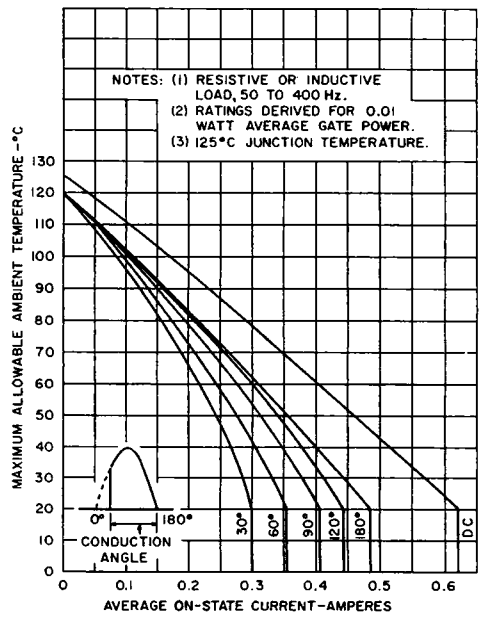
1. TYPICAL ON-STATE CHARACTERISTICS



2. TYPICAL OFF-STATE AND REVERSE BLOCKING CHARACTERISTICS

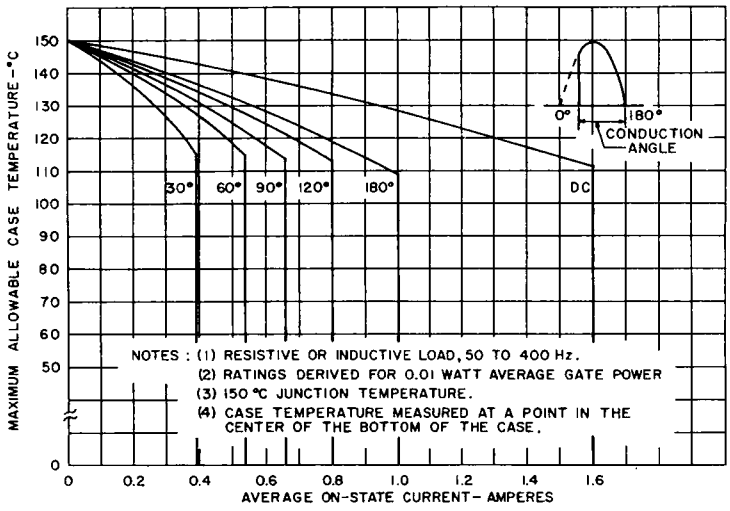


3. MAXIMUM ALLOWABLE CASE TEMPERATURE (150°C Junction Temp.)

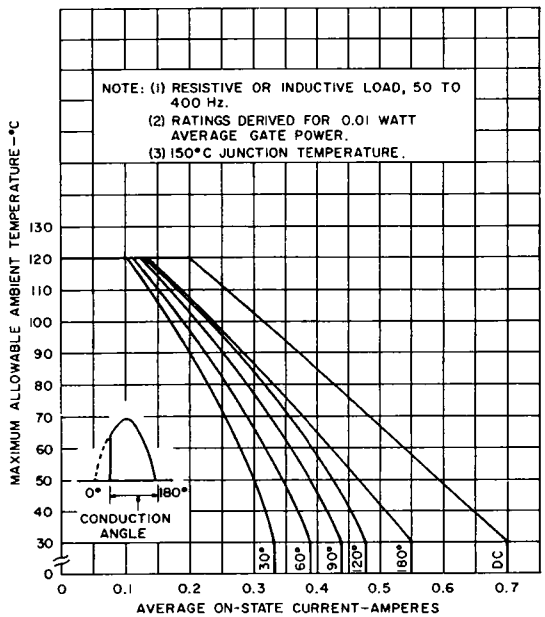


4. MAXIMUM ALLOWABLE AMBIENT TEMPERATURE (125°C Junction Temp.)

Charts 5 and 6 apply to latching applications where SCR need not block off-state voltage after being turned on, since the V_{DRM} specification does not apply above + 125°C junction temperature. SCR will again block rated off-state voltage after junction temperature drops below + 125°C.



5. MAXIMUM ALLOWABLE CASE TEMPERATURE (125°C Junction Temp.)



6. MAXIMUM ALLOWABLE AMBIENT TEMPERATURE (150°C Junction Temp.)