



P-channel 20 V, 0.0195 Ω typ., 8 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet - production data

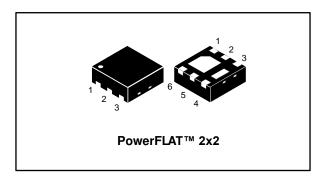
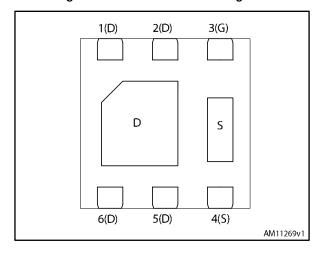


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL8P2UH7	20 V	0.0225 Ω @ 4.5 V	8 A

- Extremely low on-resistance R DS(on)
- Ultra logic level

Applications

• Switching applications

Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL8P2UH7	8L2U	PowerFLAT™ 2x2	Tape and reel



Contents STL8P2UH7

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STL8P2UH7 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	20	V
V _{GS}	Gate-source voltage	± 8	V
I _D	Drain current (continuous) at T _{pcb} = 25 °C	8	Α
I _D	Drain current (continuous) at T _{pcb} = 100 °C	5.3	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	32	Α
P _{TOT}	Total dissipation at T _{pcb} = 25 °C	2.4	W
T _{stg}	Storage temperature	- 55 to 150	°C
T _j	Max. operating junction temperature	150	°C

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max	52	°C/W

Notes:

⁽¹⁾When mounted on 1inch² FR-4 board, 2 oz Cu



⁽¹⁾Pulse width limited by safe operating area

Electrical characteristics STL8P2UH7

2 Electrical characteristics

(T _C= 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 250 μA	20			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 20 V			1	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 5 \text{ V}$			± 5	μΑ
V _{GS(th)}	Gate threshold voltage	$V_{DS}=V_{GS}, I_{D}=250 \mu A$	0.4		1	V
	Static drain-source	V _{GS} = 4.5 V, I _D = 4 A		0.0195	0.0225	Ω
R _{DS(on)}	on- resistance	V _{GS} = 2.5 V, I _D = 4 A		0.02	0.025	Ω
(on) פטיי		V _{GS} = 1.8 V, I _D = 4 A		0.036	0.043	Ω
		V _{GS} = 1.5 V, I _D = 4 A		0.05	0.085	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance	$V_{GS} = 0, V_{DS} = 16 V,$	-	2390	-	pF
C _{oss}	Output capacitance	f = 1 MHz	-	220	-	рF
C _{rss}	Reverse transfer capacitance		-	188	-	pF
Qg	Total gate charge	V _{DD} = 16 V, I _D = 8 A,	-	22	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 4.5 V	-	4.2	-	nC
Q _{gd}	Gate-drain charge		-	3.6	-	nC



Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Uni t
t _{d(on)}	Turn-on delay time	V _{DD} = 16 V, I _D = 8 A,	-	12.5	-	ns
t _r	Rise time	R_G = 1 Ω , V_{GS} = 4.5 V	-	30.5	-	ns
t _{d(off)}	Turn-off delay time		-	128	-	ns
t _f	Fall time		-	84.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		1		8	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		32	Α
$V_{SD}^{(2)}$	Forward on voltage	V _{GS} = 0, I _{SD} = 1 A	-		1	V
t _{rr}	Reverse recovery time	V _{DD} = 16 V	-	15.8		ns
Q _{rr}	Reverse recovery charge	di/dt = 100 A/μs, I _{SD} = 1 A	-	5.9		nC
I _{RRM}	Reverse recovery current	יים – ייזי	-	0.7		Α

Notes:

 $^{^{(2)}}$ Pulsed: pulse duration = 300 μ s, duty cycle 1.5%



⁽¹⁾Pulse width limited by safe operating area.

2.1 Electrical characteristics (curves)

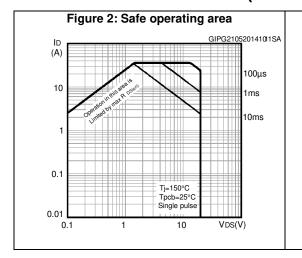


Figure 3: Thermal impedance

K $\delta = 0.5$ 0.2 0.1 0.05 0.02 0.01 0.02 0.01 0.05 0.02 0.01 0.02 0.01 0.02 0.02 0.01 0.02 0.02 0.02 0.02 0.02 0.03 0.04 0.05 0.0

Figure 4: Output characteristics

GIPG210520141044\$A

ID(A)

VGS=2.5, 3, 3.5, 4, 4.5, 5V

20

15

10

0

2 4 6 8 VDS(V)

Figure 5: Transfer characteristics

GIPG210520141055SA

12.00

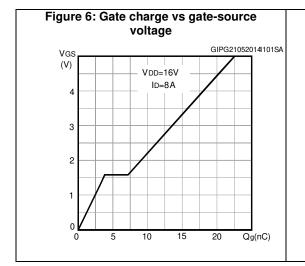
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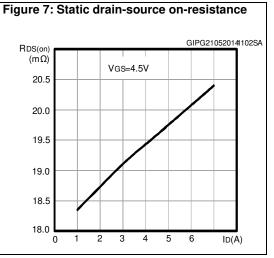
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0.05

1 1.5

2 VGS(V)





STL8P2UH7 Electrical characteristics

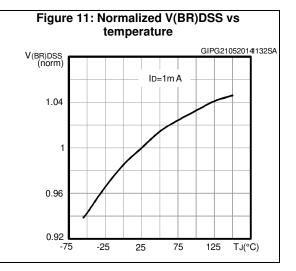
Figure 8: Capacitance variations

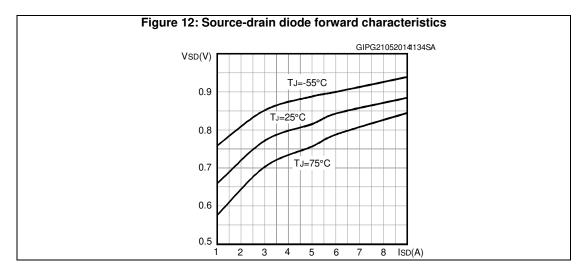
C
GIPG21052014I108SA

(pF)
Ciss
Ciss
Coss
Crss
Crss
Crss

Figure 9: Normalized gate threshold voltage vs temperature GIPG210520141114SA VGS(th) (norm) ID=250μ A 1.4 1.2 0.8 0.6 0.4 0.2 -25 25 75 125 TJ(°C)

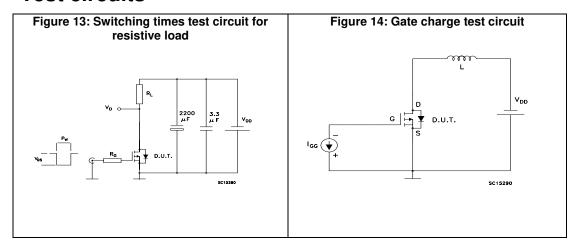
Figure 10: Normalized on-resistance vs temperature RDS(on) (norm) ID=4A 1.6 VGS=4.5V 1.4 1.2 1.0 0.8 0.6 0.4 0.2 0.0 -25 75 -75 25 125 TJ(°C)

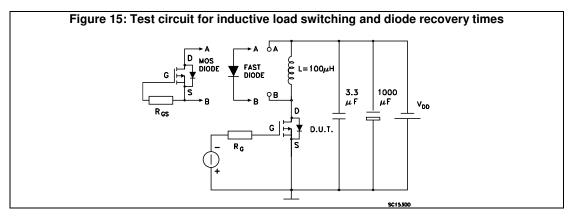




Test circuits STL8P2UH7

3 Test circuits





4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 2x2 package mechanical data

PIN#1 ID BOTTOM VIEW C 0.25 D2 E2 b (x6) **→** 0.10 M (A3) SIDE VIEW A 0.08 LASER MARK PIN#1 ID TOP VIEW 8368575_REV_C

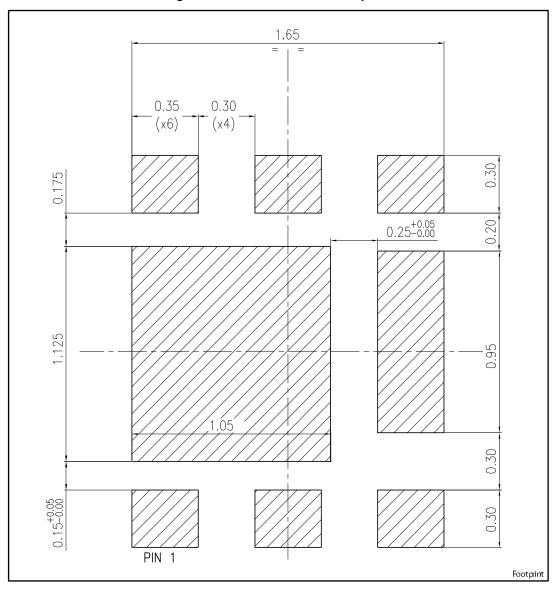
Figure 16: Drawing dimension PowerFLAT™ 2 x 2

577

Table 8: PowerFLAT™ 2 x 2 mechanical data

Dim.	mm.		
	Min.	Тур.	Max.
Α	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
Е	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
е	0.55	0.65	0.75
К	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 17: PowerFLAT™ 2 x 2 footprint



STL8P2UH7 Revision history

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
20-Aug-2013	1	First release.
04-Jun-2014	2	Document status promoted from preliminary data to production data Modified: title Modified: R _{DS(on)} max value in cover page Modified: R _{DS(on)} (typical and maximum) values in <i>Table 4: "On /off states"</i> Modified: the entire typical values in <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> and <i>Table 7: "Source drain diode"</i> Added <i>Section 8.1: "Electrical characteristics (curves)"</i> Minor text changes

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