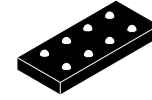


Auto Focus (AF) Controller

LC898219XI



WLCSP8, 0.97x2.25x0.265
CASE 567TE

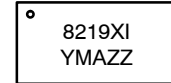
Overview

This LSI is Closed-Auto Focus control LSI equipped with hall sensor. It consists of 1 system feedback circuit and constant current driver. It has also a built-in EEPROM and temperature sensor.

Features

- Built-in Equalizer Circuit Using Digital Operation
 - ◆ AF Control Equalizer Circuit
 - ◆ Any Coefficient can be Specified by 2-wire Serial I/F (TWIF)
- 2-wire Serial Interface
(The Communication Protocol is Compatible with I²C)
- Built-in A/D Converter
- Built-in D/A Converter
 - ◆ Hall Offset
 - ◆ Constant Current Bias
- Built-in Hall Sensor
 - ◆ Si Hall Sensor
- Built-in VGA
 - ◆ Hall Amp
- Built-in EEPROM
 - ◆ 128 Byte (16 Byte/Page)
- Built-in OSC
- Built-in Constant Current Driver
 - ◆ 140 mA
- Package
 - ◆ WLCSP 8-pin
- Supply Voltage
 - ◆ V_{DD} (2.6 V to 3.3 V)
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

MARKING DIAGRAM



8219XI = Specific Device Code
Y = Year
M = Month
A = Assembly Site
ZZ = Lot Number

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|---------|-----------------------|
| LC898219XI-MH | WLCSP8 | 4000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

LC898219XI

PIN DESCRIPTION

Table 1. PIN DESCRIPTION

| Pin Name | Description |
|----------|-------------------|
| I | Input |
| P | Power Supply, GND |
| NC | Not Connect |
| O | Output |
| B | Bidirection |

- 2-wire serial interface
 - SCL I 2-wire serial interface clock pin
 - SDA B 2-wire serial interface data pin
- Driver interface
 - OUT1 O Driver output (to Actuator)
 - OUT2 O Driver output (to Actuator)
- Power supply pin
 - VDD P Power Supply
 - VSS P GND
- Port pin
 - PORT B Convergence detection monitor output
VSYNC input
Test pin
- Test pin
 - TEST O Test pin

**Process when pins are not used*

PIN TYPE “O” – Ensure that it is set to OPEN.

PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the V_{DD} or V_{SS} even when it is unused. (Please contact **onsemi** for more information about selection of V_{DD} or V_{SS} .)

PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us.

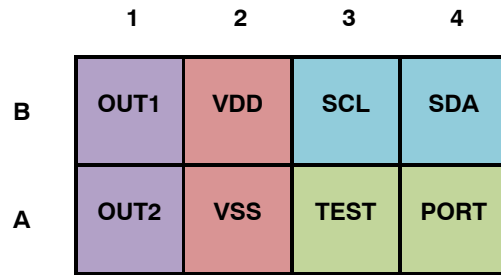
Note that incorrect processing of unused pins may result in defects.

**In case of connecting PORT pin with HOST CPU*

When LC898219XI is power off and HOST CPU is power on, a HOST CPU pin connected with PORT pin have to be fixed “L” level.

LC898219XI

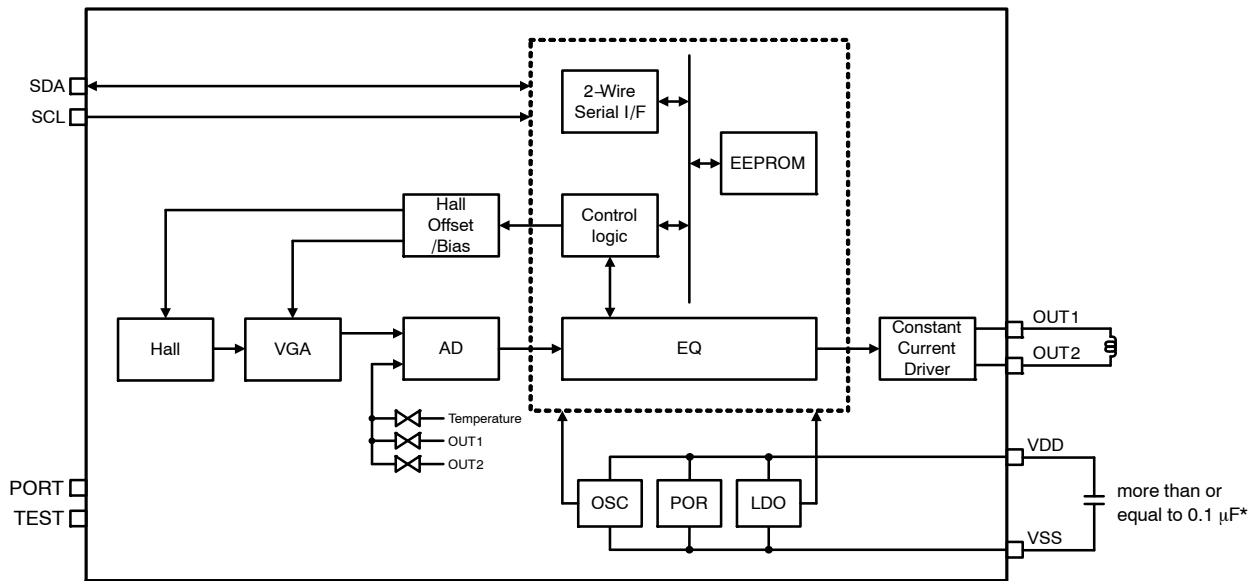
PIN LAYOUT



BOTTOM VIEW

Figure 1. Pin Layout

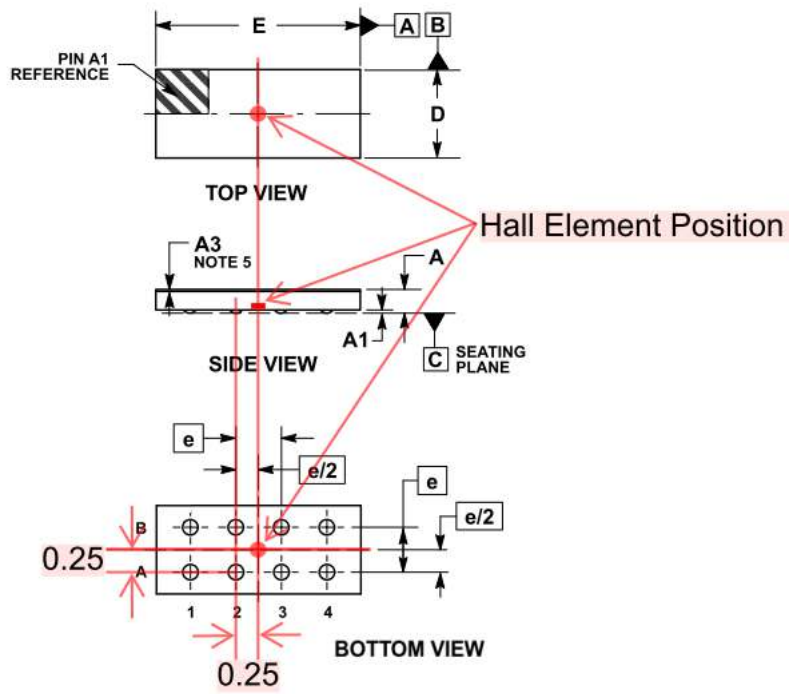
BLOCK DIAGRAM



*Consider capacitance of capacitor between V_{DD} and V_{SS} . According to power source environment, attach an additional capacitor in camera module.

Figure 2. Block Diagram

HALL ELEMENT POSITION



unit: mm(typ)

Please refer to package diagram for each dimension.

Figure 3. Hall Element Position

LC898219XI

ELECTRICAL CHARACTERISTICS

Table 2. ABSOLUTE MAXIMUM RATINGS ($V_{SS} = 0\text{ V}$)

| Symbol | Item | Condition | Rating | Unit |
|-----------------------|-------------------------------|-----------------------------|--------------------------|------------------|
| $V_{DD33\text{ max}}$ | Supply voltage | $T_a \leq 25^\circ\text{C}$ | -0.3 to 4.6 | V |
| V_{I33}, V_{O33} | Input/output voltage | $T_a \leq 25^\circ\text{C}$ | -0.3 to $V_{DD33} + 0.3$ | V |
| Tstg | Storage ambient temperature | | -55 to 125 | $^\circ\text{C}$ |
| Topr | Operating ambient temperature | | -30 to 70 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. ACCEPTABLE OPERATING RANGES ($T_a = -30$ to 70°C , $V_{SS} = 0\text{ V}$, 3 V power supply (V_{DD}))

| Symbol | Item | Min | Typ | Max | Unit |
|------------|---------------------|-----|-----|------------|------|
| V_{DD33} | Supply voltage | 2.6 | 2.8 | 3.3 | V |
| V_{IN} | Input voltage range | 0 | | V_{DD33} | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. DC CHARACTERISTICS (Input / output level at $V_{SS} = 0\text{ V}$, $V_{DD} = 2.6$ to 3.3 V , $T_a = -30$ to 70°C)

| Symbol | Item | Condition | Min | Typ | Max | Unit | Applicable Pins |
|----------|---------------------------|-------------------------|--------------|-----|-----|------------------|-----------------|
| V_{IH} | High-level input voltage | CMOS compliant Schmitt | 1.4 | | | V | SCL, SDA, PORT |
| V_{IL} | Low-level input voltage | | | | 0.4 | V | |
| V_{OH} | High-level output voltage | $I_{OH} = -2\text{ mA}$ | $V_{DD}-0.4$ | | | V | PORT |
| V_{OL} | Low-level output voltage | $I_{OL} = 2\text{ mA}$ | | | 0.2 | V | SDA, PORT |
| Rdn | Pulldown resistor | | 50 | | 220 | $\text{k}\Omega$ | PORT |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. DRIVER OUTPUT (OUT1, OUT2) ($V_{SS} = 0\text{ V}$, $V_{DD} = 2.8\text{ V}$, $T_a = 25^\circ\text{C}$)

| Symbol | Item | Condition | Min | Typ | Max | Unit | Applicable Pins |
|-------------------|-----------------|-----------|-----|-----|-----|------|-----------------|
| I _{full} | Maximum current | | 133 | 140 | 147 | mA | OUT1, OUT2 |

Table 6. NON-VOLATILE MEMORY CHARACTERISTICS

| Symbol | Item | Condition | Min | Typ | Max | Unit | Applicable Circuit |
|-----------------|----------------|-----------|-----|-----|------|--------|--------------------|
| EN | Endurance | | | | 1000 | Cycles | EEPROM |
| RT | Data retention | | 10 | | | Years | |
| t _{WT} | Write time | | | | 20 | ms | |

AC CHARACTERISTICS

V_{DD} Supply Timing

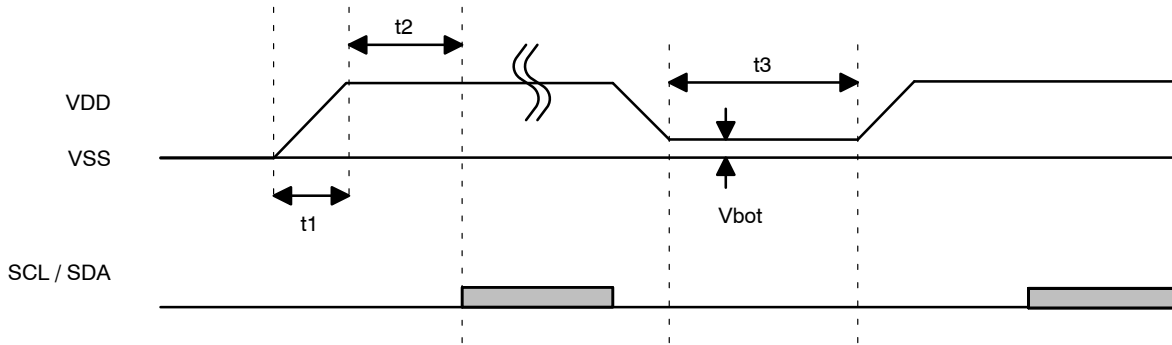


Figure 4. V_{DD} Supply Timing

It is available to use 2-wire serial interface 5 ms later for Power On Reset of V_{DD}.

Table 7. V_{DD} SUPPLY TIMING

| Symbol | Item | Min | Typ | Max | Unit |
|------------------|--|-----|-----|-----|------|
| t ₁ | V _{DD} turn on time | | | 3 | ms |
| t ₂ | 2-wire serial interface start time from V _{DD} on | 5 | | | ms |
| t ₃ | V _{DD} off time | 100 | | | ms |
| V _{bot} | Bottom Voltage | | | 0.1 | V |

AC Specification

Figure 5 shows interface timing definition and Table 8 shows electric characteristics.

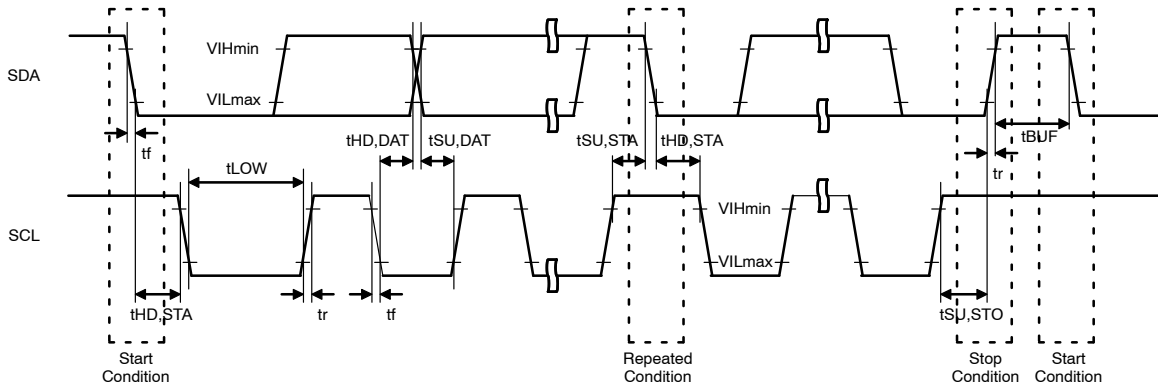


Figure 5. 2-wire Serial Interface Timing Definition

Table 8. ELECTRICAL CHARACTERISTICS FOR 2-WIRE SERIAL INTERFACE (AC CHARACTERISTICS)

| Symbol | Item | Pin Name | Fast-mode | | | Fast-mode Plus | | | Unit |
|---------|---|------------|---------------|-----|-----|----------------|-----|------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| FSCL | SCL clock frequency | SCL | | | 400 | | | 1000 | kHz |
| tHD,STA | START condition hold time | SCL SDA | 0.6 | | | 0.26 | | | μs |
| tLOW | SCL clock Low period | SCL | 1.3 | | | 0.5 | | | μs |
| tHIGH | SCL clock High period | SCL | 0.6 | | | 0.26 | | | μs |
| tSU,STA | Setup time for repetition START condition | SCL SDA | 0.6 | | | 0.26 | | | μs |
| tHD,DAT | Data hold time | SCL SDA | 0 (Note 1) | | 0.9 | 0 (Note 1) | | | μs |
| tSU,DAT | Data setup time | SCL SDA | 100 | | | 50 | | | ns |
| tr | SDA, SCL rising time | SCL SDA | | | 300 | | | 120 | ns |
| tf | SDA, SCL falling time | SCL SDA | | | 300 | | | 120 | ns |
| tSU,STO | STOP condition setup time | SCL SDA | 0.6 | | | 0.26 | | | μs |
| tBUF | Bus free time between STOP and START | SCL SDA | 1.3 | | | 0.5 | | | μs |

1. LC898219XI is designed for a condition with typ. 20 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

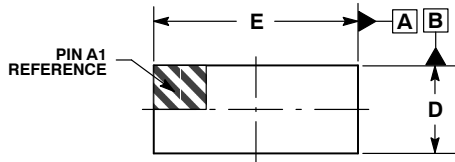
ON Semiconductor®



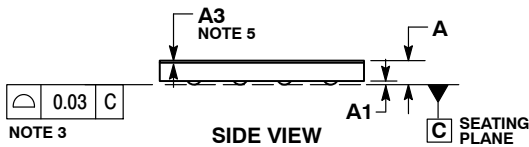
SCALE 4:1

WLCSP8, 0.97x2.25X0.265
CASE 567TE
ISSUE A

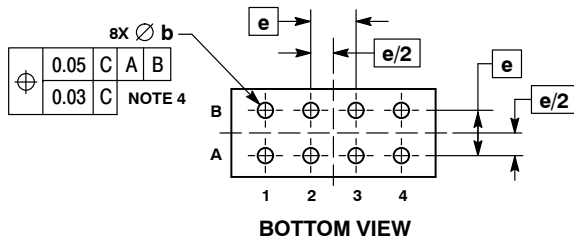
DATE 10 MAR 2017



TOP VIEW

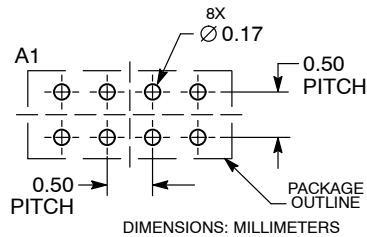


SIDE VIEW



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

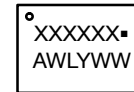
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER PARALLEL TO DATUM C.
5. DIMENSION A3 IS AN OPTIONAL BACKSIDE COATING LAYER.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|------|
| | MIN | NOM | MAX |
| A | 0.24 | 0.265 | 0.29 |
| A1 | 0.04 REF | | |
| A3 | 0.025 REF | | |
| b | 0.12 | 0.17 | 0.22 |
| D | 0.92 | 0.97 | 1.02 |
| E | 2.20 | 2.25 | 2.30 |
| e | 0.50 BSC | | |

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|------------------|-------------------------|--|
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| DESCRIPTION: | WLCSP8, 0.97X2.25X0.265 | PAGE 1 OF 1 |

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