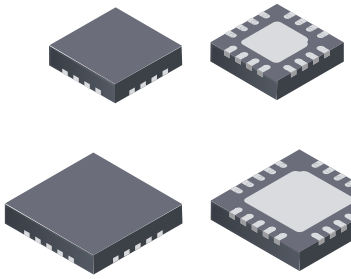
Dual DMOS Full-Bridge Motor Driver

FEATURES AND BENEFITS

- Wide, 2.7 to 15 V input voltage operating range
- Dual DMOS full-bridges: drive two DC motors or one stepper motor
- Low $R_{DS(ON)}$ outputs
- Synchronous rectification for reduced power dissipation
- Low-current sleep mode
- Overcurrent protection
- Internal UVLO and thermal shutdown circuitry
- Integrated charge pump
- Pin-to-pin compatible with A3906

PACKAGES:



16-contact QFN
3 mm × 3 mm
(suffix ES)

20-contact QFN
4 mm × 4 mm
(suffix ES,-1)

Not to scale

DESCRIPTION

Designed for pulse-width-modulated (PWM) control of low-voltage stepper motors and single and dual DC motors, the A3916 is capable of output currents up to 1 A per channel and operating voltages from 2.7 to 15 V.

The A3916 has an internal fixed off-time PWM timer that sets a peak current based on the selection of a current sense resistor. An output fault flag is provided that notifies the user of a TSD or overcurrent protection event.

The A3916 is supplied in a low-profile 3 × 3 mm 16-terminal QFN (suffix “ES”) and a low-profile 4 × 4 mm 20-terminal QFN (suffixes “ES, -1”) both with exposed power tabs for enhanced thermal dissipation.

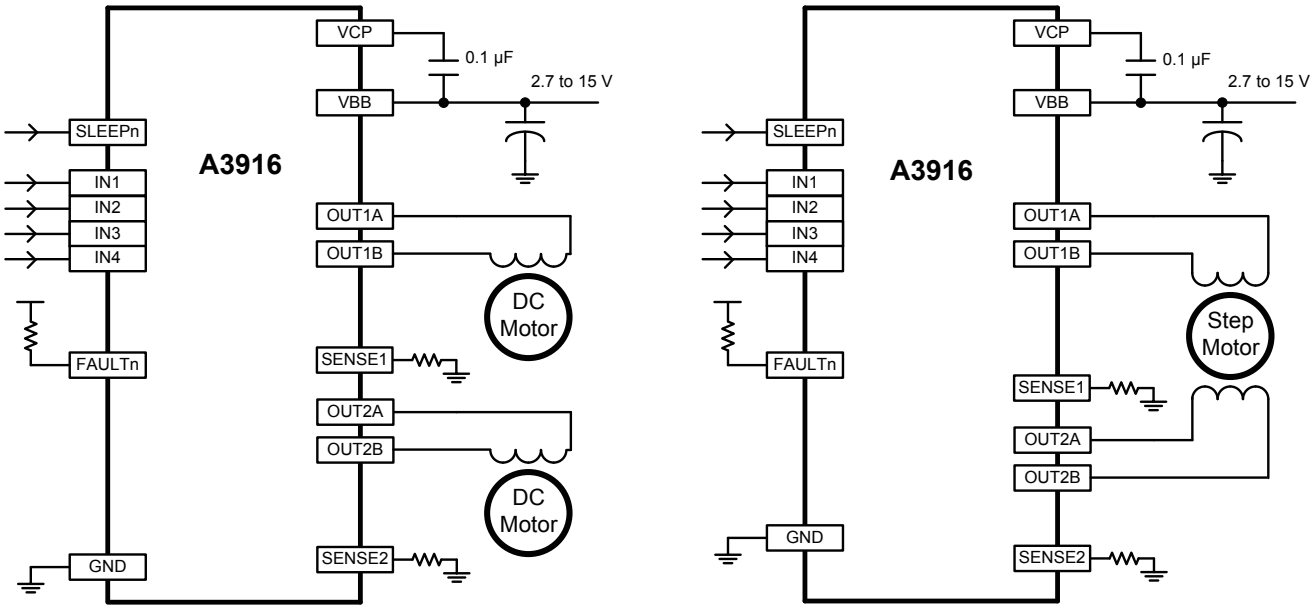


Figure 1: Typical Applications

SPECIFICATIONS

SELECTION GUIDE

Part Number	Packaging	Packing
A3916GESTR-T	3 × 3 mm 16-contact QFN package	1500 pieces per 7-inch reel
A3916GESTR-T-1	4 × 4 mm 20-contact QFN package	1500 pieces per 7-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		15	V
Output Current	I_{OUT}	Continuous	1.0	A
Output Current (parallel mode)	$I_{OUT(PAR)}$	Continuous	1.8	A
Sense Voltage	V_{SENSEx}	Continuous	0.5	V
		Pulsed, t_w < 1 µs	2.5	V
Logic Input Voltage Range	V_{IO}		–0.3 to 5.5	V
Junction Temperature	$T_{J(MAX)}$		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A	Range G	–40 to 105	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
3 × 3 mm ES package	RθJA	4-layer PCB based on JEDEC standard	47	°C/W
4 × 4 mm ES-1 package		4-layer PCB based on JEDEC standard	37	°C/W

*Additional thermal information available on the Allegro website.

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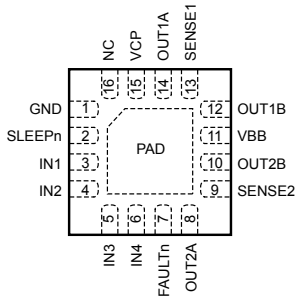
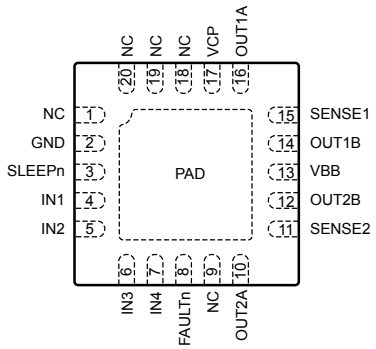
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



16-Contact QFN (ES) Package



20-Contact QFN (ES, -1) Package

Terminal List Table

Number		Name	Function
ES	ES, -1		
1	2	GND	Ground
2	3	SLEEPn	Active-Low Sleep Input
3	4	IN1	Control Input
4	5	IN2	Control Input
5	6	IN3	Control Input
6	7	IN4	Control Input
7	8	FAULTn	Open-Drain Logic Output
8	10	OUT2A	DMOS H-Bridge 2, Output A
9	11	SENSE2	Sense Resistor Terminal, Bridge 2
10	12	OUT2B	DMOS H-Bridge 2, Output B
11	13	VBB	Motor Supply Voltage
12	14	OUT1B	DMOS H-Bridge 1, Output B
13	15	SENSE1	Sense Resistor Terminal, Bridge 1
14	16	OUT1A	DMOS H-Bridge 1, Output A
15	17	VCP	Charge Pump Capacitor
16	1,9,18,19,20	NC	No Internal Connection
–	–	PAD	Exposed Pad for Enhanced Thermal Performance

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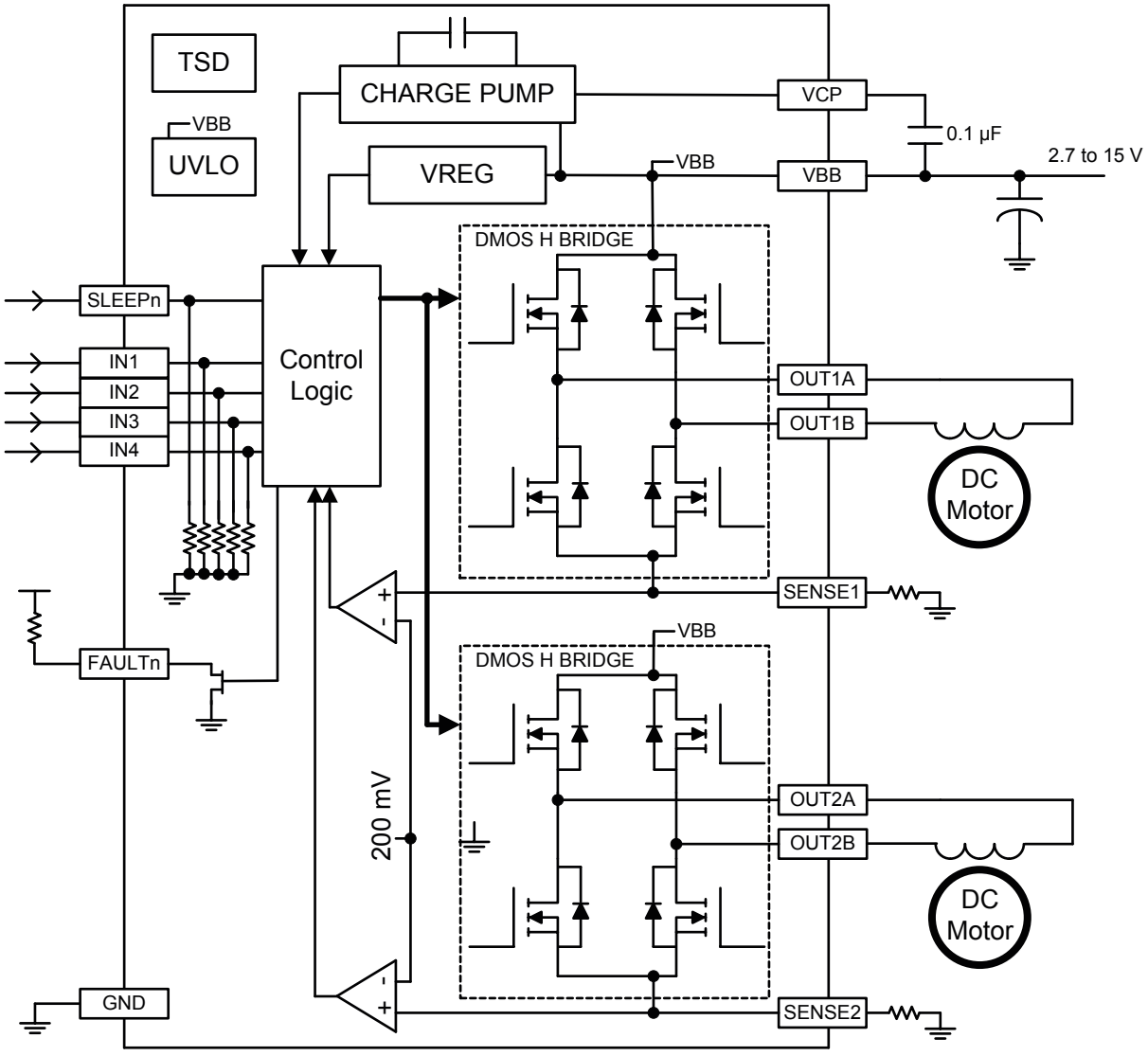
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS [1][2]: Valid at T_J = 25°C, V_{BB} = 2.7 to 15 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
Load Supply Voltage Range	V_{BB}	Operating	2.7	–	15	V
Output On Resistance	$R_{DS(ON,HS)}$	T_J = 25°C, 500 mA, V_{BB} = 5 V	–	335	450	mΩ
		T_J = 25°C, 500 mA, V_{BB} = 2.7 V	–	335	450	mΩ
		T_J = 85°C, 500 mA, V_{BB} = 5 V	–	410	–	mΩ
		T_J = 85°C, 500 mA, V_{BB} = 2.7 V	–	410	–	mΩ
	$R_{DS(ON,LS)}$	T_J = 25°C, 500 mA, V_{BB} = 5 V	–	375	525	mΩ
		T_J = 25°C, 500 mA, V_{BB} = 2.7 V	–	375	525	mΩ
		T_J = 85°C, 500 mA, V_{BB} = 5 V	–	455	–	mΩ
		T_J = 85°C, 500 mA, V_{BB} = 2.7 V	–	455	–	mΩ
Diode Forward Voltage	V_F	I = 500 mA	–	0.85	1.0	V
VBB Supply Current	$I_{BB(2p7V)}$	Outputs disabled, V_{BB} = 2.7 V	–	2.2	4.5	mA
	$I_{BB(15V)}$	Outputs disabled, V_{BB} = 15 V	–	3.1	4.5	mA
	$I_{BB(SLEEP)}$	Sleep Mode	–	–	0.5	µA
CONTROL LOGIC						
Logic Input Voltage, INx	$V_{IN(1)}$		2.0	–	–	V
	$V_{IN(0)}$		–	–	0.8	V
Logic Input Voltage, SLEEPn	$V_{IN(1)}$		2.0	–	–	V
	$V_{IN(0)}$		–	–	0.4	V
Logic Input Hysteresis	V_{HYS}		100	–	500	mV
Logic Input Current	I_{IN}	V_{IN} = 3.3 V, pulldown = 100 kΩ	–	33	50	µA
Fault Output Voltage	V_{FAULTn}	Flag asserted, I_{FAULTn} = 1 mA	–	–	200	mV
Fault Output Leakage Current	I_{FAULTn}	V_{FAULTn} = 5 V	–	–	1.0	µA
V_{SENSE} Blank time	t_{BLANK}		2.1	3.1	4.1	µs
V_{SENSE} Trip Voltage	V_{TRIP}		170	205	240	mV
Fixed Off-Time	t_{OFF}		20	30	40	µs
PROTECTION CIRCUITS						
Crossover Delay	t_{OCD}		200	550	1000	ns
VBB Undervoltage Lockout	$V_{BB(UVLO)}$	V_{BB} rising	–	2.55	2.65	V
VBB Hysteresis	$V_{BB(UVLO,HYS)}$		–	125	–	mV
Thermal Shutdown Temperature	T_{J1}		150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_{J1}		–	20	–	°C

[1] Typical data is for design information only.
[2] Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

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CONTROL LOGIC

Table 1: DC Motor Operation

IN1	IN2	OUT1A	OUT1B	Function
0	0	Off	Off	Disabled
1	0	High	Low	Forward
0	1	Low	High	Reverse
1	1	Low	Low	Brake

IN3	IN4	OUT2A	OUT2B	Function
0	0	Off	Off	Disabled
1	0	High	Low	Forward
0	1	Low	High	Reverse
1	1	Low	Low	Brake

Table 2: Stepper Motor Operation

IN1	IN2	IN3	IN4	OUT1A	OUT1B	OUT2A	OUT2B	Function	
0	0	0	0	Off	Off	Off	Off	Disabled	Disabled
1	0	1	0	High	Low	High	Low	Full Step 1	½ Step 1
0	0	1	0	Off	Off	High	Low	–	½ Step 2
0	1	1	0	Low	High	High	Low	Full Step 2	½ Step 3
0	1	0	0	Low	High	Off	Off	–	½ Step 4
0	1	0	1	Low	High	Low	High	Full Step 3	½ Step 5
0	0	0	1	Off	Off	Low	High	–	½ Step 6
1	0	0	1	High	Low	Low	High	Full Step 4	½ Step 7
1	0	0	0	High	Low	Off	Off	–	½ Step 8

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FUNCTIONAL DESCRIPTION

Device Operation

The A3916 is a dual full-bridge motor driver capable of operating one stepper motor, two DC motors, or one high-current DC motor. MOSFET output stages substantially reduce the voltage drop and the power dissipation of the A3916 outputs, compared to typical drivers with bipolar transistors.

Output current can be regulated by pulse-width modulating (PWM) the inputs. In addition to supporting external PWM of the driver, the A3916 limits the peak current by internally PWMing the source driver when the current in the winding exceeds the peak current, as determined by a sense resistor. If internal current limiting is not needed, the sense pin should be shorted to ground.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage lockout, internal clamp diodes, crossover current protection, and overcurrent protection.

External PWM

Output current regulation can be achieved by pulse-width modulating the inputs. Slow decay mode is selected by holding one input high while PWMing the other input. Holding one input low and PWMing the other input results in fast decay.

Blanking

This function blanks the output of the current sense comparator when the outputs are switched. The comparator output is blanked to prevent false current limit detections due to reverse recovery currents of the clamp diodes or to switching transients related to the capacitance of the load. The blank time, t_{BLANK}, is approximately 3 µs.

Sleep Mode

An active-low control input used to minimize power consumption when the A3916 is not in use. This disables much of the internal circuitry including the output drivers, internal regulator, and charge pump. A logic high allows normal operation. When coming out of sleep mode, wait 1.5 ms before issuing a command to allow the internal regulator and charge pump to stabilize.

Enable

When all logic inputs are pulled to logic low, the outputs of the bridges are disabled. The charge pump and internal circuitry continue to run when the outputs are disabled.

Thermal Shutdown

The A3916 will disable the outputs if the junction temperature reaches 165°C. When the junction temperature drops 20°C, the outputs will be enabled.

Brake Mode

When driving DC motors, the A3916 goes into brake mode (turns on both sink drivers) when both of its inputs are high (IN1 and IN2, or IN3 and IN4). There is no current limiting during braking, so care must be taken to ensure that the peak current during braking does not exceed the absolute maximum current.

Internal PWM Current Control

Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and the current sense resistor, R_{SENSEx}. When the voltage across R_{SENSEx} equals the internal reference voltage, the current sense comparator resets the PWM latch, which turns off the source driver.

The maximum value of current limiting, $I_{TRIP(max)}$, is set by the selection of the sense resistor, R_{SENSEx}, and is approximated by a transconductance function:

$$I_{TRIP(max)} = 0.2 \div R_{SENSEx}$$

It is critical to ensure the maximum rating on SENSEx pins (0.5 V) is not exceeded.

Synchronous Rectification

When a PWM off-cycle is triggered by an internal fixed off-time cycle, load current recirculates in slow decay SR mode. During slow decay, current recirculates through the sink-side FET and the sink-side body diode. The SR feature enables the sink-side FET, effectively shorting out the body diode. The sink driver is

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not enabled until the source driver is turned off and the cross-over delay has expired. This feature helps lower the voltage drop during current recirculation, lowering power dissipation in the bridge.

OCP

The voltage across enabled output drivers is monitored to protect against short circuits. If an overcurrent protection event occurs, both motor bridges are disabled until either SLEEPn is brought low or the VBB supply is cycled.

FAULTn

This is an open-drain output that is pulled low during a TSD or overcurrent protection event. For a TSD event, The output is released when the die temperature falls below the TSD level minus the hysteresis. For an over-current event, the output is held low until either SLEEPn is brought low or the VBB supply is cycled.

Parallel Operation

The A3916 can be paralleled for applications that require higher output currents. In paralleled mode, the driver can source 1.8 A continuous. The A3916 has two completely independent bridges with separate internal current limit latches. This allows the device to supply two separate loads, and as a result, when paralleled, it is imperative that the internal current control is disabled by shorting the sense pins to ground.

Because the internal current limit trip threshold is internally fixed at 0.2 V, the trace resistance must be kept small so the internal current latch is not triggered prematurely. With acceptable margin, the voltage drop across the trace resistance should be under 0.1 V. At a peak current of 2.5 A, the trace resistance should be kept below 40 mΩ to prevent false tripping of the overcurrent latch.

Each bridge has some variation in propagation delay. During this time, it is possible that one bridge will have to support the full load current for a very short period of time. Propagation delays are characterized and guard banded to protect the driver from damage during these events.

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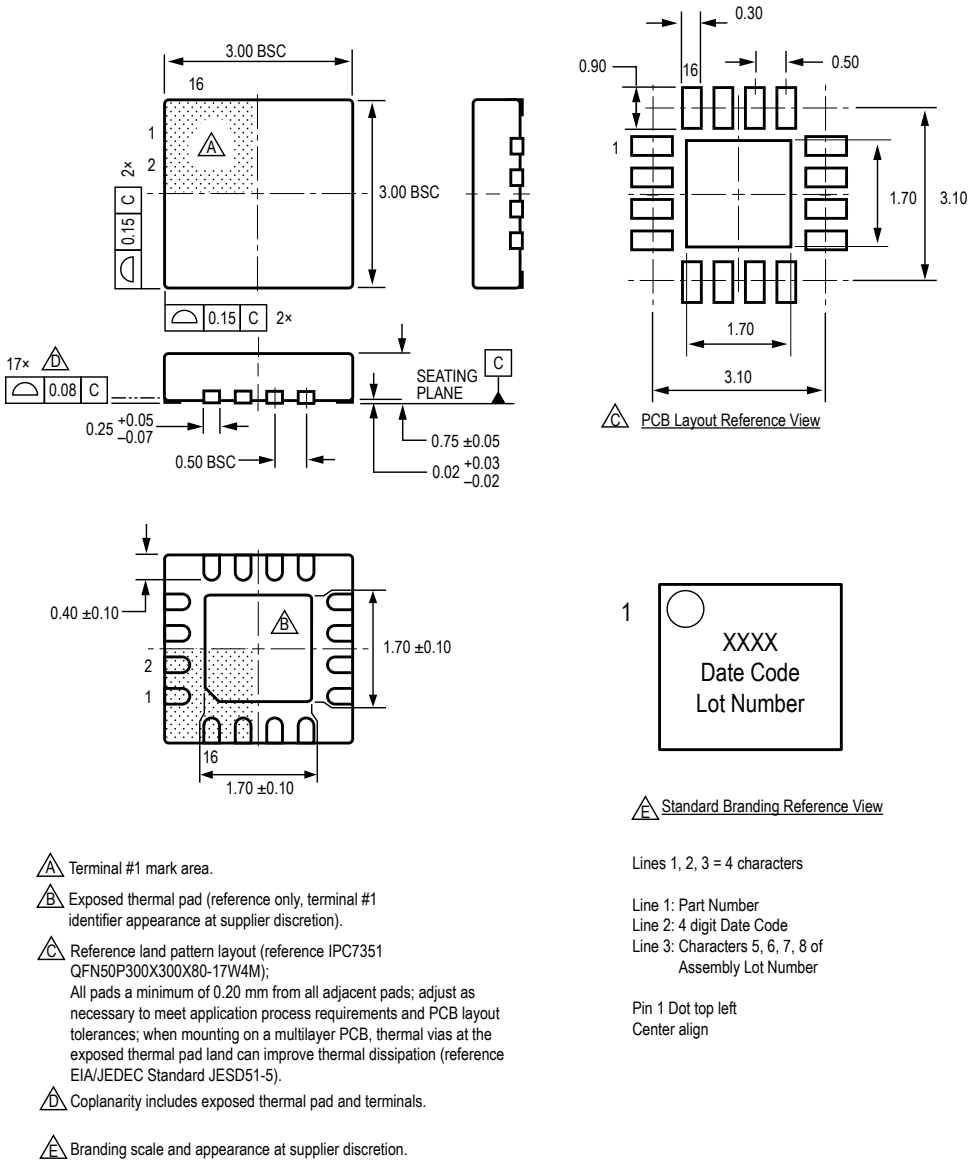
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area.

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Coplanarity includes exposed thermal pad and terminals.

E Branding scale and appearance at supplier discretion.

Lines 1, 2, 3 = 4 characters

Line 1: Part Number
Line 2: 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

Figure 2: 16-contact 3 mm × 3 mm QFN package (Suffix ES)

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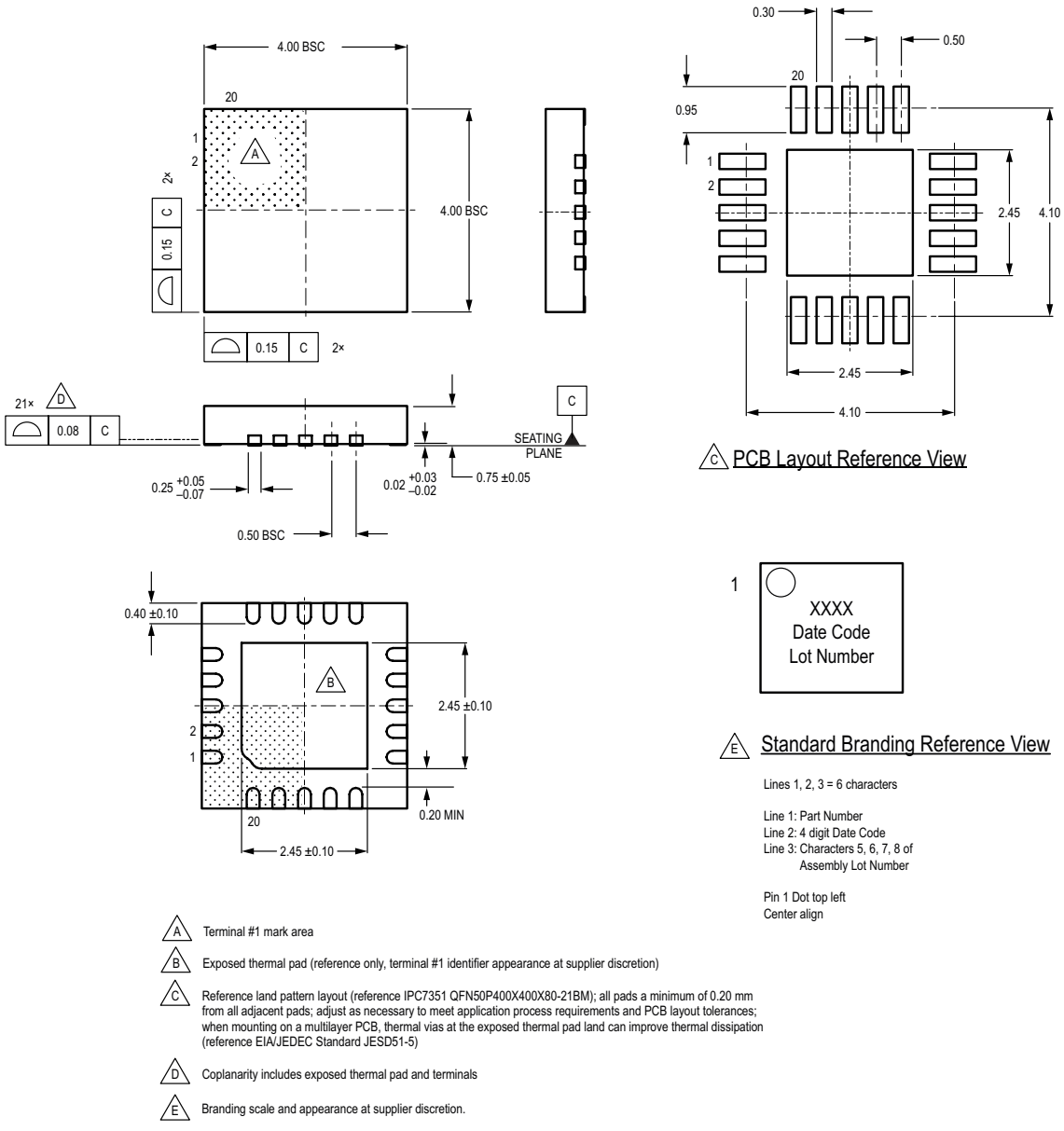
For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion.

Figure 3: 20-contact 4 mm × 4 mm QFN package (Suffix ES, -1)

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Revision History

Number	Date	Description
–	September 21, 2016	Initial release
1	October 7, 2016	Updated Features and Benefits (page 1) and Output On Resistance (page 5); corrected Selection Guide (page 2).
2	January 18, 2017	Corrected VBB Hysteresis units (page 5).
3	January 19, 2018	Updated Blanking (page 7), OCP, Faultn, and Parallel Operations sections (page 8).
4	January 27, 2019	Minor editorial updates
5	February 3, 2020	Minor editorial updates
6	February 3, 2022	Updated package drawings (pages 9-10)

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