

# MSC8103

## Networking Digital Signal Processor

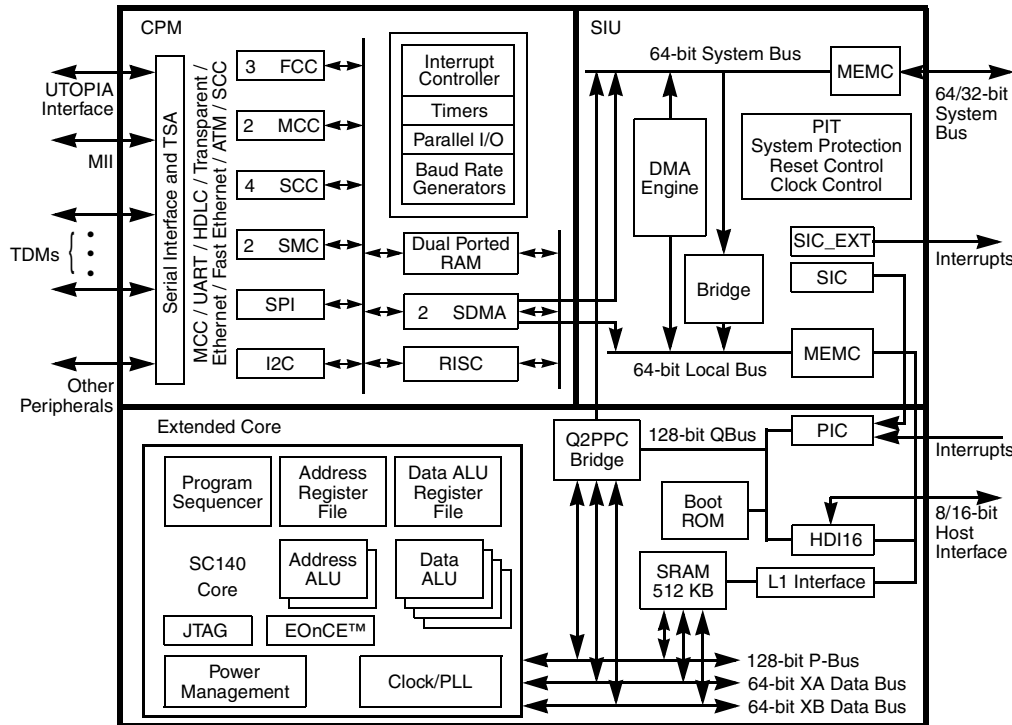


Figure 1. MSC8103 Block Diagram

*The Freescale MSC8103 16-bit Digital Signal Processor (DSP) is a member of the family of DSPs based on the StarCore™ SC140 DSP core. The MSC8103 is offered in two core speed levels: 275 and 300 MHz.*

The Freescale MSC8103 DSP is a very versatile device that integrates the high-performance SC140 four-ALU (arithmetic logic unit) DSP core along with 512 KB of on-chip memory, a communications processor module (CPM), a 64-bit bus, a very flexible system integration unit (SIU), and a 16-channel DMA controller on a single device. With its four-ALU core, the MSC8103 can execute up to four multiply-accumulate (MAC) operations in a single clock cycle. The MSC8103 CPM is a 32-bit RISC-based communications protocol engine that can network to time-division multiplexed (TDM) highways, Ethernet, and asynchronous transfer mode (ATM) backbones. The MSC8103 60x-compatible bus interface connects to multi-master system architectures. The large on-chip unified program and data SRAM, 512 KB, reduces the need for off-chip memories. The MSC8103 offers 1200 DSP MMACS performance using an internal 300 MHz clock with a 1.6 V core and independent 3.3 V input/output (I/O).

# Features

- SC140 core
  - Architecture optimized for efficient C/C++ code compilation
  - Four 16-bit ALUs and two 32-bit AGUs
  - 1200 MMACS, 3000 RISC MIPS, running at 300 MHz
  - Very low power dissipation—less than 0.25 W for the core running full speed at 1.6 V
  - Variable-length execution set (VLES) execution model improves code density
  - JTAG/enhanced OnCE debug port
- Communications processor module (CPM)
  - Programmable protocol machine using a 32-bit RISC engine
  - 155 Mbps ATM interface (including AAL 0/1/2/5)
  - 10/100 Mbit Ethernet interface
  - Up to four E1/T1 interfaces or one E3/T3 interface and one E1/T1 interface
  - HDLC support up to T3 rates, or 256 channels
- 100 MHz 64- or 32-bit wide bus interface
  - Bursts for high efficiency
  - Glueless interface to 60x-compatible bus systems
  - Multi-master support
- Programmable memory controller
  - Control for up to eight banks of external memory
  - User-programmable machines (UPM) allowing glueless interface to various memory types (SRAM, DRAM, EPROM, and Flash memory) and other user-definable peripherals
  - Dedicated pipelined SDRAM memory interface
- Large on-chip SRAM
  - 256K 16-bit words (512 KB)
  - Unified program and data space configurable by the application
  - Word and byte addressable
- DMA controller
  - 16 DMA channels, FIFO based, with burst capabilities
  - Sophisticated addressing capabilities
- Small footprint package: 17 mm × 17 mm lidded FC-PBGA package with lead-bearing or lead-free spheres
- Very low power consumption
- Separate power supply for internal logic (1.6 V) and for I/O (3.3 V)
- Enhanced 16-bit parallel host interface (HDI16) supports a variety of microcontroller, microprocessor, and DSP bus interfaces
- Phase-lock loops (PLLs)
  - System PLL
  - CPM DPLLs (SCC and SCM)
- Process technology: 0.13 micron copper interconnect

# Target Applications

The MSC8101 targets applications requiring very high performance, very large amounts of on-chip memory, and such networking capabilities as:

- Third-generation wideband wireless infrastructure systems
- Packet telephony systems
- Multi-channel modem banks
- Multi-channel xDSL

# Product Documentation

The documents listed in **Table 1** are required for a complete description of the MSC8103 and are necessary to design properly with the part. Documentation is available from the following sources (see back cover for detailed information):

- A local Freescale distributor
- A Freescale Semiconductor sales office
- A Freescale literature distribution center
- The world wide web (WWW)

**Table 1.** MSC8103 Documentation

Name	Description	Order Number
<i>MSC8103 Technical Data</i>	MSC8103 features list and physical, electrical, timing, and package specifications	MSC8103
<i>MSC8103 User's Guide</i>	Detailed functional description of the MSC8103 memory configuration, operation, and register programming	MSC8103UG
<i>MSC8103 Reference Manual</i>	Detailed description of the MSC8103 processor core and instruction set	MSC8103RM
<i>SC140 DSP Core Reference Manual</i>	Detailed description of the SC140 family processor core and instruction set	MNSC140CORE
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the MSC8103 product website

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