

User's Guide

OPA3S328 Evaluation Module



ABSTRACT

This user's guide contains information and support documentation for the OPA3S328 evaluation module (EVM). Included are the circuit description, jumper settings, required connections, printed circuit board (PCB) layout, schematic, and bill of materials of the OPA3S328EVM. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the OPA3S328EVM.

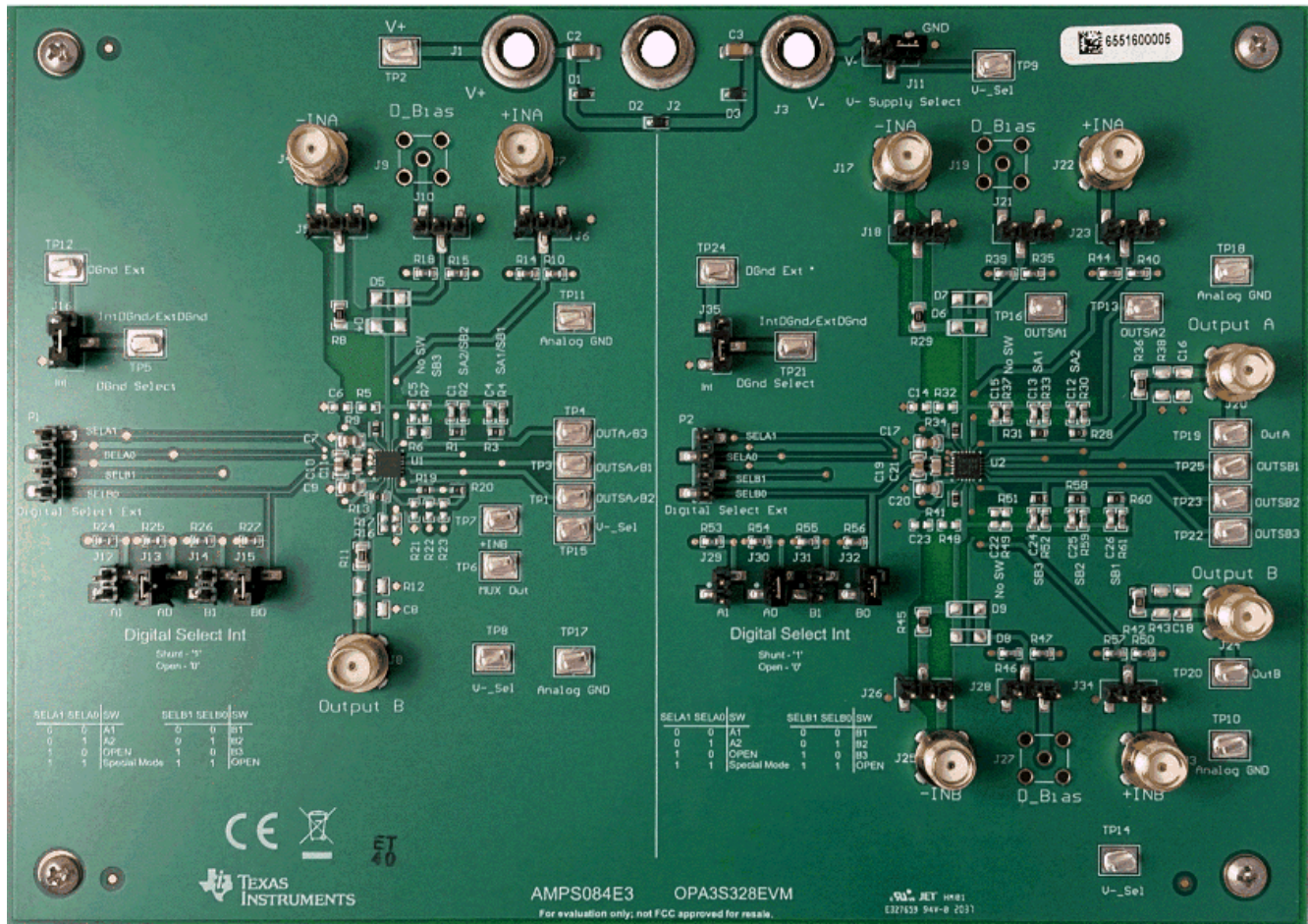


Table of Contents

1 Overview	3
1.1 Related Documentation.....	3
1.2 Electrostatic Discharge Caution.....	3
2 EVM Circuit Description	4
3 Jumper Settings	6
4 Power-Supply Connections	9
5 Input and Output Connections	10
6 Modifications	11

7 Schematic, PCB Layout, and Bill of Materials	11
7.1 Schematic.....	12
7.2 PCB Layout.....	14
7.3 Bill of Materials.....	19

List of Figures

Figure 2-1. OPA3S328EVM Site 1 Simplified Schematic.....	4
Figure 2-2. OPA3S328EVM Site 2 Simplified Schematic.....	5
Figure 3-1. OPA3S328EVM Default Jumper Settings.....	6
Figure 4-1. OPA3S328EVM Voltage Supply Connections.....	9
Figure 7-1. OPA3S328EVM Schematic - Site 1.....	12
Figure 7-2. OPA3S328EVM Schematic - Site 2.....	13
Figure 7-3. Top Overlay.....	14
Figure 7-4. Top Layer PCB Layout.....	15
Figure 7-5. Ground Layer PCB Layout.....	16
Figure 7-6. Power Layer PCB Layout.....	17
Figure 7-7. Bottom Layer PCB Layout.....	18

List of Tables

Table 1-1. Related Documentation.....	3
Table 3-1. Default Jumper Configuration.....	6
Table 3-2. Select Pin Gain Decoder for Site 1	7
Table 3-3. Select Pin Gain Decoder for Site2, Amplifier A	8
Table 3-4. Select Pin Gain Decoder for Site2, Amplifier B	8
Table 4-1. OPA3S328EVM Supply-Range Specifications.....	9
Table 5-1. OPA3S328EVM Site 1 Input and Output Connections.....	10
Table 5-2. OPA3S328EVM Site 2 Input and Output Connections.....	10
Table 7-1. OPA3S328EVM Bill of Materials.....	19

Trademarks

All other trademarks are the property of their respective owners.

1 Overview

The OPA3S328 is a precision, low-voltage CMOS operational amplifier with integrated switches optimized for transimpedance applications from Texas Instruments. For a full list of electrical characteristics for the OPA3S328, see the [OPA3S328 40-MHz CMOS Amplifier With Switches Data Sheet](#).

1.1 Related Documentation

The following document provides information regarding Texas Instruments integrated circuits used in the assembly of the OPA3S328EVM. This user's guide is available from the TI website under literature number SBOU231. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI website at <http://www.ti.com/>, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

Table 1-1. Related Documentation

Device	Literature Number
OPA3S328	SBOS937

1.2 Electrostatic Discharge Caution

Many of the components on the OPA3S328EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

2 EVM Circuit Description

The OPA3SS28 is a dual operational amplifier with integrated switches for transimpedance applications. This EVM provides access to the features and measure the performance of the OPA3S328. The OPA3S328EVM features two independent sites with OPA3S328 devices on different circuit configurations: site 1 and site 2.

Site 1 incorporates OPA3S328 device U1 with amplifier U1A configured in the transimpedance configuration, with two possible transimpedance gains: 2 k Ω connected to switch SA1 and 200 k Ω connected to switch SA2. Amplifier U1B is configured by default as a high-impedance buffer, with switches SB1, SB2, and SB3 configured to sense the selected transimpedance gain. The simplified schematic of site 1 is displayed in [Figure 2-1](#).

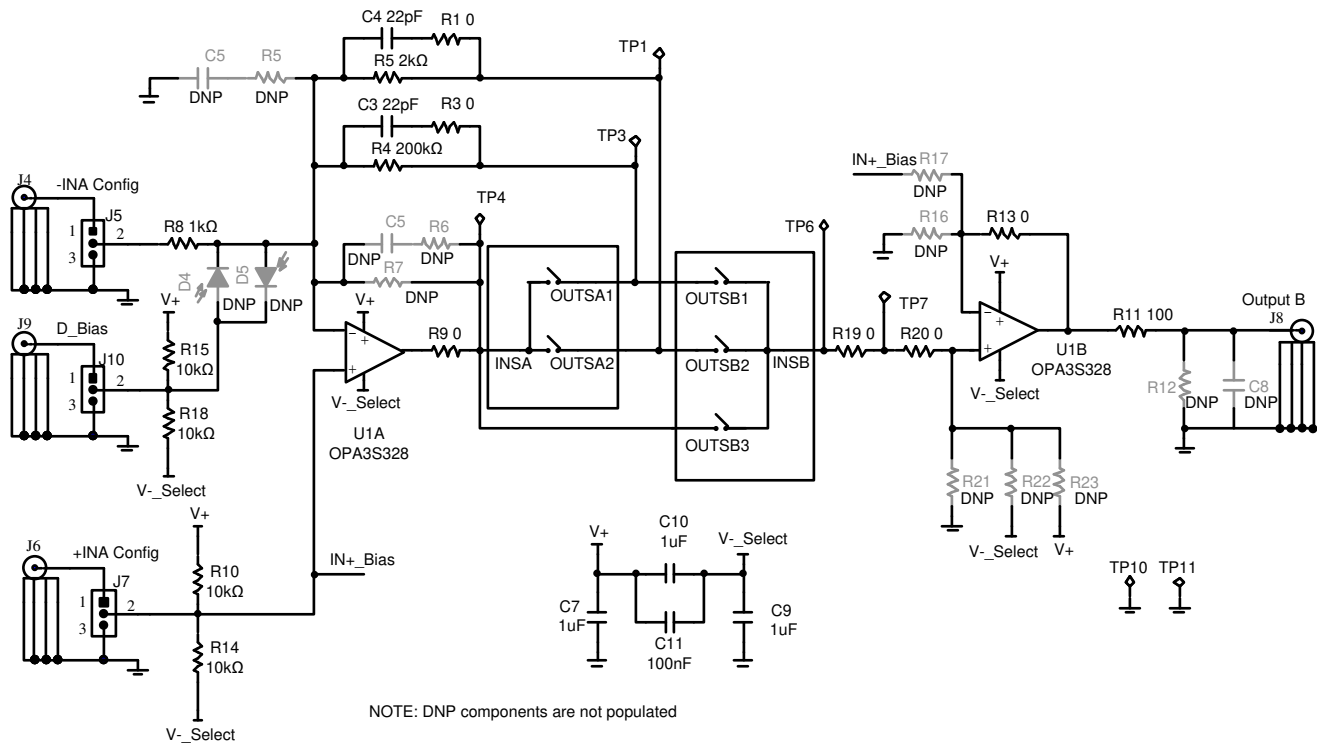


Figure 2-1. OPA3S328EVM Site 1 Simplified Schematic

Site 2 incorporates OPA3S328 device U2 with amplifier U2A configured in the transimpedance configuration, with three possible transimpedance gains: 20 kΩ connected to switch SA1 , 2 kΩ to SA2 and a fixed feedback resistor and unswitched feedback resistor of 200 kΩ. Amplifier U2B is also configured in the transimpedance configuration, with three possible gains: 2 kΩ connected to switch SB3, 20 kΩ to switch SB2 and 200 kΩ to switch SB1.

The simplified schematic of site 2 is displayed in Figure 2-2.

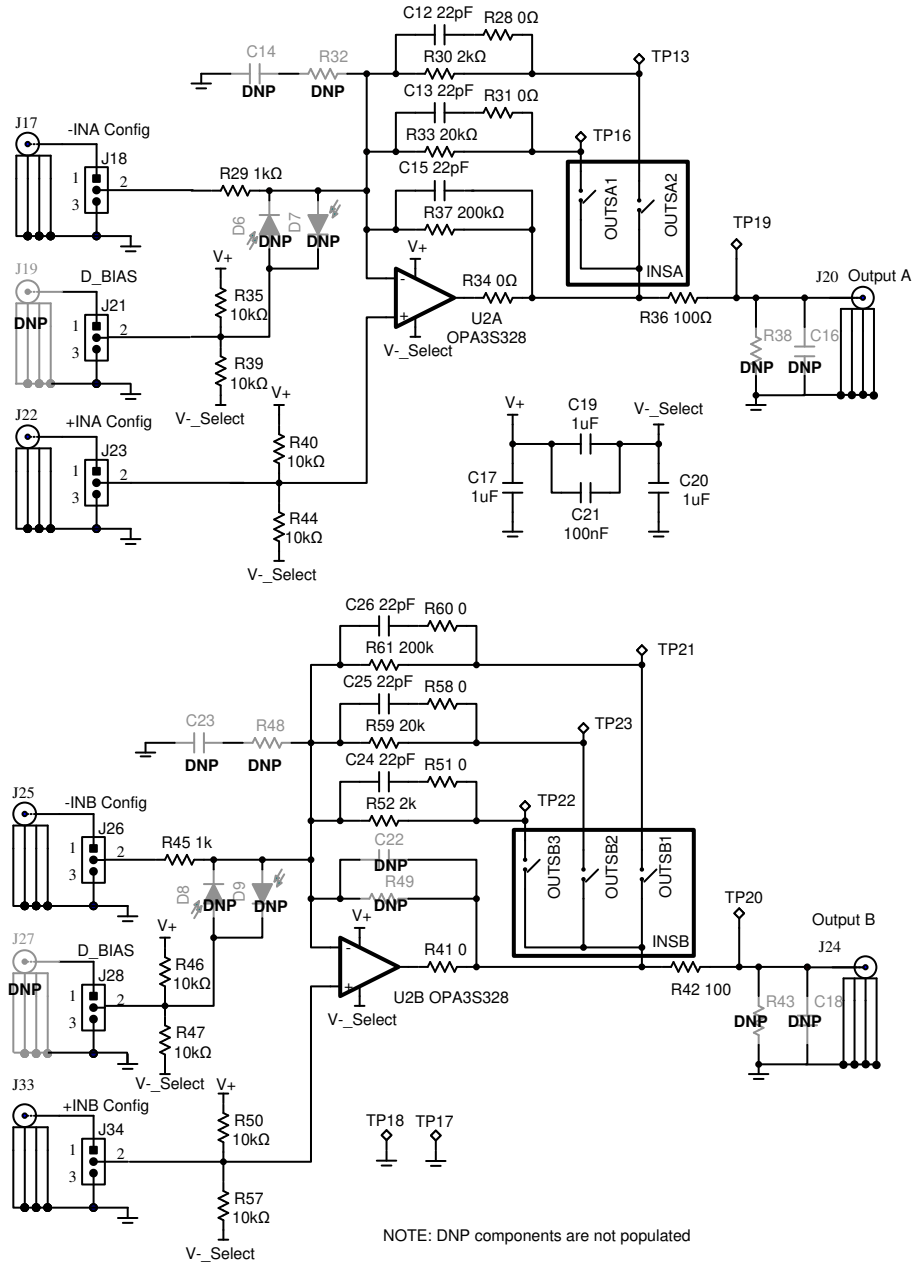


Figure 2-2. OPA3S328EVM Site 2 Simplified Schematic

3 Jumper Settings

Figure 3-1 details the default jumper settings of the OPA3S328EVM. Table 3-1 explains the configuration for these jumpers.

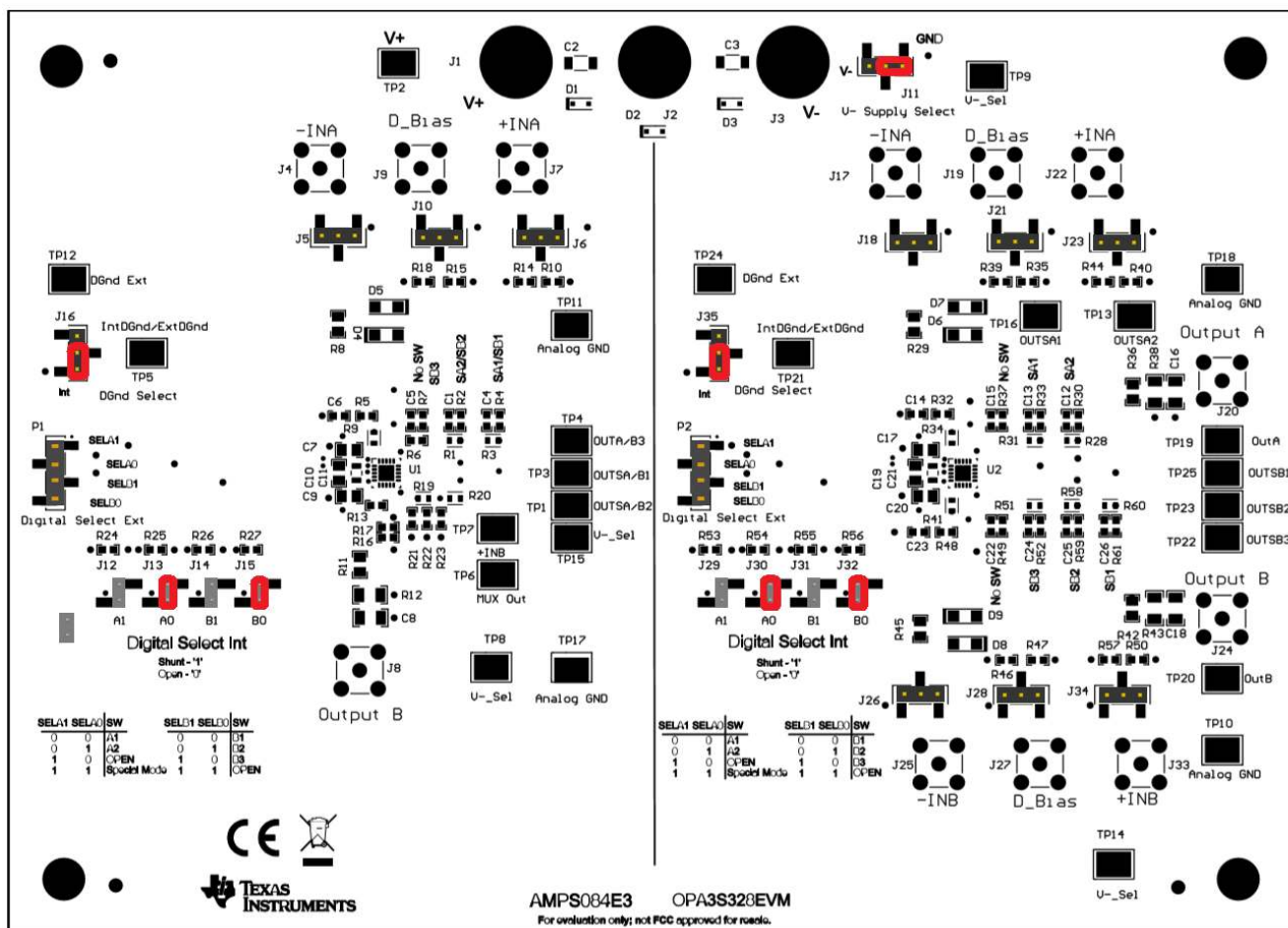


Figure 3-1. OPA3S328EVM Default Jumper Settings

Table 3-1. Default Jumper Configuration

Jumper	Function	Default Position	Description
J11	V- Supply Select	Shunt 2-3	Shunt 2-3: Selects AGND as V- for unipolar supply configuration Shunt 1-2: Selects Ext V- supply for bipolar supply configuration
J16	Int DGND / Ext DGND: Site 1	Shunt 1-2	Site 1 internal or external DGND: Shunt 1-2: Selects internal DGND (AGND) Shunt 2-3: Selects external DGND
J35	Int DGND / Ext DGND: Site 2	Shunt 1-2	Site 2 internal or external DGND: Shunt 1-2: Selects internal DGND (AGND) Shunt 2-3: Selects external DGND
J5	-IN Input Amp A, Site 1	Open	Inverting input, amplifier A, site 1: Shunt 1-2: Selects external signal through SMA J4 Shunt 2-3: Selects AGND Open: Bias at Vsupply/2
J10	Photodiode BIAS Amp A, Site 1	Open	Photodiode bias, amplifier A, site 1: Shunt 1-2: Selects external bias through SMA J9 Shunt 2-3: Selects AGND Open: Bias at Vsupply/2

Table 3-1. Default Jumper Configuration (continued)

Jumper	Function	Default Position	Description
J6	+IN Input Amp A, Site 1	Open	Non-inverting input, amplifier A, site 1: Shunt 1–2: Selects external signal through SMA J7 Shunt 2–3: Selects AGND Open: Bias at $V_{supply} / 2$
J18	-IN Input Amp A, Site 2	Open	Inverting input, amplifier A, site 2: Shunt 1–2: Selects external signal through SMA J17 Shunt 2–3 selects AGND Open: Bias at $V_{supply}/2$
J21	Photodiode BIAS Amp A, Site 2	Open	Photodiode bias, amplifier A, site 2: Shunt 1–2: Selects external bias through SMA J19 Shunt 2–3: Selects AGND Open: Bias at $V_{supply}/2$
J23	+IN Input Amp A, Site 2	Open	Non-inverting input, amplifier A, site 2: Shunt 1–2: Selects external signal through SMA J22 Shunt 2–3: Selects AGND Open: Bias at $V_{supply} / 2$
J26	-IN Input Amp B, Site 2	Open	Inverting input, amplifier B, site 2: Shunt 1–2: Selects external signal through SMA J25 Shunt 2–3: Selects AGND Open: Bias at $V_{supply}/2$
J28	Photodiode BIAS Amp B, Site 2	Open	Photodiode bias, amplifier B, site 2: Shunt 1–2: Selects external bias through SMA J27 Shunt 2–3: Selects AGND Open: Bias at $V_{supply} / 2$
J34	+IN Input Amp B, Site 2	Open	Non-inverting input, amplifier B, site 2: Shunt 1–2: Selects external signal through SMA J33 Shunt 2–3: Selects AGND Open: Bias at $V_{supply} / 2$
J12–J15	Input select for switch matrix, Site 1	J12 - Open J13 - Shunt J14 - Open J15 - Shunt	Site 1 SELA0, SELA1, SELB0, SELB1: Digital input pins for switch and shutdown control: Open: Low Shunt: High
J29–J32	Input select for switch matrix, Site 2	J29 - Open J30 - Shunt J31 - Open J32 - Shunt	Site 1 SELA0, SELA1, SELB0, SELB1: Digital input pins for switch and shutdown control: Open: Low Shunt: High

Table 3-2 details the select pin (SELxx) gain decoder for site 1 connections. For the special case with SELA0 = SELA1 = 1 (device on shutdown mode) decoder table, consult the [OPA3S328 data sheet](#).

Table 3-2. Select Pin Gain Decoder for Site 1

SELA1 J12	SELA0 J13	SELB1 J14	SELB0 J15	Switch Configuration, Gain
Low (Open)	Low (Open)	Low (Open)	Low (Open)	A1: Closed, A2: Open B1: Closed, B2: Open, B3:Open Selects feedback R4 (G = 200 kΩ)
Low (Open)	High (Shunt)	Low (Open)	High (Shunt)	A1: Open, A2: Closed B1: Open, B2:Closed, B3:Open Selects feedback R2 (G = 2 kΩ)
High (Shunt)	Low (Open)	High (Shunt)	Low (Open)	A1: Open, A2: Open B1: Open, B2:Open, B3:Closed Selects default feedback R7 (R7 is Unpopulated)

Table 3-3 details the select pin (SELxx) gain decoder for amplifier A site 2 connections. Table 3-4 shows the select pin (SELxx) gain decoder for amplifier B site 2 connections. For the select pin decoder special case with SELA0 = SELA1 = 1 (shutdown mode), consult the [OPA3S328 data sheet](#).

Table 3-3. Select Pin Gain Decoder for Site2, Amplifier A

SELA1 J29	SELA0 J30	Switch Configuration, Gain
Low (Open)	Low (Open)	A1: Closed, A2: Open Selects feedback R33 (20 kΩ, Switch A1) in parallel with default feedback R37 (200 kΩ) Gain = $20\text{ k}\Omega 200\text{ k}\Omega$ = approximately 181.8 kΩ
Low (Open)	High (Shunt)	A1: Open, A2: Closed Selects feedback R30 (20 kΩ, Switch A2) in parallel with default feedback R37 (200 kΩ) Gain = $2\text{ k}\Omega 200\text{ k}\Omega$ = approximately 1.98 kΩ
High (Shunt)	Low (Open)	A1: Open, A2: Open Selects feedback default feedback R37 (200 kΩ) Gain = 200 kΩ

Table 3-4. Select Pin Gain Decoder for Site2, Amplifier B

SELB1 J31	SELB0 J32	Switch Configuration, Gain
Low (Open)	Low (Open)	B1: Closed, B2: Open, B3: Open Selects feedback R61 Gain = 200 kΩ
Low (Open)	High (Shunt)	B1: Open, B2: Closed, B3: Open Selects feedback R59 Gain = 20 kΩ
High (Shunt)	Low (Open)	B1: Open, B2: Open, B3: Closed Selects feedback R52 Gain = 2 kΩ
High (Shunt)	High (Shunt)	B1: Open, B2: Open, B3: Open Selects default feedback R49 (unpopulated, feedback Open)

4 Power-Supply Connections

The power-supply connections for the OPA3S328EVM are provided through standard banana jack connectors J1, J2, and J3 at the top of the EVM. The OPA3S328EVM can be set up with a single unipolar supply or with dual bipolar supplies by setting jumper J11. Table 4-1 summarizes the pin definition for supply connector J1, J2, and J3 and the allowed voltage range for each supply connection when configured with either unipolar or bipolar supplies.

Table 4-1. OPA3S328EVM Supply-Range Specifications

Pin Number	Supply Connection	Voltage Range
J1	(V+) supply	Unipolar: 2.2 V to 5.5 V Bipolar: 1.1 V to 2.75 V
J2	Analog Ground	0 V
J3	(V-) Supply	Unipolar: Do not Connect Bipolar: -1.1 V to -2.75 V

The EVM is configured by default to use a single unipolar supply by shunting jumper J11 pin 2–3. To configure the device with dual bipolar supply, set jumper J11 to shunt pin 1–2.

The digital ground pin (GND) of each site can be connected to analog ground or can be biased externally. The digital ground pin of site 1 is configured by setting jumper J16. Site 2 is configured by setting jumper J35. The EVM configures by default the digital ground connections to analog Ground by shunting pins 1–2. Place J16 and J35 to shunt pins 2–3 to bias the device digital GND to an external voltage through test points TP12 and TP34, respectively.

Figure 4-1 shows the J1, J2, and J3 standard banana supply connectors, and the jumpers J11, J34, and J35 configuration.

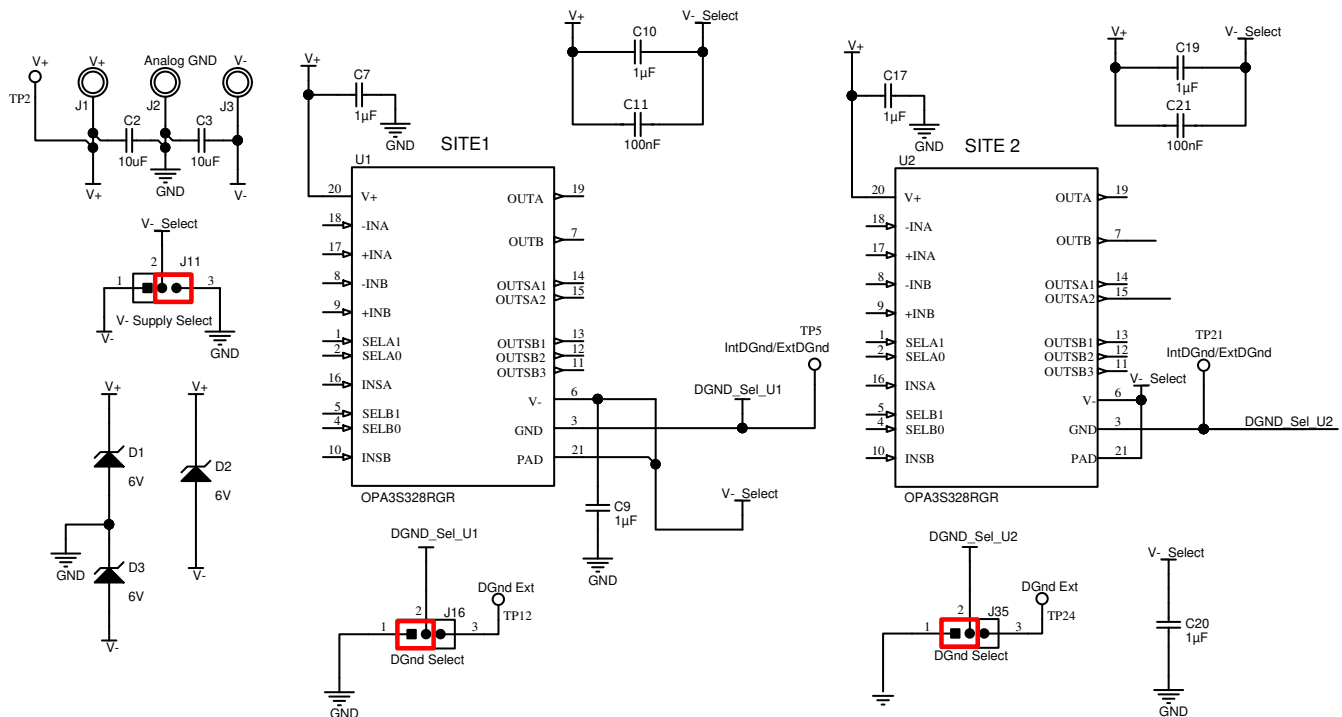


Figure 4-1. OPA3S328EVM Voltage Supply Connections

5 Input and Output Connections

Input signal connections for the OPA3S328EVM are provided through the use of SMA connectors and jumper headers. The output amplifier connections are provided through SMA connectors and test points. A simplified diagram of the OPA3S328EVM input and output connections is displayed in [Figure 2-1](#) and [Figure 2-2](#).

[Table 5-1](#) summarizes the input and output connectors and corresponding test points for site 1.

Table 5-1. OPA3S328EVM Site 1 Input and Output Connections

Designator	Signal	Connector Type	Description
J4	-INA	SMA	Inverting input, amplifier A
J9	D_BIAS	SMA (not populated)	Photodiode bias input, amplifier A
J7	+INA	SMA	Non-inverting input, amplifier A
J8	Output B	SMA	Output, amplifier B
TP4	OUTA/B3	Test Point	Output, amplifier A, unswitched
TP3	OUTSA1/B1	Test point	Output, amplifier A, switch A1
TP1	OUTSA2/B2	Test point	Output, amplifier A, switch A2
TP6	MUXOUT	Test point	Multiplexer switch B
TP11, TP17	Analog GND	Test point	Analog GND
TP12	DGND Ext	Test point	External digital GND bias

[Table 5-2](#) summarizes the input and output connectors and corresponding test points for site 2.

Table 5-2. OPA3S328EVM Site 2 Input and Output Connections

Designator	Signal	Connector Type	Description
J17	-INA	SMA	Inverting input, amplifier A
J19	D_BIAS	SMA (not populated)	Photodiode bias input, amplifier A
J22	+INA	SMA	Non-inverting input, amplifier A
J20	Output A	SMA	Output, amplifier A
J25	-INB	SMA	Inverting input, amplifier B
J27	D_BIAS	SMA (not populated)	Photodiode bias input, amplifier B
J33	+INB	SMA	Non-inverting input, amplifier B
J24	Output B	SMA	Output, amplifier B
TP19	OUTA	Test point	Output, amplifier A
TP16	OUTSA1	Test Point	Output, amplifier A, switch A1
TP13	OUTSA2	Test Point	Output, Amplifier A, switch A2
TP20	OUTB	Test Point	Output, amplifier B
TP25	OUTSB1	Test Point	Output, amplifier B, switch B1
TP23	OUTSB2	Test Point	Output, amplifier B, switch B2
TP22	OUTSB3	Test Point	Output, amplifier B, switch B3

Table 5-2. OPA3S328EVM Site 2 Input and Output Connections (continued)

Designator	Signal	Connector Type	Description
TP10, TP18	Analog GND	Test Point	Analog GND
TP24	DGND Ext	Test point	External digital GND bias

6 Modifications

By default, the OPA3S328EVM is populated with both devices set for transimpedance amplifier configurations. However, for flexibility, the PCB layout has additional unpopulated passive component footprints, and additional input connections. These additional component footprints in the layout allow the user to change the OPA3S328 circuit to other common configurations, such as programmable amplifier configurations. For a full schematic of the OPA3S328EVM, see [Figure 7-1](#) and [Figure 7-2](#).

7 Schematic, PCB Layout, and Bill of Materials

This section contains the schematic, bill of materials, and references for the OPA3S328EVM.

7.1 Schematic

Figure 7-1 and Figure 7-2 illustrate site 1 and site 2 of the OPA3S328EVM schematic.

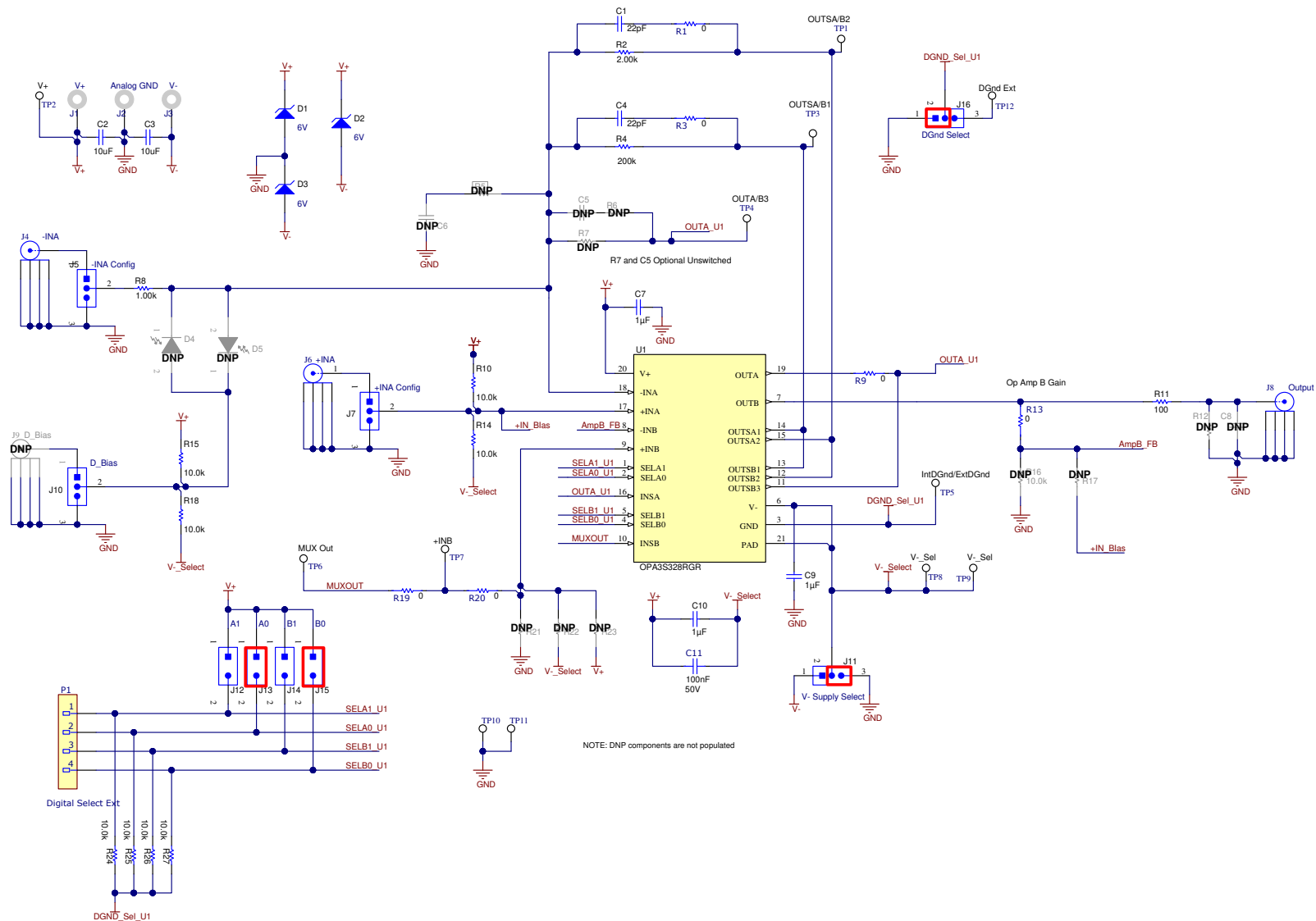


Figure 7-1. OPA3S328EVM Schematic - Site 1

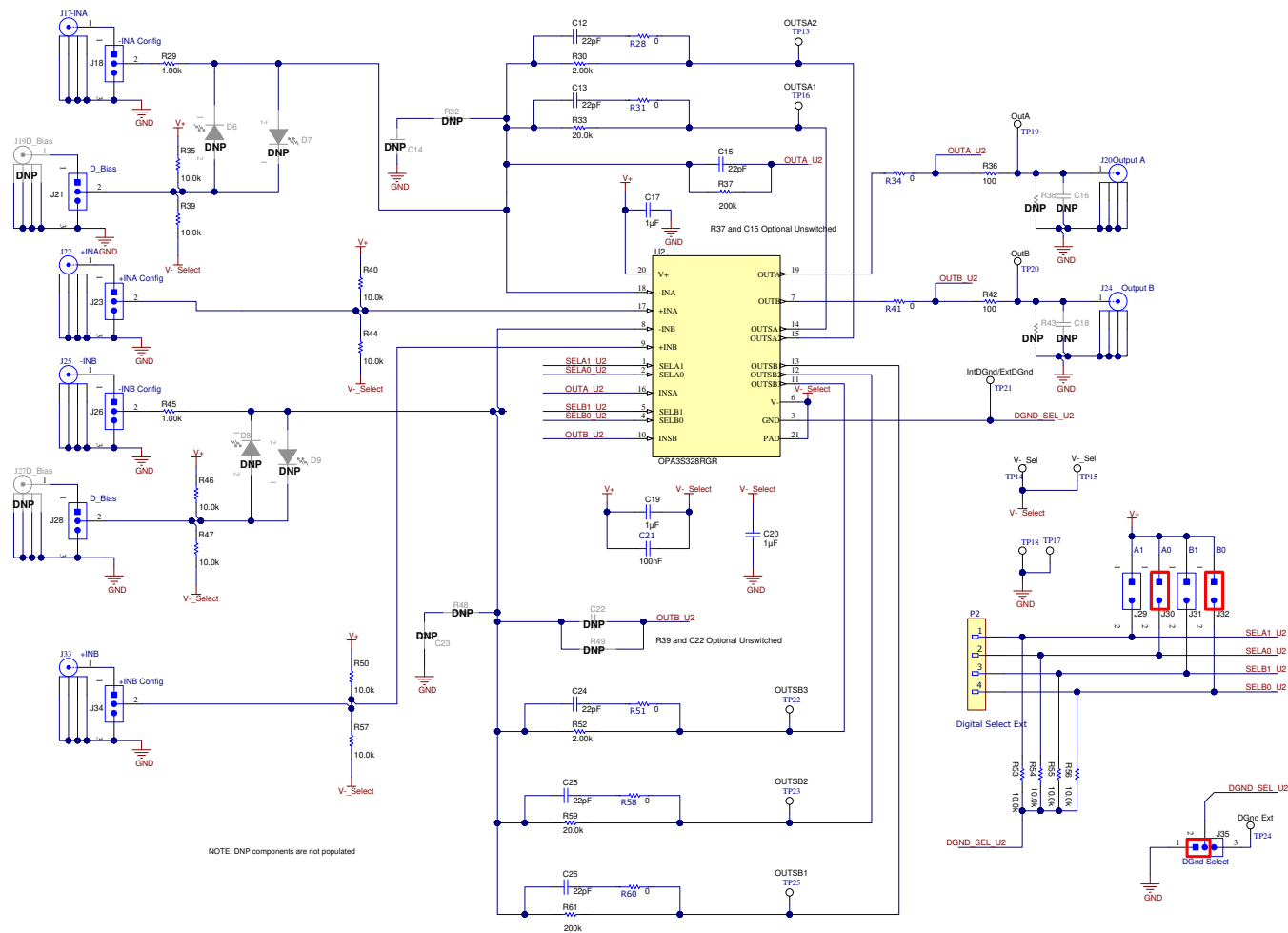


Figure 7-2. OPA3S328EVM Schematic - Site 2

7.2 PCB Layout

The OPA3S328EVM is a four-layer PCB design. Figure 7-3 to Figure 7-7 show the PCB layer illustrations. The top layer consists of all signal path traces, and is poured with a solid ground plane. Site 1 decoupling supply capacitors C7, C9, C10, and C11 are positioned on the top layer as close as possible to the power supply pins of device U1. Similarly, site 2 decoupling supply capacitors C17, C19, C20, and C21 are placed as close as possible to the power supply pins of the device U2. Selectable gain resistors and compensation capacitors are placed in close proximity to the inverting terminal of the corresponding operational amplifier forming a small feedback loop. The second internal layer is a dedicated solid GND plane. Independent vias to ground are placed at the ground connection of every component to provide a low-impedance, short path to ground. The third internal layer routes the power-supply connections. The bottom layer routes additional signal traces and the switch control signals.

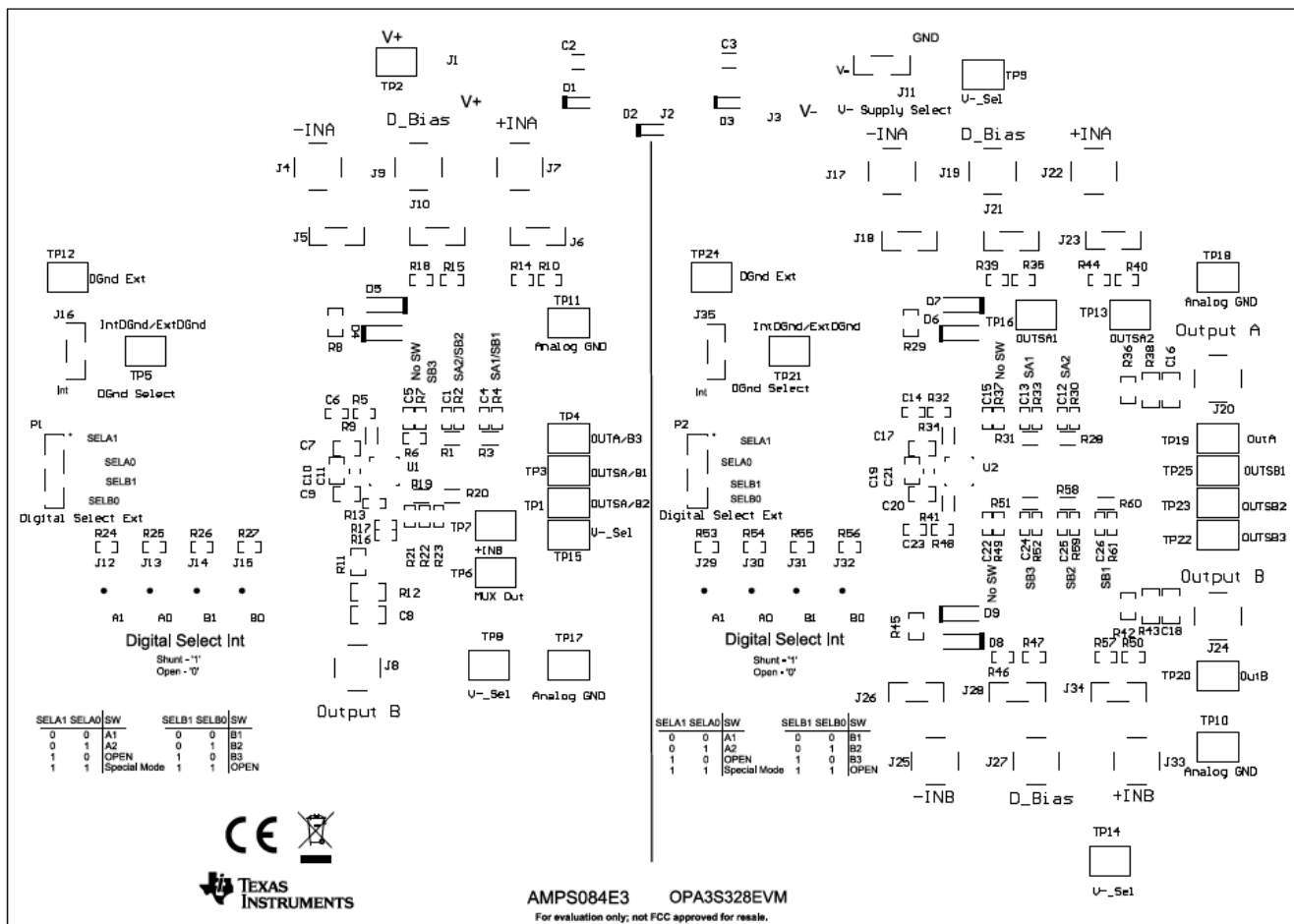


Figure 7-3. Top Overlay

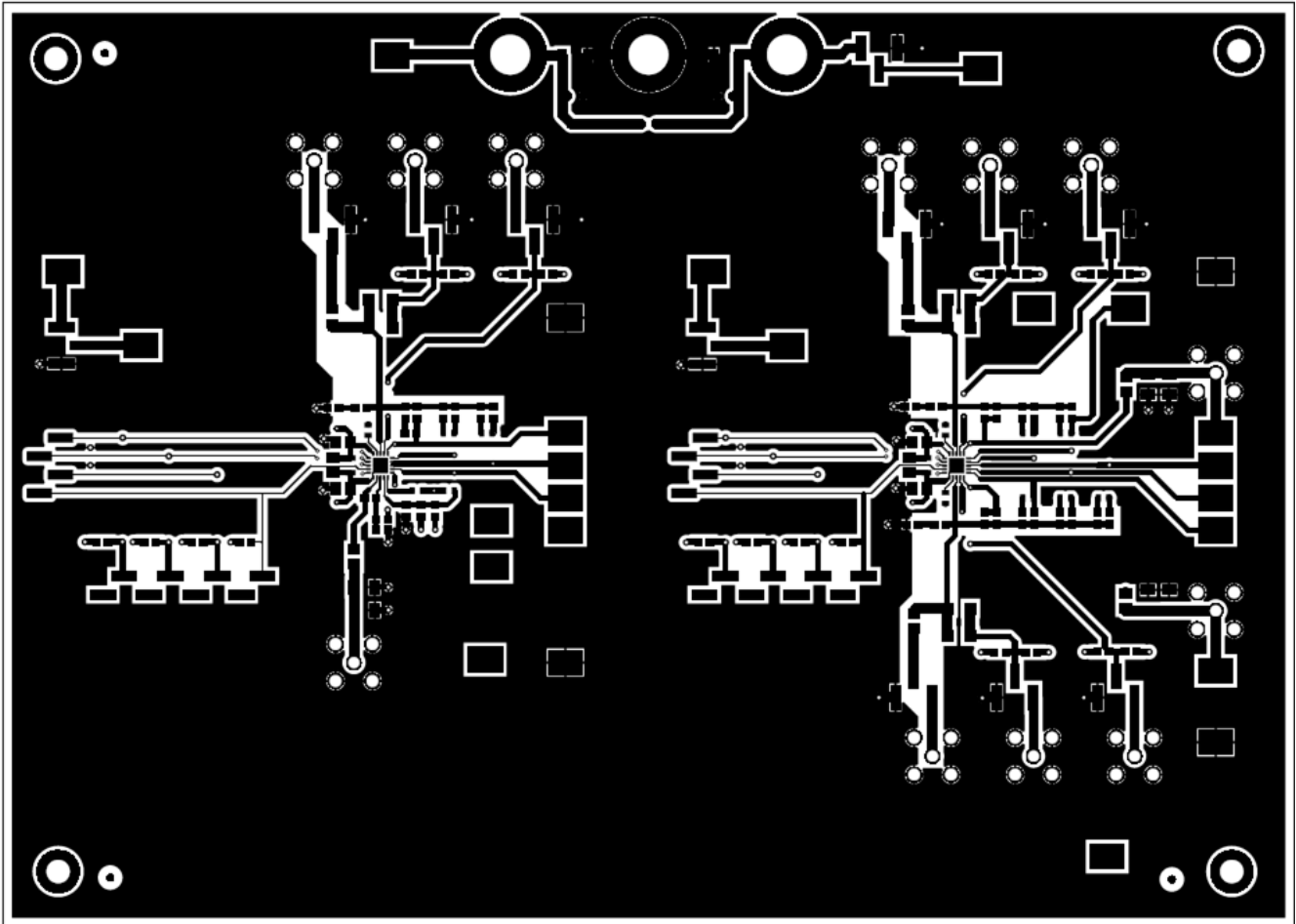


Figure 7-4. Top Layer PCB Layout

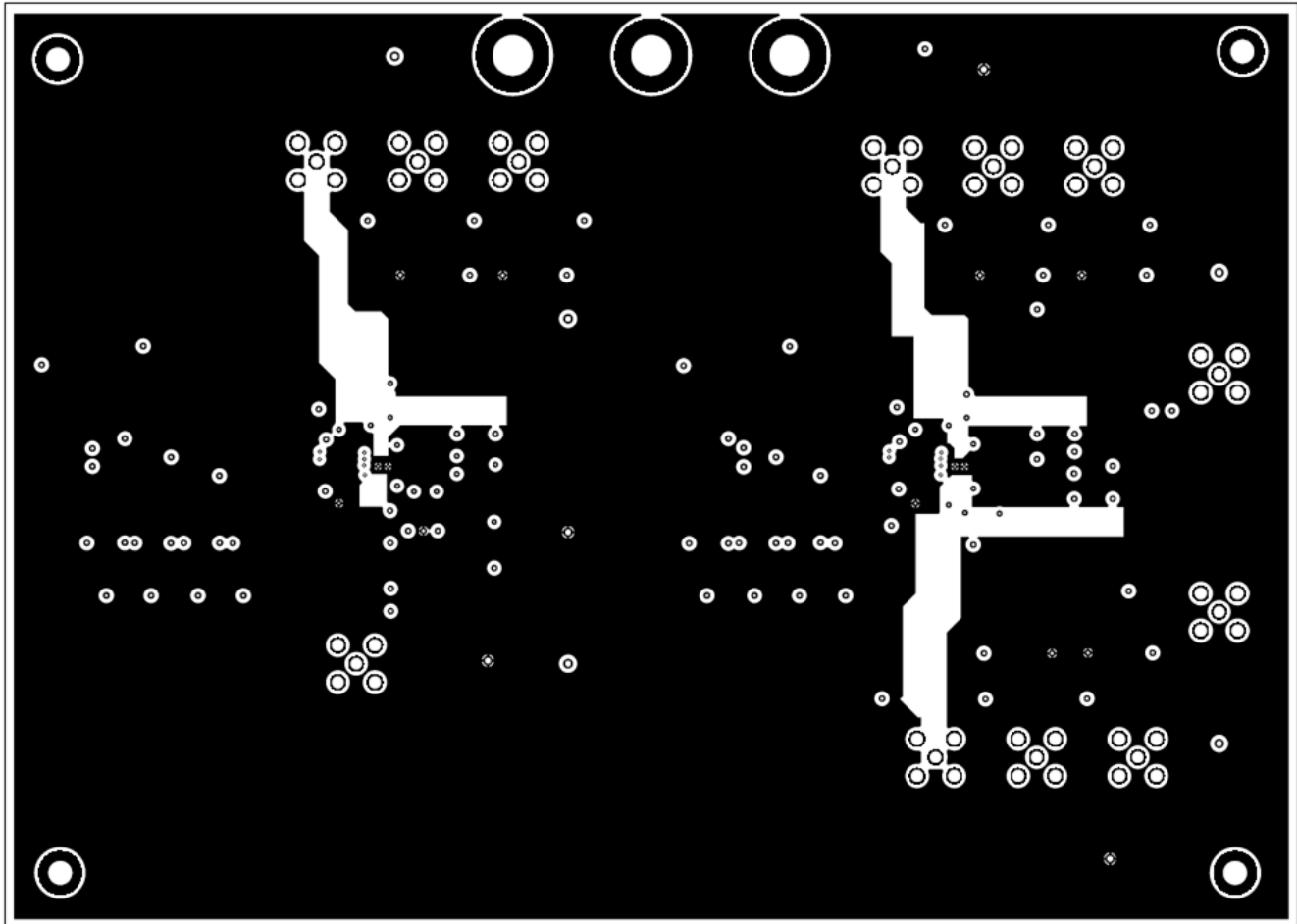


Figure 7-5. Ground Layer PCB Layout

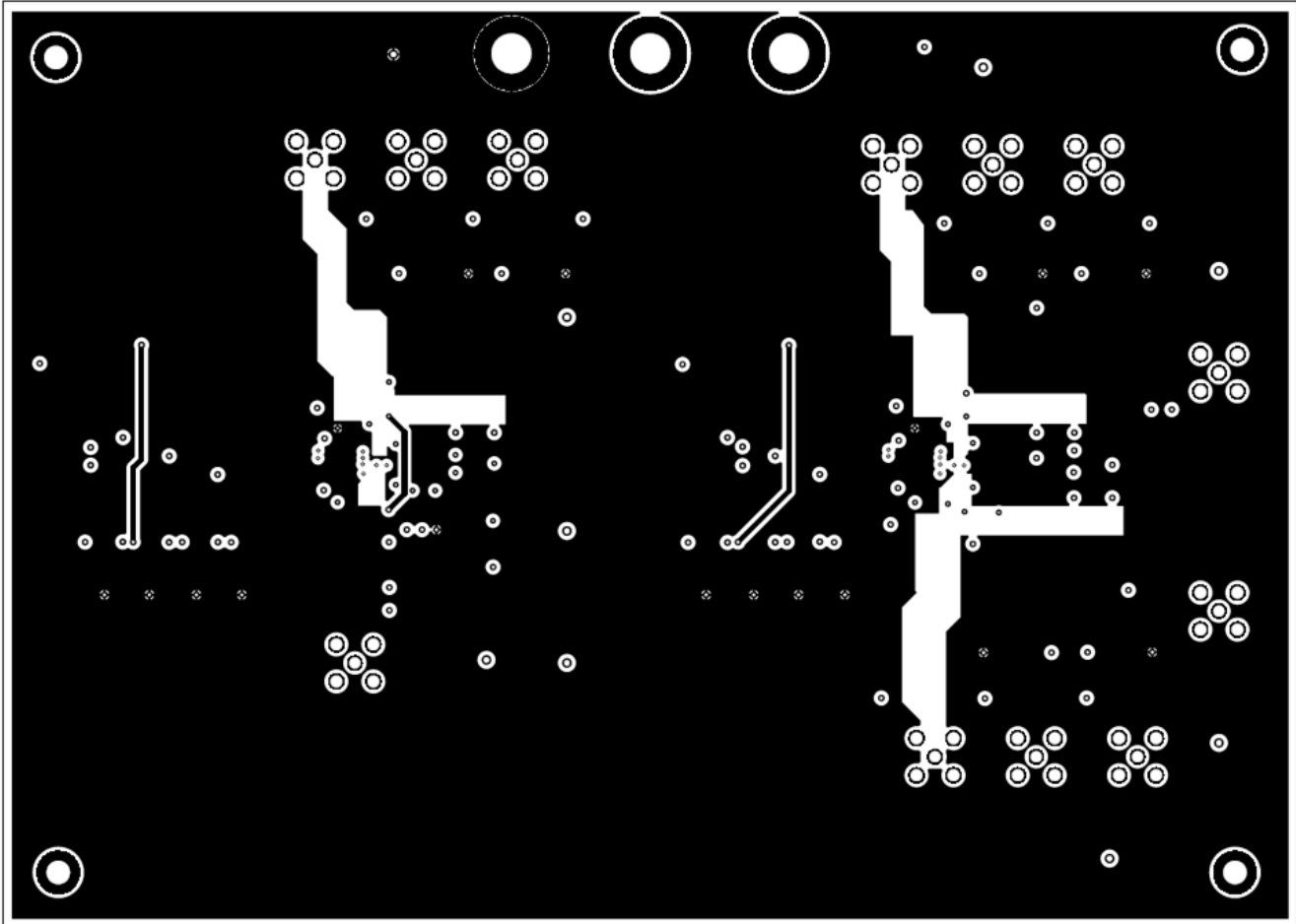


Figure 7-6. Power Layer PCB Layout

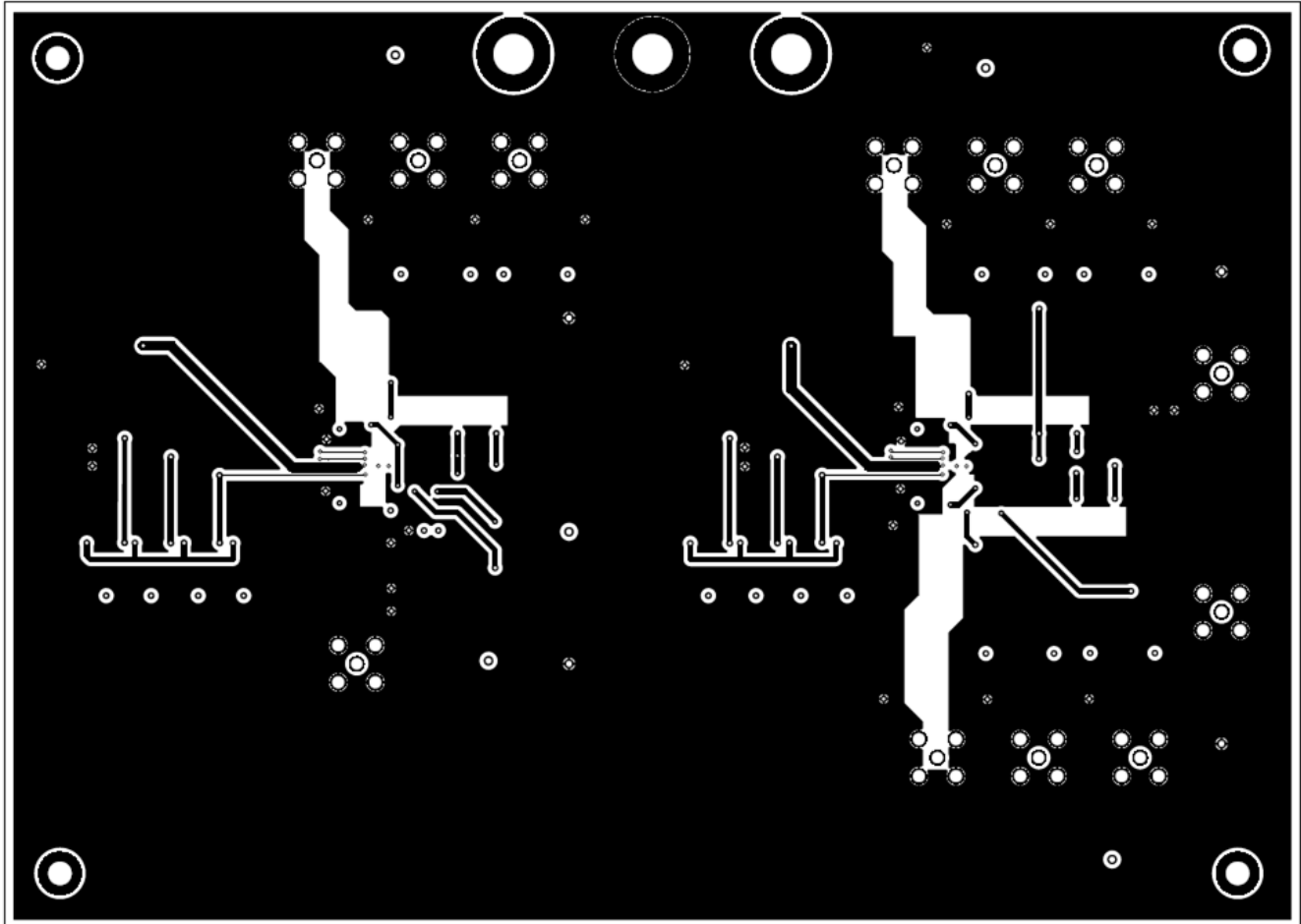


Figure 7-7. Bottom Layer PCB Layout

7.3 Bill of Materials

Table 7-1 lists the OPA3S328EVM bill of materials (BOM).

Table 7-1. OPA3S328EVM Bill of Materials

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS084	Any
C1, C4, C12, C13, C15, C24, C25, C26	8	22pF	CAP, CERM, 22 pF, 50 V, ±5%, C0G/NP0, 0603	0603	06035A220JAT2A	AVX
C2, C3	2	10uF	CAP, CERM, 10 uF, 25 V, ±20%, X7R, 1206_190	1206_190	C3216X7R1E106M160AE	TDK
C7, C9, C10, C17, C19, C20	6	1uF	CAP, CERM, 1 uF, 50 V, ±10%, X7R, 0805	0805	08055C105KAT2A	AVX
C11, C21	2	0.1µF	0.1µF ±10% 50V Ceramic Capacitor X7R 0805 (2012 Metric)	0805	GCE21BR71H104KA01L	Murata
D1, D2, D3	3	6V	Diode, Zener, 6 V, 200 mW, SOD-323	SOD-323	MMSZ5233BS-7-F	Diodes Inc.
H1, H2, H3, H4	4		MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4 inch	PMSSS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4			HEX STANDOFF 4-40 ALUMINUM 1/2 inch	2203	Keystone
J1, J2, J3	3		Standard Banana Jack, Uninsulated, 5.5mm	Keystone_575-4	575-4	Keystone
J4, J6, J8, J17, J20, J22, J24, J25, J33	9		SMA Straight PCB Socket Die Cast, 50 Ohm, TH	SMA Straight PCB Socket Die Cast, TH	5-1814832-1	TE Connectivity
J5, J7, J10, J11, J16, J18, J21, J23, J26, J28, J34, J35	12		Header, 100mil, 3x1, Gold, SMT	Samtec_TSM-103-01-X-SV	TSM-103-01-L-SV	Samtec
J12, J13, J14, J15, J29, J30, J31, J32	8		Header, 100mil, 2x1, Gold with Tin Tail, SMT	2x1 Header	TSM-102-01-L-SV	Samtec
P1, P2	2			HDR4	TSM-104-01-L-SV-P-TR	Samtec
R1, R3, R9, R13, R19, R20, R28, R31, R34, R41, R51, R58, R60	13	0 Ohms	0 Ohms Jumper 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	0603	ERJ-3GEY0R00V	Panasonic
R2, R30, R52	3	2.00k	RES, 2.00 k, 0.1%, 0.1 W, 0603	0603	RG1608P-202-B-T5	Susumu Co Ltd
R4, R37, R61	3	200k	RES, 200 k, 0.1%, 0.1 W, 0603	0603	RG1608P-204-B-T5	Susumu Co Ltd
R8, R29, R45	3	1.00k	RES, 1.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08051K00FKEA	Vishay-Dale

Table 7-1. OPA3S328EVM Bill of Materials (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
R10, R14, R15, R18, R24, R25, R26, R27, R35, R39, R40, R44, R46, R47, R50, R53, R54, R55, R56, R57	20	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RCG060310K0FKEA	Vishay Draloric
R11, R36, R42	3	100	RES, 100, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW0805100RFKEA	Vishay-Dale
R33, R59	2	20.0k	RES, 20.0 k, 0.1%, 0.1 W, 0603	0603	RG1608P-203-B-T5	Susumu Co Ltd
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7	7	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25	25		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone
U1, U2	2		40-MHz CMOS Operational Amplifier With Switches, RGR0020A (VQFN-20)	RGR0020A	OPA3S328RGR	Texas Instruments
C5, C6, C14, C22, C23	0	1000pF	CAP, CERM, 1000 pF, 50 V, ±5%, C0G/NP0, 0603	0603	C0603C102J5GACTU	Kemet
C8, C16, C18	0	0.1uF	CAP, CERM, 0.1 uF, 50 V, ±20%, X7R, 1206	1206	C1206C104M5RACTU	Kemet
D4, D5, D6, D7, D8, D9	0	820nm	High Speed PIN Photodiode, SMD	3.2x1.5mm	SFH 2701	OSRAM
J9, J19, J27	0		SMA Straight PCB Socket Die Cast, 50 Ohm, TH	SMA Straight PCB Socket Die Cast, TH	5-1814832-1	TE Connectivity
R5, R6, R7, R17, R21, R22, R23, R32, R48, R49	0	1.00k	RES, 1.00 k, 0.1%, 0.1 W, 0603	0603	RG1608P-102-B-T5	Susumu Co Ltd
R12, R38, R43	0	10.0k	RES, 10.0 k, 1%, 0.25 W, 1206	1206	CRCW120610K0FKEA	Vishay-Dale
R16	0	10.0k	RES, 10.0 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD0710KL	Yageo America

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated