PurePath Digital™ AUDIO SIX-CHANNEL PWM PROCESSOR

FEATURES

- Audio Input/Output
  - Automatic Master Clock Rate and Data Sample Rate Detection
  - Four Serial Audio Inputs (Eight Channels)
  - Support for 32-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz Sampling Rates
  - Data Formats: 16-, 20-, or 24-Bit Input Data; Left-Justified, Right-Justified, and I^2S
  - 64- or 48-f_S Bit-Clock Rate
  - 128-, 192-, 256-, 384-, and 512-f_S Master Clock Rates (Up to a Maximum of 50 MHz)
  - Six PWM Audio Output Channels
  - Any Output Channel Can be Mapped to Any Output Pin
  - Supports Single-Ended and Bridge-Tied Loads
  - I^2S Serial Audio Output
- Audio Processing
  - Volume Control Range of 48 dB to –100 dB
  - Master Volume Control from 24 dB to –100 dB in 0.5-dB Increments
  - Six Individual Channel Volume Controls With 24-dB to –100-dB Attenuation in 0.5-dB Increments
  - Serial Output Can Be Produced by Downmix of 5.1-Channel Input or Fourth Serial Input
  - 5.1-Channel Downmix to 2.1 or 3.1 PWM Output Speaker System
  - Integrated Bass Management
  - Two Programmable Biquads in Subwoofer Channel
  - Full Six-Channel Input and Output Mapping
  - Selectable DC Blocking Filters
- PWM Processing
  - 8× Oversampling With Fourth-Order Noise Shaping at 44.1, 48 kHz; 4× Oversampling at 88.2, 96 kHz; 2× Oversampling at 176.4, 192 kHz; and 12× Oversampling at 32 kHz
  - ≥105-dB Dynamic Range (TAS5086+TAS5186)
  - THD < 0.06% (TAS5086 Only)
  - 20-Hz–20-kHz Flat Noise Floor for 44.1-, 48-, 88.2-, 96-, 176.4- and 192-kHz Data Rates
  - Digital De-Emphasis for 32-kHz, 44.1-kHz and 48-kHz Data Rates
  - Intelligent AM Interference Avoidance System Provides Clear AM Reception
  - Optimized PWM Sequence for Click- and Popless Start and Stop
  - Optimized PWM Sequence for Charging of AC-Coupling Capacitors in Single-Ended Configurations
  - Adjustable Modulation Limit From 93.8% to 99.2%
- General Features
  - Automated Operation With Easy-to-Use Control Interface
  - I^2C Serial Control Slave Interface
  - Control Interface Operational Without MCLK
  - Single 3.3-V Power Supply
  - 38-Pin TSSOP Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The TAS5086 is a six-channel digital pulse-width modulator (PWM) that provides both advanced performance and a high level of system integration. The TAS5086 is designed to interface seamlessly with most audio digital signal processors and MPEG decoders, accepting a wide range of input data and clock formats.

The TAS5086 drives six channels of speakers in either single-ended or bridge-tied load configurations that accept a 1N + 1 interface format. The TAS5086 also supports 2N + 1 power stages with the use of some external logic (e.g., TAS5112). Stereo line out in I^2S format is available with either a pass-through signal (SDIN4) or an internal downmix.

The TAS5086 uses AD modulation operating at a 384-kHz switching rate for 32-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz data. The 8× oversampling, combined with the 4th-order noise shaper, provides a broad, flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

The TAS5086 is only an I^2C slave device, which always receives MCLK, SCLK, and LRCLK from other system components. The TAS5086 accepts clock rates of 128, 192, 256, 384, and 512 f_S. The TAS5086 accepts a 64-f_S master clock for 176.4-kHz and 192-kHz data.

The TAS5086 accepts a 64-f_S bit clock for all data rates. The TAS5086 also can accept a 48-f_S SCLK rate for MCLK ratios of 192 f_S and 384 f_S.

The TAS5086 is composed of five functional blocks.

- Power supply
- Clock, PLL, and serial data interface
- Serial control interface
- Device control
- PWM section

For detailed application information, see the *Using the PurePath Digital PWM Processor* application report (SLEA046).

Figure 1 shows the functional structure of the TAS5086.

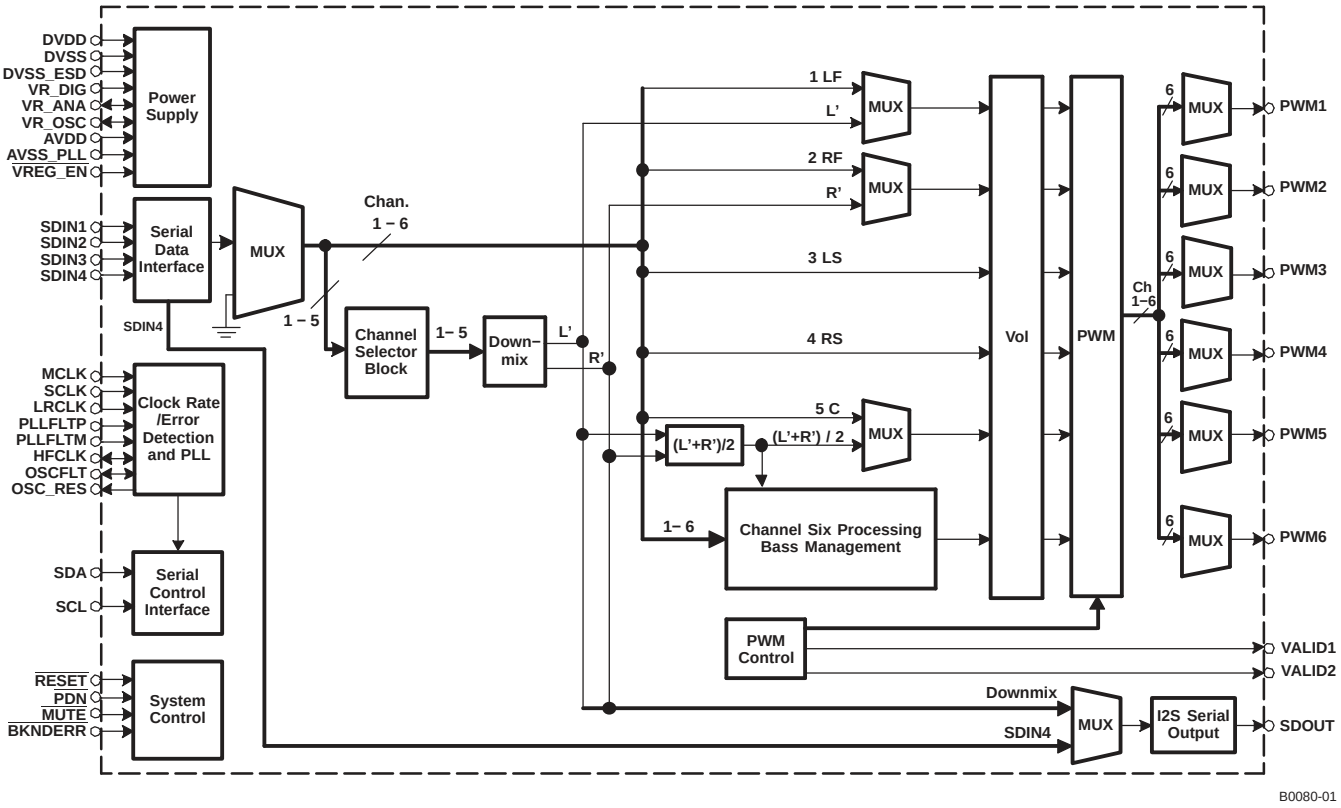


Figure 1. TAS5086 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

Supply voltage	DVDD and DVD_ESD	–0.3 V to 3.6 V
	AVDD	–0.3 V to 3.6 V
Input voltage	3.3-V-digital input	–0.5 V to DVDD + 0.5 V
	5-V-tolerant(2) digital input	–0.5 V to 6 V
Input clamp current, I_{IK} (V_I < 0 or V_I > 1.8 V)		±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > 1.8 V)		±20 mA
Operating free-air temperature		0°C to 70°C
Storage temperature range, T_{stg}		–65°C to 150°C

(1) Stresses beyond those listed under “absolute ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operation conditions” are not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are $\overline{\text{RESET}}$, $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$, SCLK, LRCLK, MCLK, SDA, and SCL.

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBT	817.16 mW	10.214 mW/C	357.5 mW	204.29 mW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Digital supply voltage	DVDD	3	3.3	3.6	V
	Analog supply voltage	AVDD	3	3.3	3.6	V
V_{IH}	High-level input voltage	3.3-V TTL, 5-V tolerant	2			V
V_{IL}	Low-level input voltage	3.3-V TTL, 5-V tolerant			0.8	V
T_A	Operating ambient-air temperature range		0	25	70	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	3.3-V TTL and 5-V(1) tolerant	I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage	3.3-V TTL and 5-V(1) tolerant	I_{OL} = 4 mA			0.5	V
I_{OZ}	High-impedance output current	3.3-V TTL				20	µA
I_{IL}	Low-level input current	3.3-V TTL	$V_I = V_{IL}$			1	µA
		5-V tolerant(2)	V_I = 0 V, DVDD = 3 V			1	
I_{IH}	High-level input current	3.3-V TTL	$V_I = V_{IH}$			1	µA
		5-V tolerant(2)	V_I = 5.5 V, DVDD = 3 V			20	
I_{DD}	Input supply current	Digital supply voltage, DVDD	f_S = 48 kHz		140		mA
			f_S = 96 kHz		150		
			f_S = 192 kHz		155		
			Power down		8		
		Analog supply voltage, AVDD	Normal		20		mA
			Power down		2		

(1) 5-V-tolerant outputs are SCL and SDA
(2) 5-V-tolerant inputs are SDA, SCL, $\overline{\text{RESET}}$, $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$, $\overline{\text{HP\_SEL}}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDIN3, and SDIN4.

Serial Audio Port

Serial audio port slave mode over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLKIN}	SCLK input frequency	C_L = 30 pF, SCLK = 64 f_S	2.048		12.288	MHz
t_{su1}	Setup time, LRCLK to SCLK rising edge		10			ns
t_{h1}	Hold time, LRCLK from SCLK rising edge		10			ns
t_{su2}	Setup time, SDIN to SCLK rising edge		10			ns
t_{h2}	Hold time, SDIN from SCLK rising edge		10			ns
	LRCLK frequency		32	48	192	kHz
	SCLK duty cycle		40%	50%	60%	
	LRCLK duty cycle		40%	50%	60%	
	SCLK rising edges between LRCLK rising edges		64		64	SCLK edges
	LRCLK clock edge with respect to the falling edge of SCLK		–1/4		1/4	SCLK period

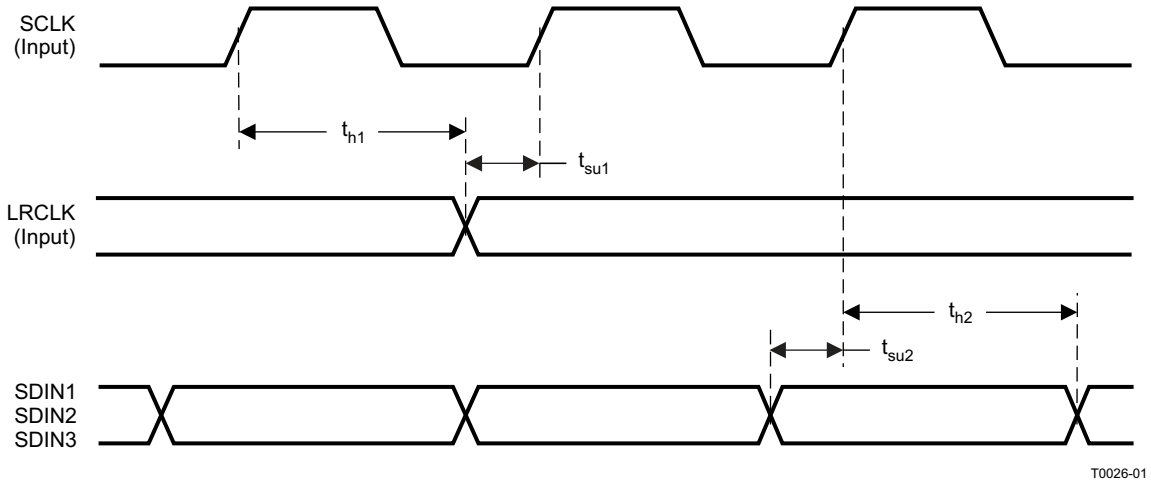


Figure 2. Slave Mode Serial Data Interface Timing

TAS5086 Pin-Related Characteristics of the SDA and SCL I/O Stages for F/S-Mode I²C-Bus Devices

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
V_{IL}	LOW-level input voltage		–0.5	0.3 V_{DD}	–0.5	0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}		0.7 V_{DD}		V
V_{hys}	Hysteresis of Schmitt-trigger inputs		N/A	N/A	0.05 V_{DD}		V
V_{OL1}	LOW-level output voltage (open drain or open collector)	3-mA sink current			0	0.4	V
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	Bus capacitance from 10 pF to 400 pF		250	7 + 0.1 C_b (1)	250	ns
t_{SP}	Pulse duration of spikes suppressed (2)		N/A	N/A	0	30	ns
I_i	Input current, each I/O pin		–30	30	–30 (3)	30 (3)	µA
C_i	Capacitance, each I/O pin			10		10	pF

(1) C_b = capacitance of one bus line in pF. The output fall time is faster than the standard I²C specification.
(2) SCL and SDA have a 30-ns glitch filter.
(3) The I/O pins of fast-mode devices must not obstruct the SDA and SDL lines if V_{DD} is switched off.

TAS5086 Bus-Related Characteristics of the SDA and SCL I/O Stages for F/S-Mode I²C-Bus Devices

All values are referred to V_{IHmin} and V_{ILmax} (see *TAS5086 Pin-Related Characteristics of the SDA and SCL I/O Stages for F/S-Mode I2C-Bus Devices*).

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{HD-STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4		0.6		µs
t_{LOW}	LOW period of the SCL clock		4.7		1.3		µs
t_{HIGH}	HIGH period of the SCL clock		4		0.6		µs
t_{SU-STA}	Setup time for repeated START		4.7		0.6		µs
t_{SU-DAT}	Data setup time		250		100		µs
t_{HD-DAT}	Data hold time (1)(2)		0	3.45	0	0.9	µs
t_r	Rise time of both SDA and SCL			1000	7 + 0.1 C_b (3)	500 (4)	ns
t_f	Fall time of both SDA and SCL			300	7 + 0.1 C_b (3)	300	ns
t_{SU-STO}	Setup time for STOP condition		4		0.6		µs
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		µs
C_b	Capacitive loads for each bus line			400		400	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)		0.1 V_{DD}		0.1 V_{DD}		V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)		0.2 V_{DD}		0.2 V_{DD}		V

(1) Note that SDA does not have the standard I²C specification 300-ns hold time and that SDA must be valid by the rising and falling edges of SCL. TI recommends that a 3.3-kΩ pullup resistor be used to avoid potential timing issues.
(2) A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU-DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r-max} + t_{SU-DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C bus specification) before the SCL line is released.
(3) C_b = total capacitance of one bus line in pF.
(4) Rise time varies with pullup resistor.

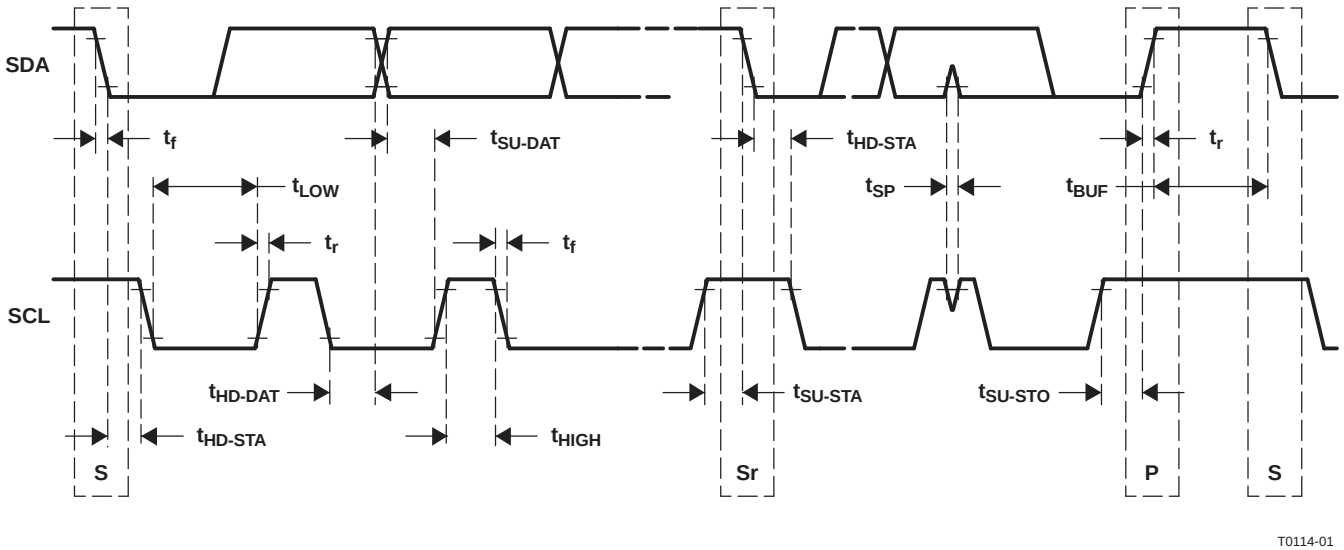


Figure 3. Start and Stop Conditions Timing Waveforms

Recommended I²C Pullup Resistors

It is recommended that the I²C pullup resistors R_P be 3.3 kΩ (see Figure 4). If a series resistor is in the circuit (see Figure 5), then the series resistor R_S should be less than or equal to 300 Ω.

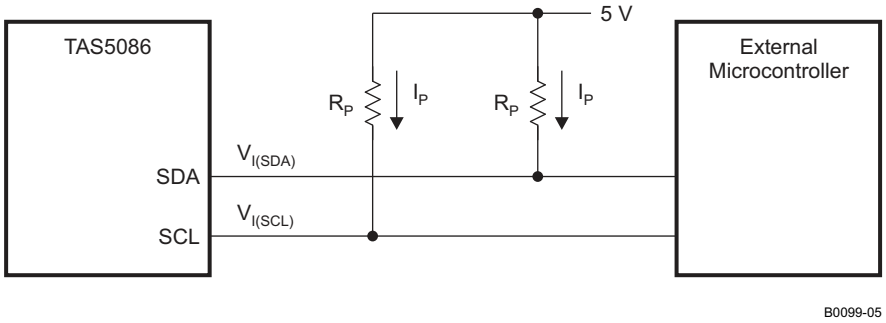
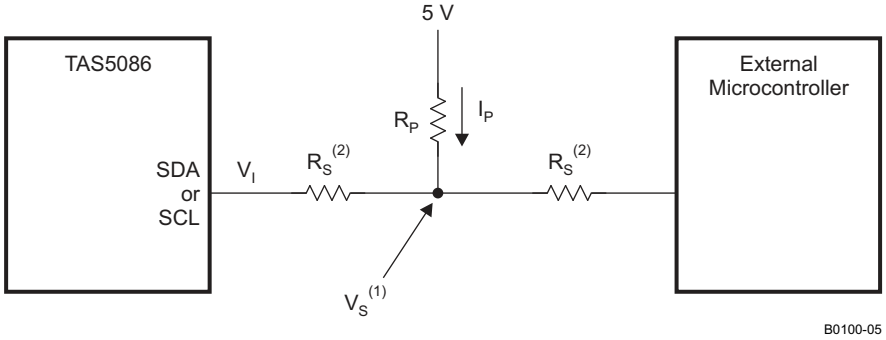


Figure 4. I²C Pullup Circuit (With No Series Resistor)



(1) $V_S = 5 \times R_S/(R_S + R_P)$. When driven low, $V_S << V_{IL}$ requirements.

(2) $R_S \leq 300\ \Omega$

Figure 5. I²C Pullup Circuit (With Series Resistor)

PHYSICAL CHARACTERISTICS

DBT PACKAGE
(TOP VIEW)

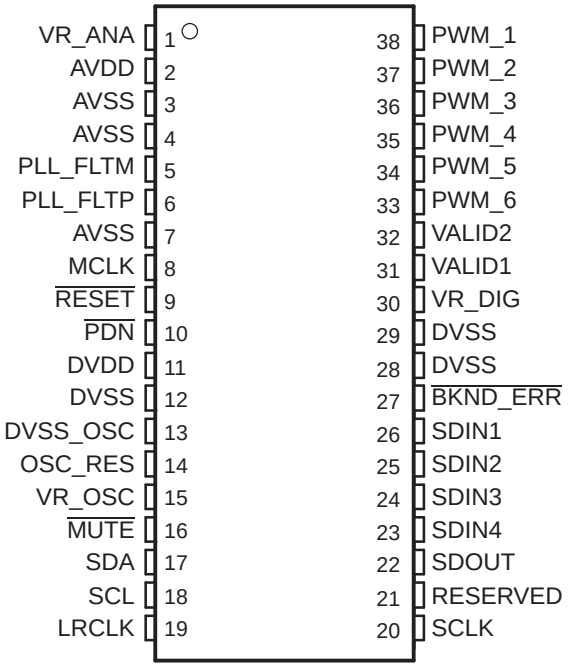


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Table 1. TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O(1)	5-V TOLERANT	TERMINATION(2)	DESCRIPTION
AVDD	2	P			3.3-V analog power supply
AVSS	3, 4, 7	P			Analog supply ground
BKND_ERR	27	DI		Pullup	Active-low. A back-end error sequence is generated by applying logic LOW to this terminal. BKND_ERR results in no change to any system parameters while VALID2 goes low.
DVDD	11	P			3.3-V digital power supply
DVSS	12, 28, 29	P			Digital ground
DVSS_OSC	13	P			Digital ground for oscillator
LRCLK	19	DI	5-V	Pulldown	Input serial audio data left/right clock (sampling rate clock)
MCLK	8	DI	5-V	Pulldown	MCLK is a 3.3-V clock master clock input. The input frequency of this clock can range from 4 MHz to 50 MHz.
MUTE	16	DI	5-V	Pullup	Performs a soft mute of outputs, active-low (muted signal = a logic low, normal operation = a logic high). The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume.
OSC_RES	14	AO			Oscillator trim resistor

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output
(2) All pullups are 20-μA *weak* pullups, and all pulldowns are 20-μA *weak* pulldowns. The pullups and pulldowns are included to ensure proper input logic levels if the terminals are left unconnected (pullups => logic 1 input; pulldowns => logic 0 input). Devices that drive inputs with pullups must be able to sink 20 μA while maintaining a logic-0 drive level. Devices that drive inputs with pulldowns must be able to source 20 μA while maintaining a logic-1 drive level.

Table 1. TERMINAL FUNCTIONS (continued)

TERMINAL NAME	TERMINAL NO.	I/O(1)	5-V TOLERANT	TERMINATION(2)	DESCRIPTION
$\overline{\text{PDN}}$	10	DI	5-V	Pullup	Power down, active-low. $\overline{\text{PDN}}$ powers down all logic, stops all clocks, and performs a soft stop whenever a logic low is applied. The internal parameters are preserved through a power-down cycle, as long as $\overline{\text{RESET}}$ is not active. The duration for system recovery from power down is 100 ms. When released, $\overline{\text{PDN}}$ powers up all logic, starts all clocks, and performs a soft start that returns to the previous configuration.
PLL_FLTM	5	AO			PLL negative input
PLL_FLTP	6	AI			PLL positive input
PWM_ 1	38	DO			PWM 1 output
PWM_ 2	37	DO			PWM 2 output
PWM_ 3	36	DO			PWM 3 output
PWM_ 4	35	DO			PWM 4 output
PWM_ 5	34	DO			PWM 5 output
PWM_ 6	33	DO			PWM 6 output
RESERVED	21	–			RESERVED (connect to ground)
$\overline{\text{RESET}}$	9	DI	5-V	Pullup	A system reset is generated by applying a logic low to this terminal. $\overline{\text{RESET}}$ is an asynchronous control signal that restores the TAS5086 to its default conditions, sets the VALID2 output low, and places the PWM in the hard-mute (M) state. Master volume is immediately set to full attenuation. On the release of $\overline{\text{RESET}}$, if $\overline{\text{PDN}}$ is high, the system performs a 4–5-ms device initialization and sets the volume at mute.
SCL	18	DI	5-V		I^2C serial control clock input
SCLK	20	DI	5-V	Pulldown	Serial audio data clock (shift clock). SCLKIN is the serial audio port (SAP) input data bit clock.
SDA	17	DIO	5-V		I^2C serial control data interface input/output
SDIN1	26	DI		Pulldown	Serial audio data 1 input is one of the serial data input ports. SDIN1 supports four discrete (stereo) data formats.
SDIN2	25	DI		Pulldown	Serial audio data 2 input is one of the serial data input ports. SDIN2 supports four discrete (stereo) data formats.
SDIN3	24	DI		Pulldown	Serial audio data 3 input is one of the serial data input ports. SDIN3 supports four discrete (stereo) data formats.
SDIN4	23	DI		Pulldown	Serial audio data 4 input is one of the serial data input ports. SDIN4 supports four discrete (stereo) data formats.
SDOUT	22	DI			Serial audio data 1 output is the only serial data output port. SDOUT supports I^2S format only.
VALID1	31	DO			Soft start valid. Output indicating validity of soft-start PWM output, active-high
VALID2	32	DO			Output indicating validity of PWM outputs, active-high.
VR_ANA	1	P			Voltage reference for analog supply, 1.8 V. A pinout of the internally regulated 1.8-V power. A 0.1-µF, low-ESR capacitor should be connected between this terminal and AVSS_PLL. This terminal must not be used to power external devices.
VR_DIG	30	P			Voltage reference for digital PWM core supply, 1.8 V. A pinout of the internally regulated 1.8-V power used by digital PWM core logic. A 0.1-µF, low-ESR(3) capacitor should be connected between this terminal and DVSS_PWM. This terminal must not be used to power external devices.
VR_OSC	15	P			Voltage reference for analog supply, 1.8 V. A pinout of the internally regulated 1.8-V power. A 0.1-µF, low-ESR(3) capacitor should be connected between this terminal and AVSS_PLL. This terminal must not be used to power external devices.

(3) If desired, low-ESR capacitance values can be implemented by paralleling two or more ceramic capacitors of equal value. Paralleling capacitors of equal value provides an extended high-frequency supply decoupling. This approach avoids the potential of producing parallel resonance circuits that have been observed when paralleling capacitors of different values.

DETAILED DESCRIPTION

POWER SUPPLY

The TAS5086 power-supply section contains regulators that provide analog and digital regulated power for various sections of the TAS5086. The analog supply supports the analog PLL while digital supplies support the digital PLL, the digital audio processor, the pulse width modulator, and the output control (reclocker). The power-supply section is enabled via $\overline{\text{VREG\_EN}}$.

CLOCK, ERROR RATE DETECTION, AND PLL

This module provides the timing and serial data interface for the TAS5086.

The TAS5086 is a clock slave device. It accepts MCLK, SCLK, and LRCLK.

The TAS5086 supports 64-f_S MCLK for the 176.4-kHz and 192-kHz data rates.

The TAS5086 accepts a 64-f_S SCLK rate for all MCLK ratios and a 48-f_S SCLK rate for MCLK ratios of 192 f_S and 384 f_S.

TAS5086 checks to verify that SCLK is a specific value of 64 f_S or 48 f_S.

The TAS5086 supports a 1-f_S LRCLK.

The timing relationship of these clocks to SDIN[1:4] and SDOUT is shown in subsequent sections.

The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable or absent) to produce a 196-MHz PLL output.

The TAS5086 can auto-detect and set the internal clock control logic to the appropriate settings for the frequencies of 32 kHz, normal speed (44.1 or 48 kHz), double speed (88.2 kHz or 96 kHz), and quad speed (176.4 kHz or 192 kHz). The automatic sample rate detection can be disabled and the values set via I^2C.

The TAS5086 also supports an AM interference-avoidance mode during which the clock rate is adjusted, in concert with the PWM sample rate converter, to produce a PWM output at 7-f_S, 8-f_S, or 9-f_S.

The sample rate must be set manually during AM interference avoidance and when de-emphasis is enabled.

The TAS5086 uses an internal oscillator time base to provide reference timing information for the following functions:

- MCLK, SCLK, and LRCLK error detection
- I^2C communication when power is first applied to the device
- Automatic data-rate detection and setting (32 kHz, normal, double, and quad speed)
- Automatic MCLK rate detection and setting (64, 128, 192, 256, 384, and 512 f_S)

OSCILLATOR TRIM

The TAS5086 PWM processor contains an internal oscillator for PLL reference. This reduces system cost because an external reference is not required. After each power up or reset, a oscillator trim is needed; see the *Oscillator Trim Register (0x1B)* section for a detailed procedure.

SERIAL DATA INTERFACE

Serial data is input on SDIN1, SDIN2, SDIN3, and SDIN4. The PWM outputs and downmix are derived from SDIN1, SDIN2, and SDIN3. SDIN4 is a selectable pass-through signal that is available at SDOUT as an I²S output. The TAS5086 accepts 32-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz serial data in 16-, 20-, or 24-bit, left-justified, right-justified, and I²S serial data formats.

Serial data is output on SDOUT. The SDOUT data format is I²S 24-bit at the same data rate as the input. The SDOUT output is synchronized to use the SCLK and LRCLK signals. There is a 1- to 2.5-LRCLK frame delay from the input data to the output data, depending on the input serial data format. The SDOUT output has no I²C-controllable functions. It is always operational.

The parameters of this clock and serial data interface input format are I²C configurable.

I²C SERIAL CONTROL INTERFACE

The TAS5086 has an I²C serial control slave interface to receive commands from a system controller. The serial control interface supports both normal-speed (100-kHz) and high-speed (400-kHz) operations without wait states. As an added feature, this interface operates even if MCLK is absent.

The serial control interface supports both single-byte and multi-byte read and write operations for status registers and the general control registers associated with the PWM.

The I²C interface supports a special mode that permits I²C write operations to be broken up into multiple-data write operations that are multiples of 4 data bytes. These are 6-, 10-, 14-, 18-, ... etc., -byte write operations that are composed of a device address, read/write bit, subaddress, and any multiple of 4 bytes of data. This permits the system to write large register values incrementally without blocking other I²C transactions.

Figure 6 shows the data flow and control through the TAS5086. The major I²C registers are shown above each applicable block (e.g., 0x04 is the serial data format control register).

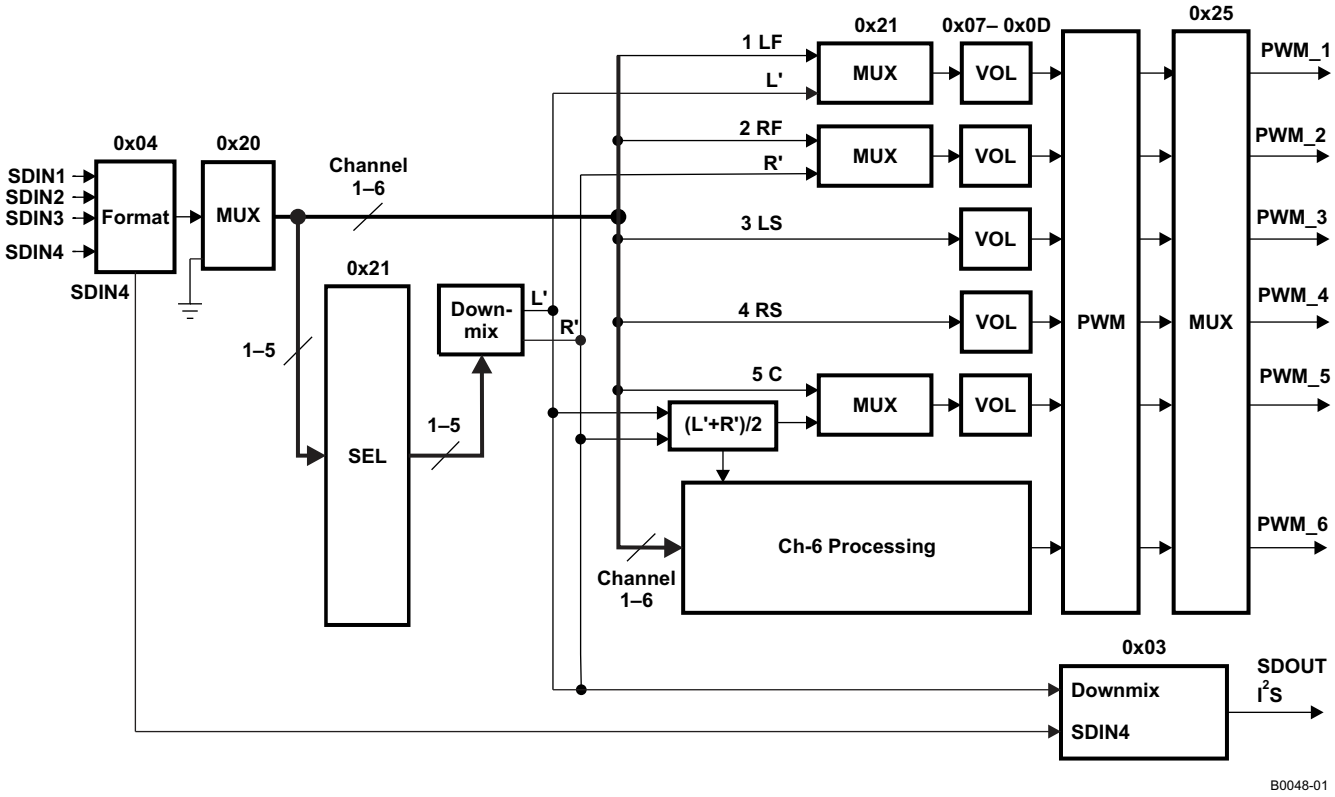


Figure 6. TAS5086 Data Flow Diagram With I²C Registers

Channel-6 Processing Section

Channel 6 has processing features that are directly applicable to the subwoofer channel.

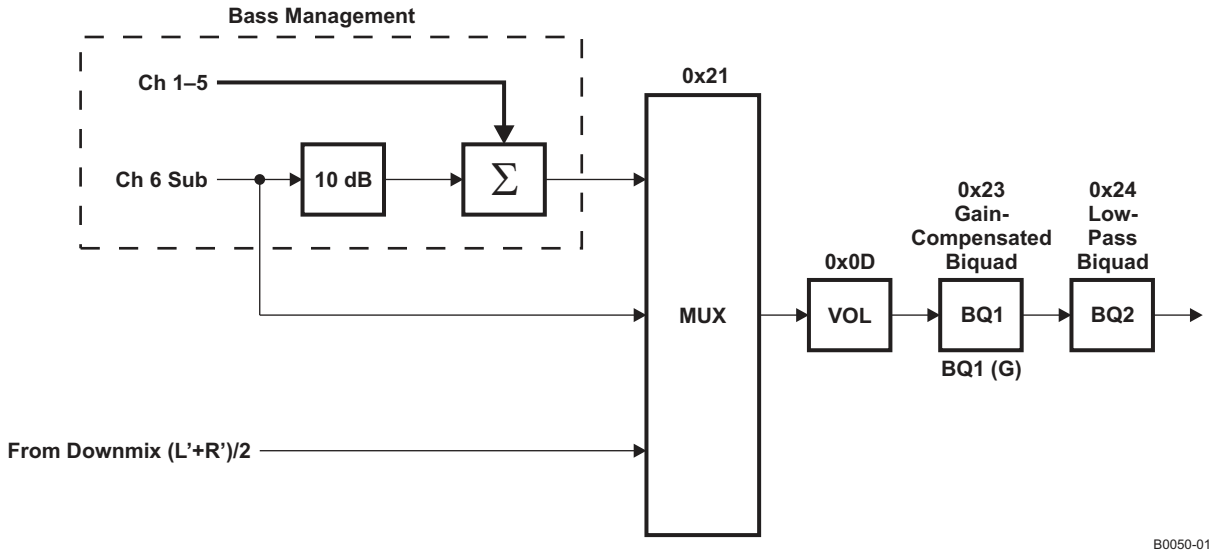


Figure 7. Channel-6 Processing Block Diagram

PWM Section

The TAS5086 has six channels of high-performance digital PWM modulators that are designed to drive switching output stages (back ends) in both single-ended (SE) and H-bridge (bridge-tied load) configurations. The TAS5086 device uses noise-shaping and sophisticated error correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The TAS5086 uses a fourth-order noise shaper to provide >105-dB SNR performance from 20 Hz to 20 kHz.

The TAS5086 PWM interface is described by using the following notation:

PN + V

where

P = number of PWM signals per channel

N = number of channels

V = total number of valid signals used to reset the power stage

For example, the TAS5086 initial interface format means that there is 1 PWM signal per channel (N = 6) and 1 valid signal is used to reset the power stages. The shorthand notation to describe this is 1N+1.

The PWM section accepts 24-bit PCM data from the serial data interface and outputs six PWM audio output channels to drive 1N+1 single-ended and BTL power stages.

The PWM interface supports:

- TAS5186 in BTL or SE mode without any external glue logic, uses 1N+1 signaling.
- TAS5142 in BTL or SE mode without any external glue logic, uses 1N+1 signaling.
- TAS5111 SE without any external glue logic, and with a pulldown on the output, uses 1N+1 signaling.
- TAS5111 BTL or TAS5112 BTL with one inverter per BTL channel of glue logic and a pulldown on the output, uses 1N+1 signaling from TAS5086, 2N+1 input to TAS5111/12.
- TAS5112 SE (with external glue logic)

See the application schematics for an example of the TAS5086 with the TAS5186 and the TAS5086 with TAS5112 SE and TAS5111 SE.

The TAS5086 has input multiplexers that allow any of the input channels to be routed to any PWM channel and output multiplexers to enable any PWM output to be routed to any PWM output pin.

It also has individual channel dc-blocking filters that are enabled by default.

Individual channel de-emphasis filters for 32, 44.1, and 48 kHz are included and can be enabled and disabled.

There is also a two-channel downmix result that can be output on SDOUT (I^2S format). This result also can be sent to the left and right front channels (channels 1 and 2) and/or to the center and subwoofer (channels 5 and 6) as well.

A mixer on the subwoofer channel supports bass management configuration 1.

PWM output characteristics

- Up to 8× oversampling
- 12× at f_S = 32 kHz, 8× at f_S = 48 kHz, 4× at f_S = 96 kHz, 2× at f_S = 192 kHz
- Fourth-order noise shaping
- ≥105-dB dynamic range, 0–20 kHz (TAS5086 + TAS5186 system measured at speaker terminals)
- THD < 0.06% (measured at TAS5086 outputs)
- Adjustable maximum modulation limit of 93.8% to 99.2%

Transitions Between Shutdown and Playing

The TAS5086 outputs are switching all the time with the noise shaper active. Mute is acheived by inputting a zero into the noise shaper, with the noise shaper running and the output still switching. By using this approach, the transitions between off and operation is avoided. The only exception is shutdown of surround channels as described in the *Surround Register (0x19)* section.

Futhermore, the TAS5086 is designed to drive a load in single-ended and bridge-tied-load configurations. The *principle* in the SE and BTL configurations is shown in Figure 8 and Figure 9. In both situations, care must be taken to ensure correct start-up sequences which charge the bootstrap capacitor and do not produce audible artifacts; the TAS5086 is designed to do that.

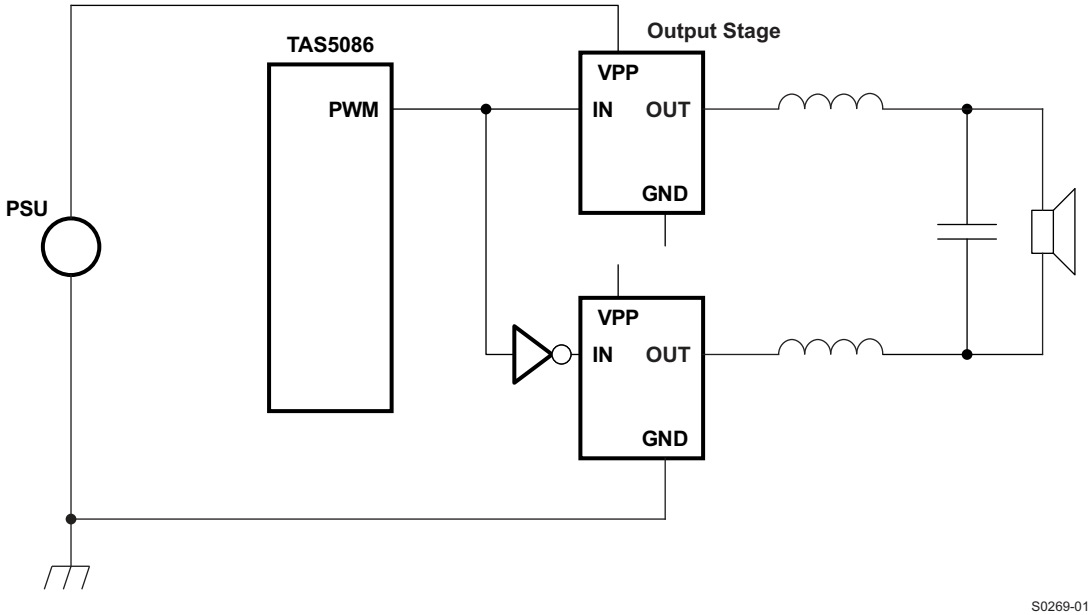


Figure 8. BTL Filter Configuration

The SE configuration presents an additional challenge in order for starting up quietly. The second terminal of the loudspeaker is connected to a split capacitor between power and ground. The advantage of this circuitly is that it provides some degree of power-supply ripple rejection. The problem related to the split capacitor is that the voltage over it must be controlled when the modulator starts (i.e., when the power stage output goes out of high impedance state) to avoid a click in the speaker.

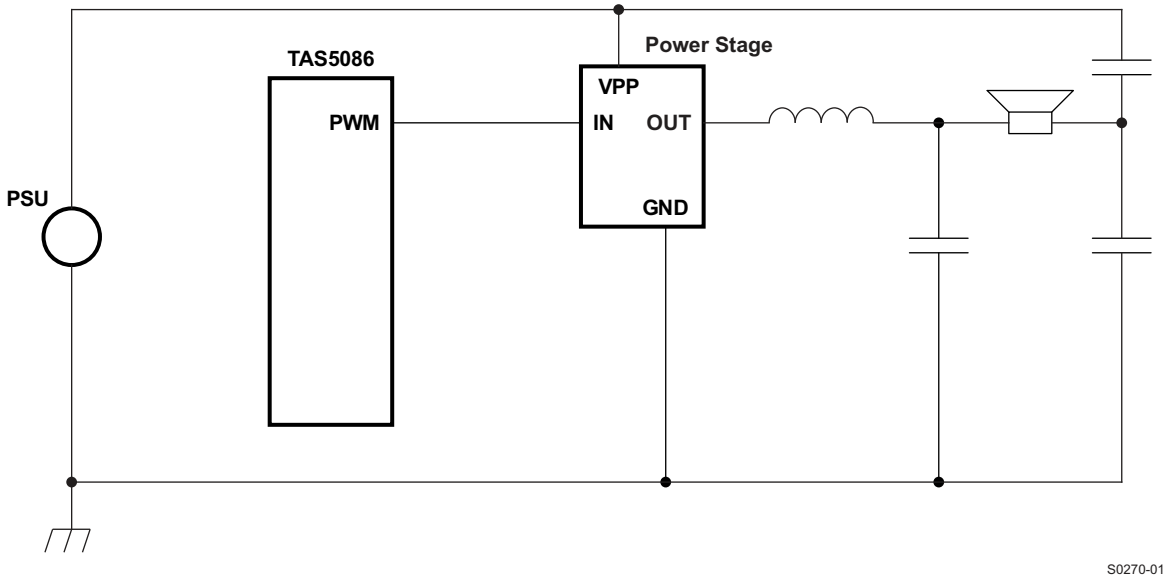


Figure 9. SE Filter Configuration

The TAS5086 supports two mechanisms for controlling the split-capacitor midpoint.

In the extra half-bridge scheme (the TAS5186 power stage is an example of this) an additional half-bridge is started and brought to a 50-percent duty cycle, i.e., a situation where the average voltage of the half-bridge is equal to the voltage which must be applied to the split-capacitor midpoint to start up without clicks in the speaker. A resistor per channel is connected between the extra half-bridge and each midpoint for the split capacitors. The split capacitors are charged through this resistor. This approach requires an extra VALID pin on the modulator to control the extra half-bridge, therefore the 1N+2 interface. Figure 10 shows the topology of the extra half-bridge. In some situations, a channel configured in BTL can be used to charge the split capacitor instead of the extra half-bridge. This is shown in Figure 11.

The mid-Z scheme charges the split capacitor through the loudspeaker. In order to do this without audible artifacts the charge current must be limited. This is done by applying a start sequence which charges the output state between low, high and high-Z. Because the ouput stage is in high-Z in a part of the sequence, the resulting output impedance can be brought to a level suitable for charging the split capacitors without audible artifacts. This solution does not require external components, as shown in Figure 9. Not all power stages are compatible with the mid-Z scheme, double-check the power-stage data sheet for compabitility. The PWM start register (0x18) programs the TAS5086 for mid-Z or the standard low-Z start sequence.

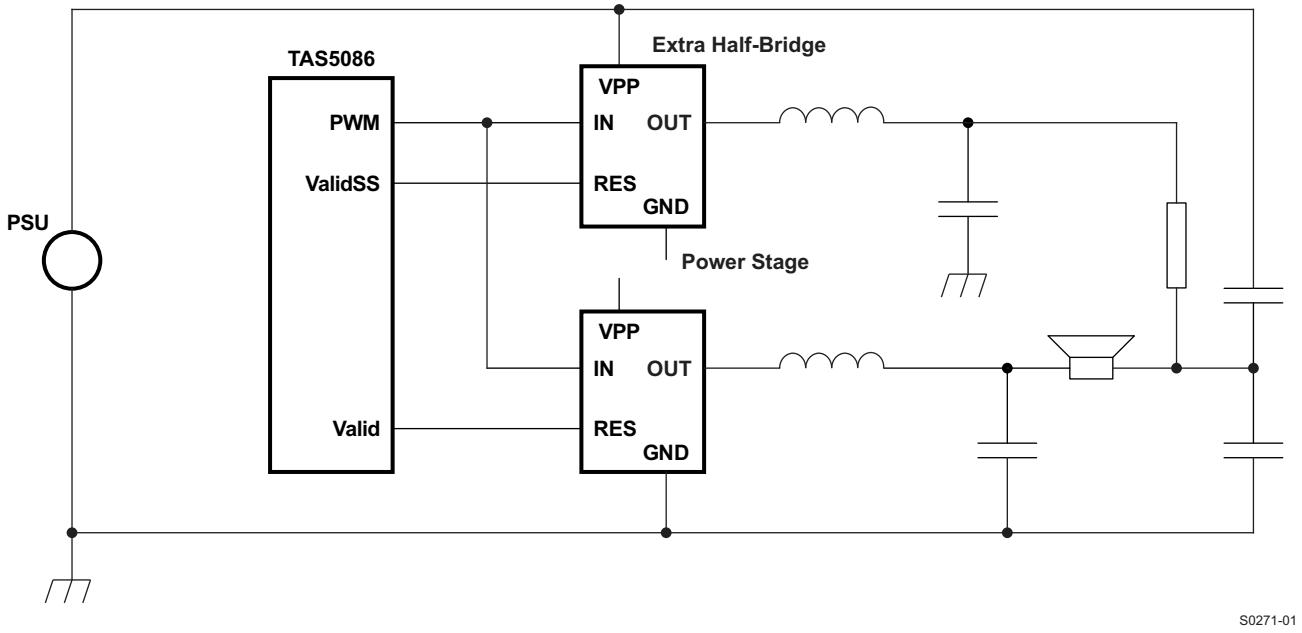


Figure 10. Split-Capacitor Charging With Extra Half-Bridge

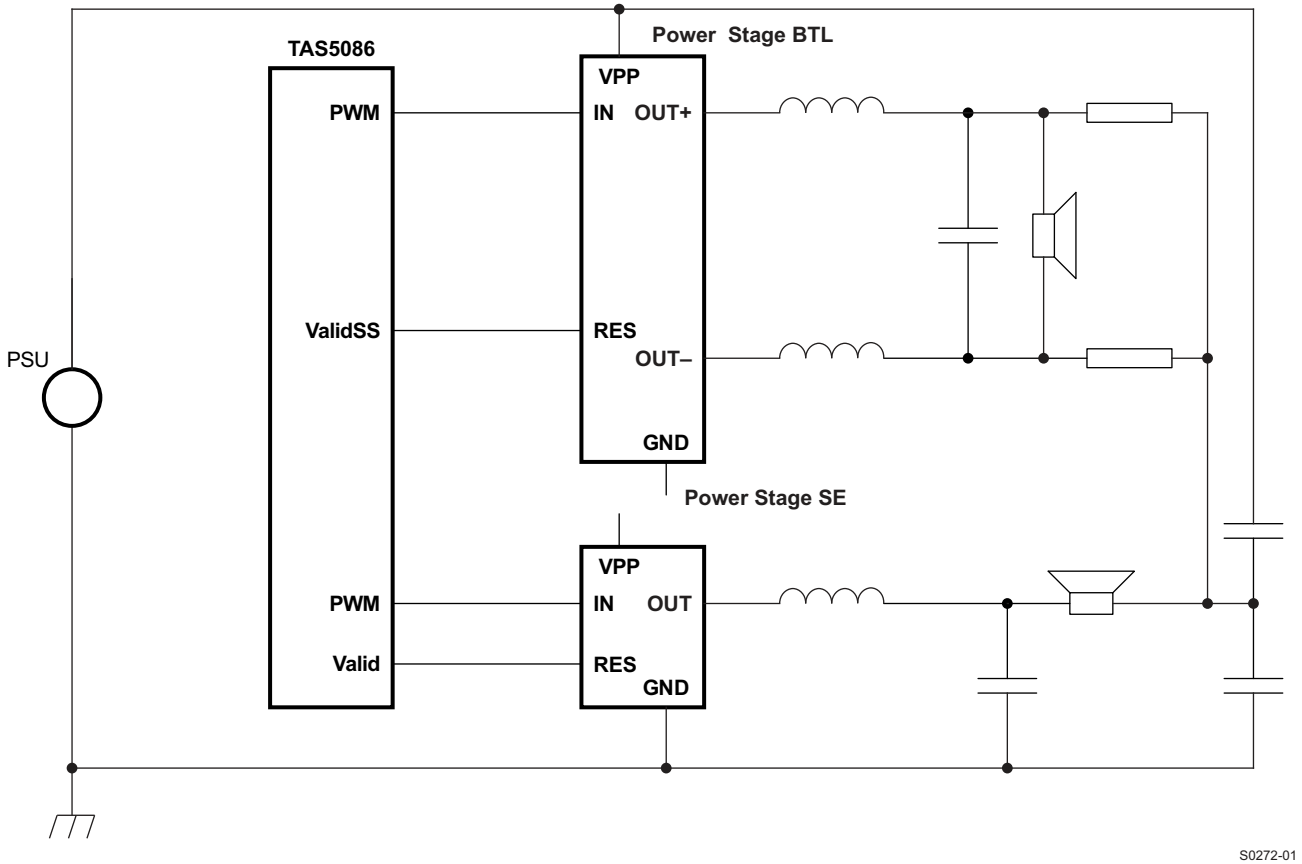
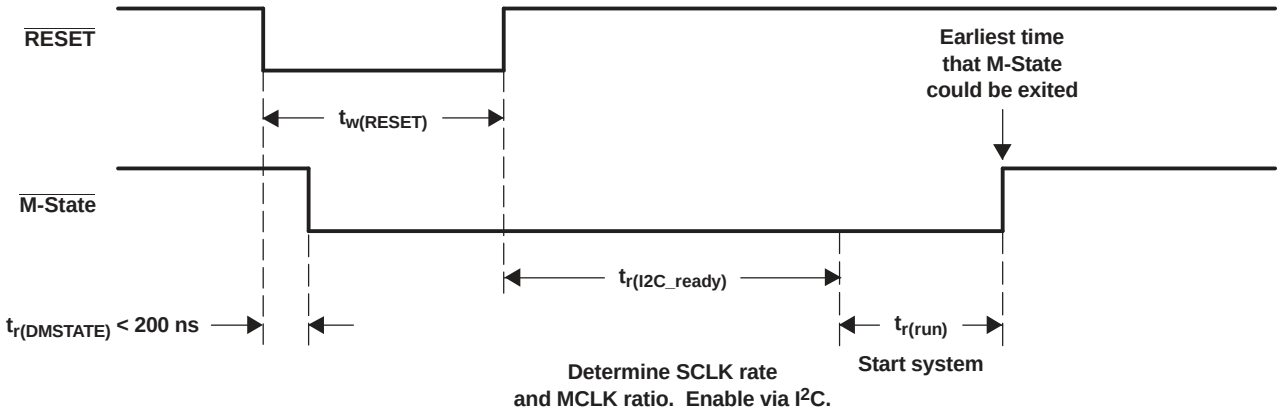


Figure 11. Split-Capacitor Charging With BTL Subwoofer

Reset Timing ($\overline{\text{RESET}}$)

Control-signal parameters over recommended operating conditions (unless otherwise noted)



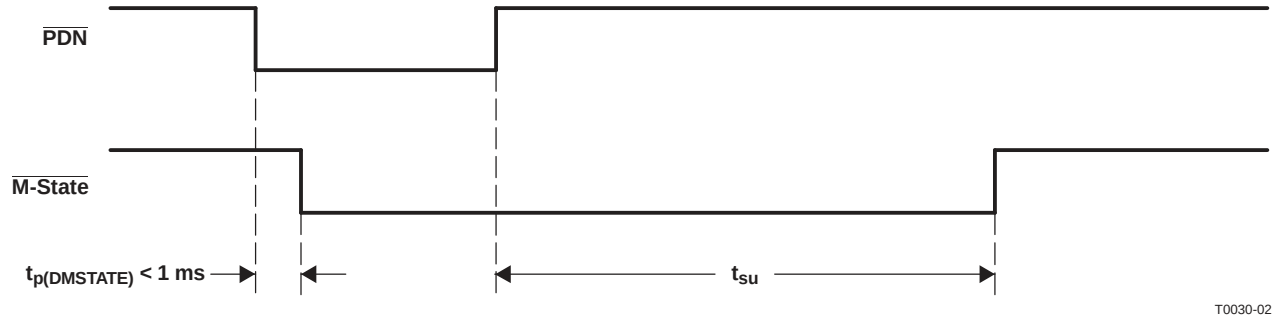
PARAMETER		MIN	TYP	MAX	UNIT
$t_{r(DMSTATE)}$	Time to $\overline{\text{M-STATE}}$ low			370	ns
$t_{w(RESET)}$	Pulse duration, RESET active	400		None	ns
$t_{r(I2C\_ready)}$	Time to enable I^2C		3		ms
$t_{r(run)}$	Device start-up time	10			ms

NOTE: Because a crystal time base is used, the system determines the CLK rates. Once the data rate and master clock ratio are determined, the system outputs audio if a master volume command is issued.

Figure 12. Reset Timing

Power-Down ($\overline{\text{PDN}}$) Timing

Control-signal parameters over recommended operating conditions (unless otherwise noted). Note that $\overline{\text{PDN}}$ does not clear I^2C registers.



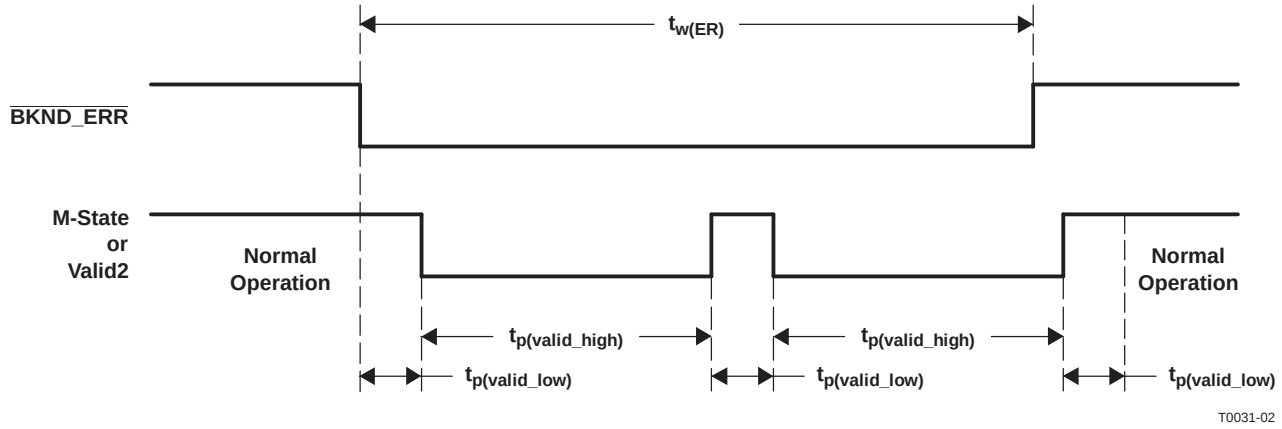
PARAMETER		MIN	TYP	MAX	UNIT
$t_{p(DMSTATE)}$	Time to $\overline{\text{M-STATE}}$ low			300	µs
	Number of MCLKs preceding the release of $\overline{\text{PDN}}$	5			
t_{su}	Device start-up time		120		ms

Figure 13. Power-Down Timing

Back-End Error ($\overline{\text{BKND\_ERR}}$)

Control-signal parameters over recommended operating conditions (unless otherwise noted)

Control-signal parameters over recommended operating conditions (unless otherwise noted)

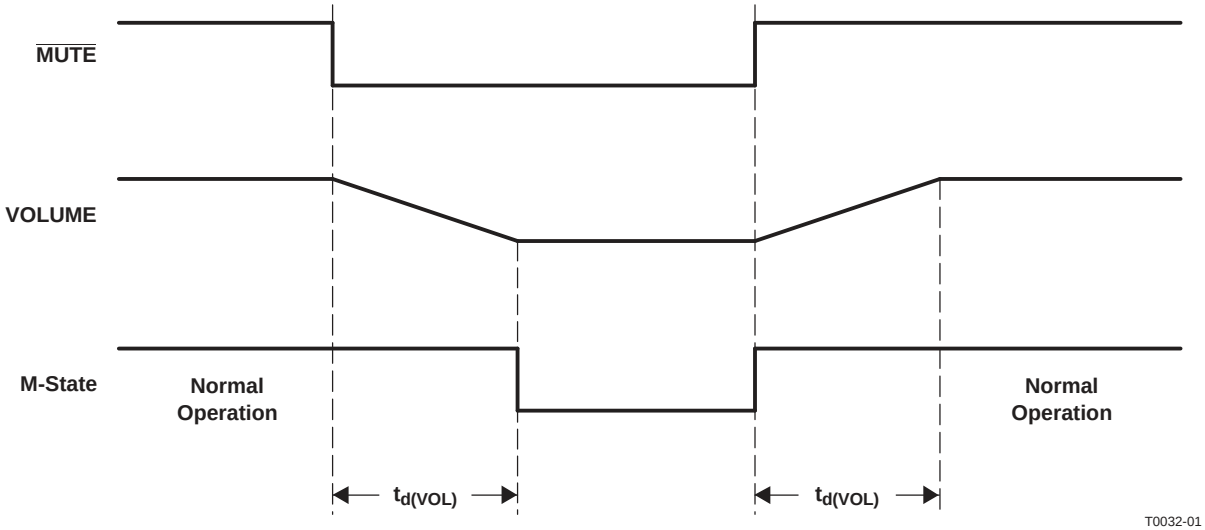


PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(ER)}$	Pulse duration, BKND_ERR active	350		None	ns
$t_{p(valid\_low)}$				<100	µs
$t_{p(valid\_high)}$	I^2C programmable to be between 1 to 10 ms	–25		25	% of interval

Figure 14. Error Recovery Timing

Mute Timing ($\overline{MUTE}$)

Control-signal parameters over recommended operating conditions (unless otherwise noted). Note that $\overline{MUTE}$ does not stop PWM switching; it stops the noise shaper, and therefore has less noise.



PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VOL)}$	Volume ramp time	Defined by rate setting(1)			ms

(1) See the *Volume Control Register (0x0E)* section.

Figure 15. Mute Timing

SERIAL INTERFACE CONTROL AND TIMING

I²S TIMING

I²S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 64 f_S is used to clock in the data. A delay of one bit clock occurs from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB-first and is valid on the rising edge of the bit clock. The TAS5086 masks unused trailing data bit positions.

2-Channel I²S (Philips Format) Stereo Input/Output

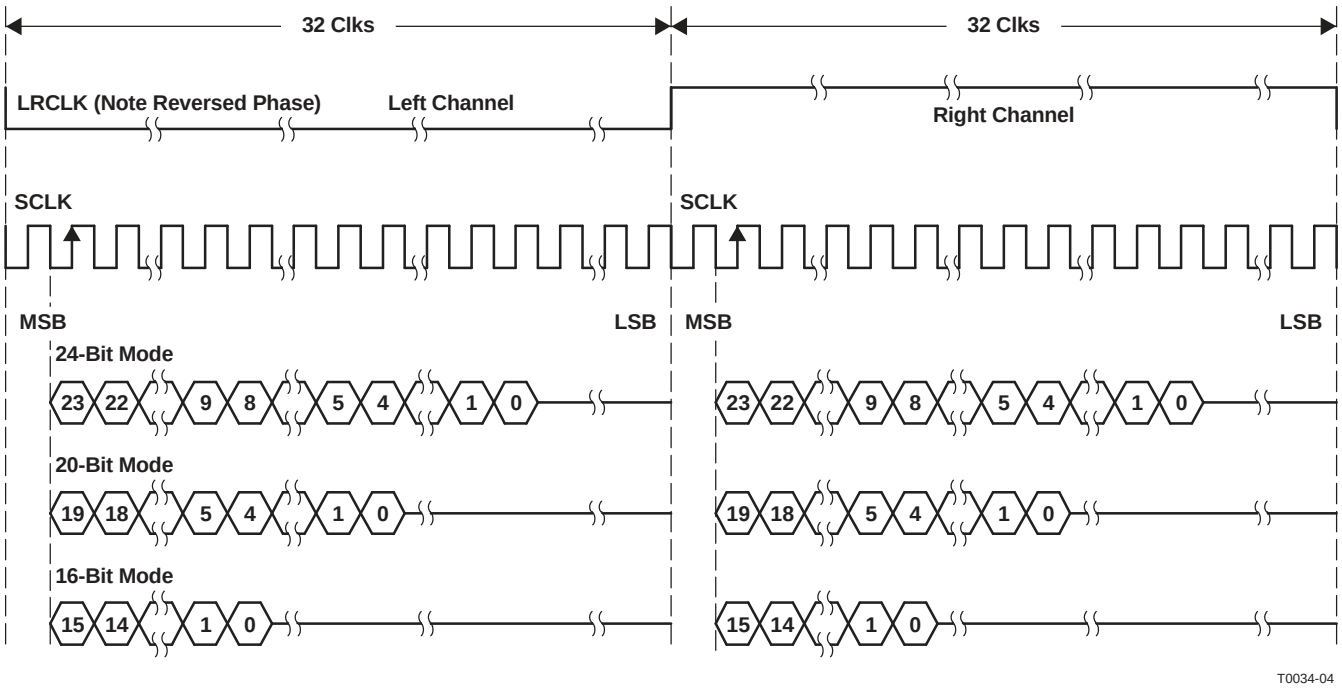


Figure 16. I²S 64-f_S Format

2-Channel I^2S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)

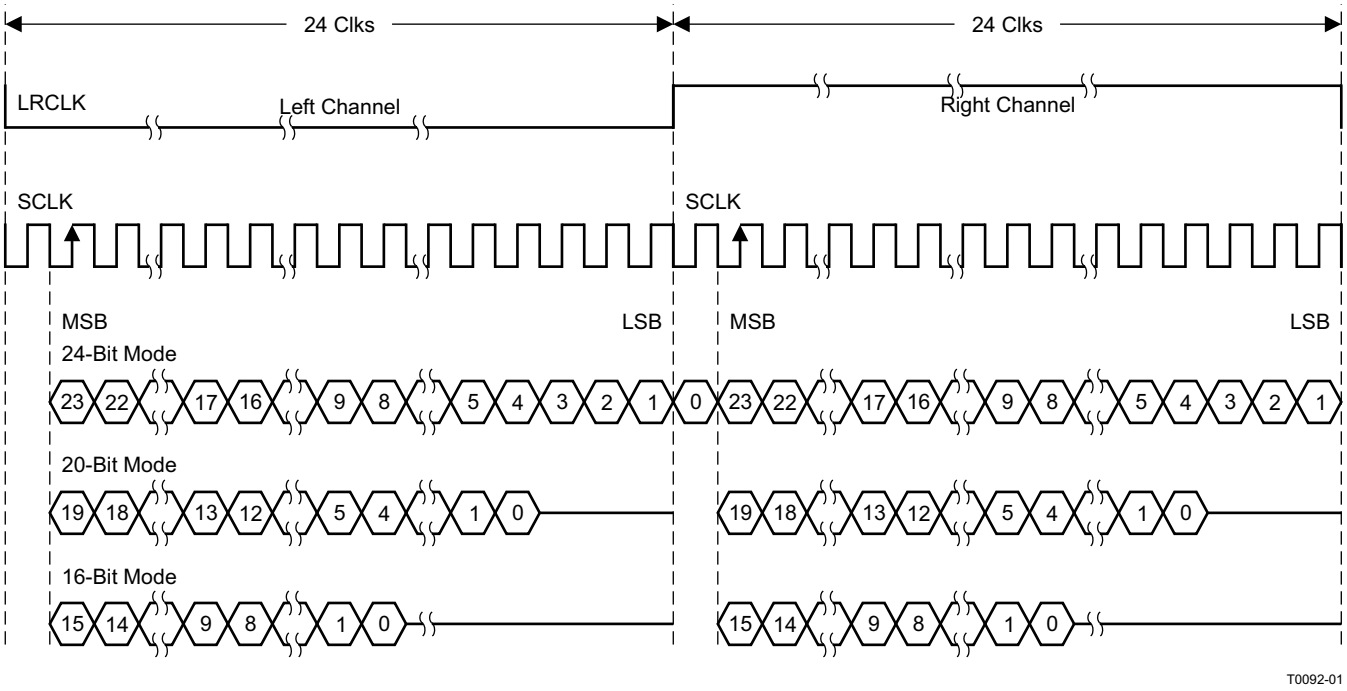


Figure 17. I^2S 48-f_S Format

LEFT-JUSTIFIED

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 64 f_S is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. The TAS5086 masks unused trailing data bit positions.

2-Channel Left-Justified Stereo Input

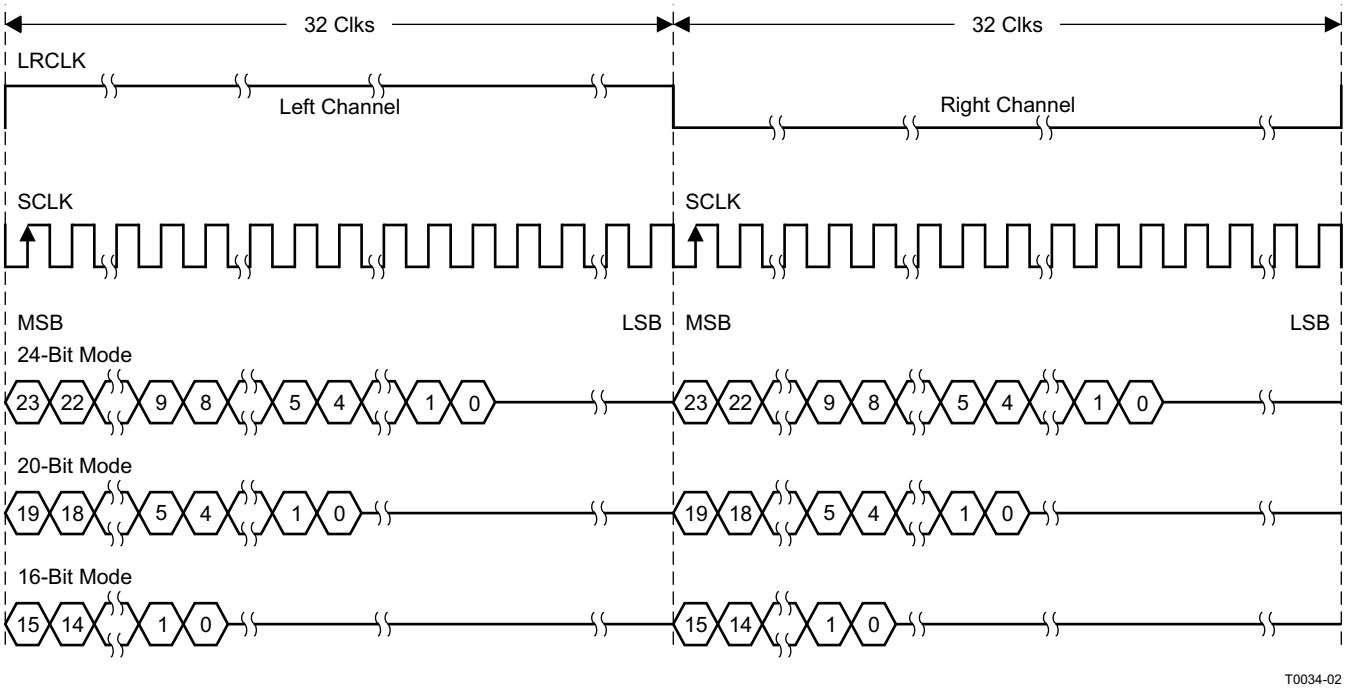


Figure 18. Left-Justified 64-f_S Format

2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)

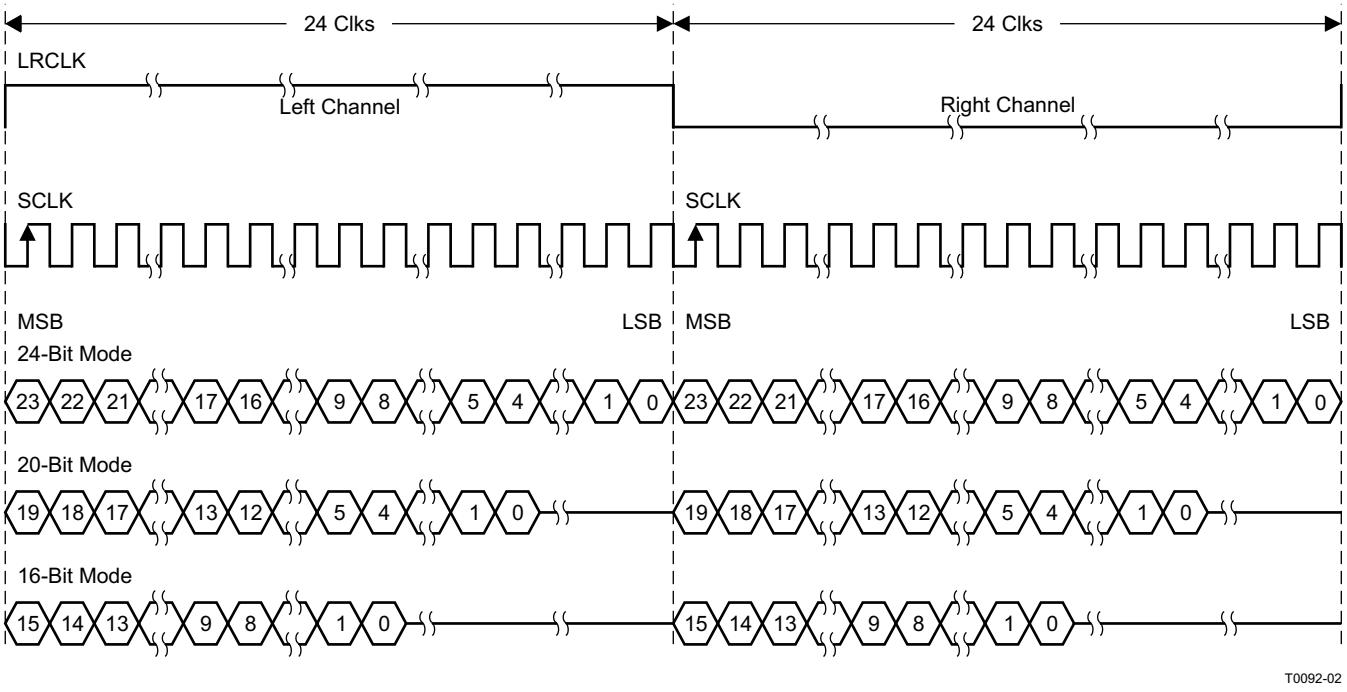


Figure 19. Left-Justified 48-f_S Format

Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 64 f_S is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode, the LSB of data always is clocked by the last bit clock before LRCLK transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The TAS5086 masks unused leading data bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input

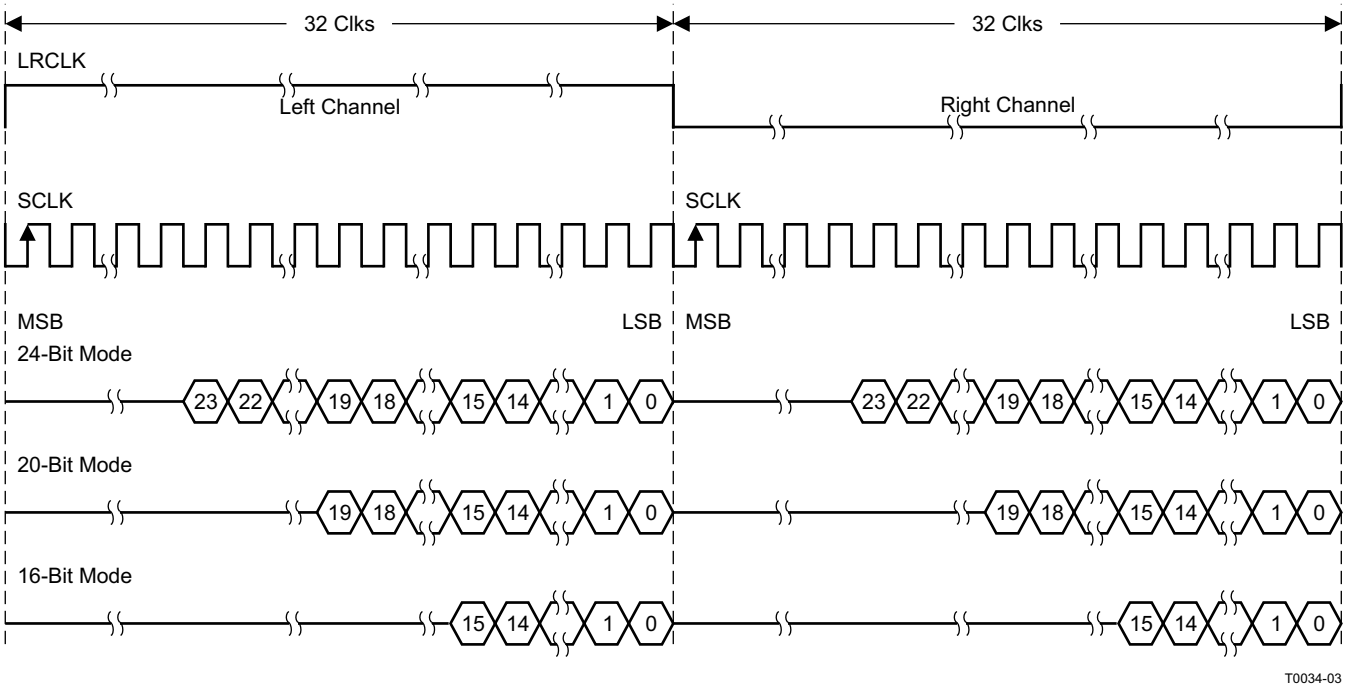


Figure 20. Right-Justified 64-f_S Format

2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)

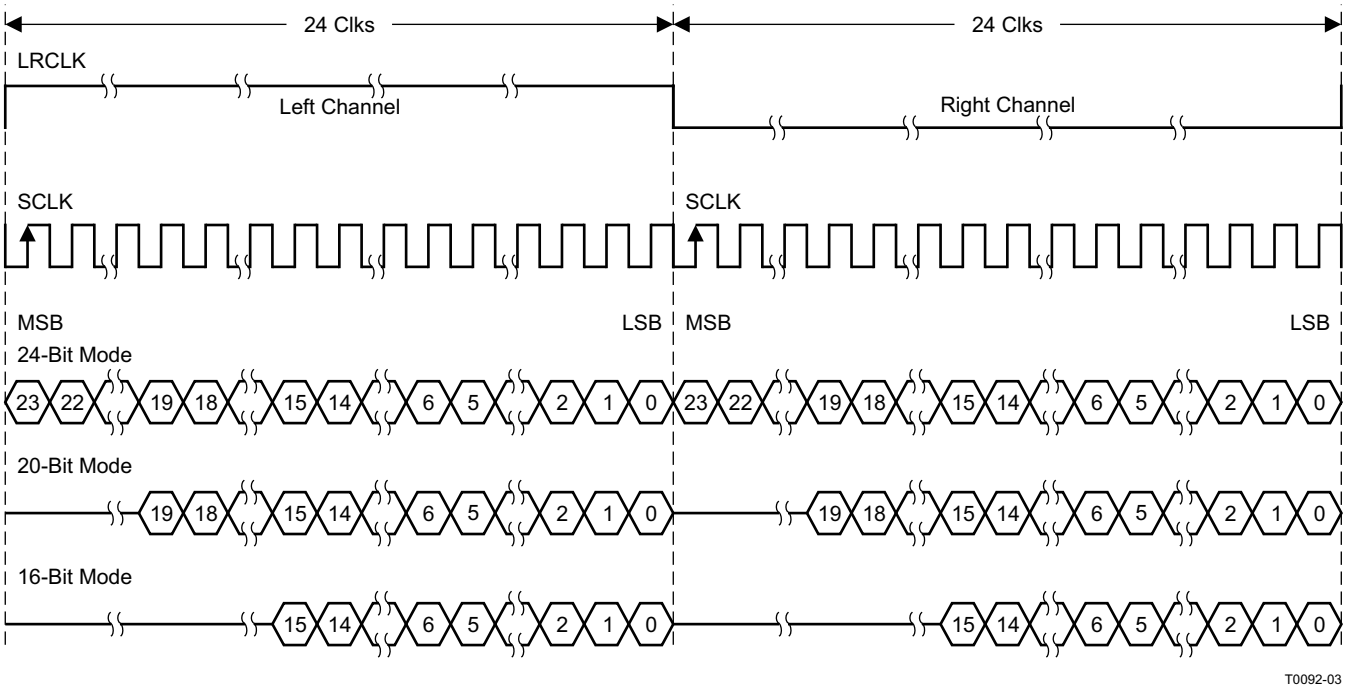


Figure 21. Right-Justified 48-f_S Bit Format

I²C SERIAL CONTROL INTERFACE

The TAS5086 has a bidirectional Inter IC (I^2C) interface that is compatible with the I^2C bus protocol and supports both single- and multiple-byte write and read operations. The control interface is used to program the registers of the device and to read device status.

The TAS5086 supports wait-state insertions by other I^2C devices on the bus. However, the TAS5086 performs all I^2C operations without I^2C wait cycles.

The TAS5086 supports standard-mode I^2C bus operation (100 kHz maximum) and fast I^2C bus operation (400 kHz maximum).

GENERAL I²C OPERATION

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 22. The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then wait for an acknowledge condition. The TAS5086 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the HIGH level for the bus.

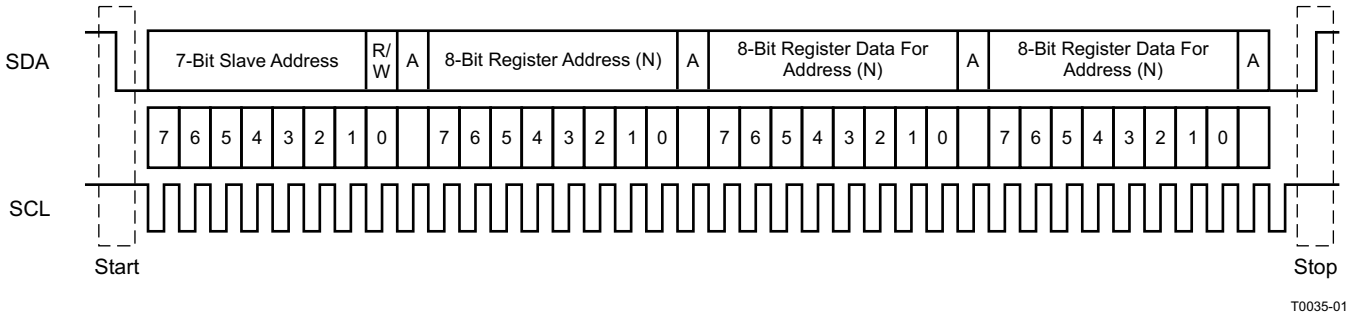


Figure 22. Typical I²C Sequence

An unlimited number of bytes can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 22.

The 7-bit address for the TAS5086 is 0011 011.

SINGLE- AND MULTIPLE-BYTE TRANSFERS

The serial control interface supports both single-byte and multiple-byte read/write operations for status registers and the general control registers associated with the PWM. However, for the DAP data processing registers, the serial control interface supports only multiple-byte (4-byte) read/write operations.

During multiple-byte read operations, the TAS5086 responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the TAS5086 compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. If a write command is received for a biquad subaddress, the TAS5086 expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded. Similarly, if a write command is received for a mixer coefficient, the TAS5086 expects to receive one 32-bit word.

Supplying a subaddress for each subaddress transaction is referred to as random I²C addressing. The TAS5086 also supports sequential I²C addressing. For write transactions, if a subaddress is issued, followed by data for that subaddress and the 15 subaddresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5086. For I²C sequential write transactions, the subaddress then serves as the start address and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; just the incomplete data is discarded.

SINGLE-BYTE WRITE

As shown is Figure 23, a single-byte data write transfer begins with the master device transmitting a start condition, followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the TAS5086 device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5086 internal memory address being accessed. After receiving the address byte, the TAS5086 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5086 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

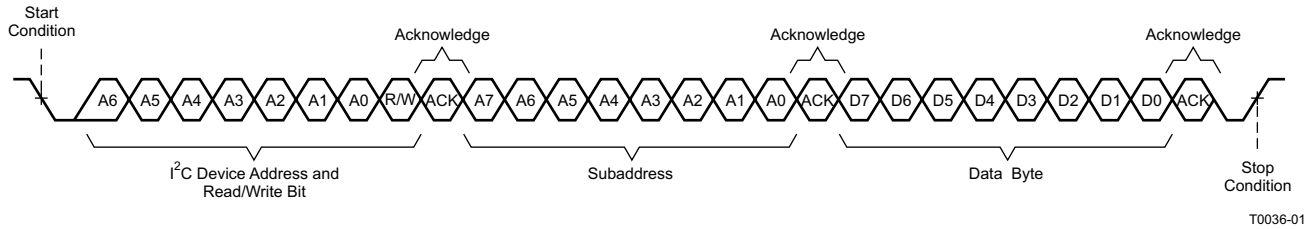


Figure 23. Single-Byte Write Transfer

MULTIPLE-BYTE WRITE AND INCREMENTAL MULTIPLE-BYTE WRITE

A multiple-byte data write transfer is identical to a single-byte data write transfer, except that multiple data bytes are transmitted by the master device to TAS5086 as shown in Figure 24. After receiving each data byte, the TAS5086 responds with an acknowledge bit.

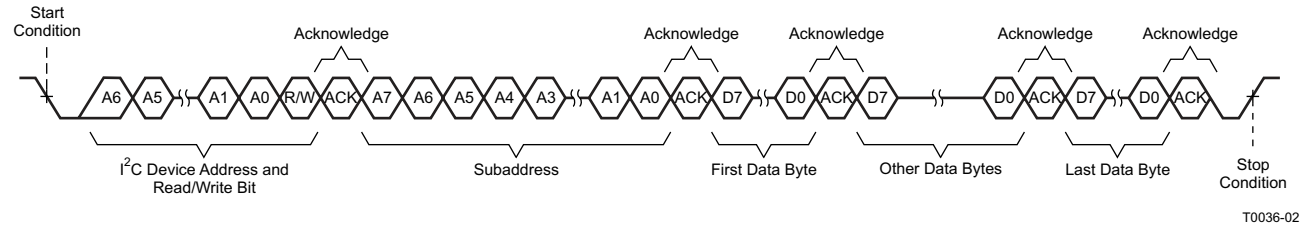


Figure 24. Multiple-Byte Write Transfer

The I²C supports a special mode that permits I²C write operations to be broken up into multiple data write operations that are multiples of 4 data bytes. These are 6-, 10-, 14-, 18-, ..., etc., -byte write operations that are composed of a device address, read/write bit, and subaddress and any multiple of 4 bytes of data. This permits the system to write large register values incrementally without blocking other I²C transactions.

This feature is enabled by the *append* subaddress (0xFE) in the TAS5086. The append address, 0xFE, enables the TAS5086 to append an integer number of 4-, 8-, 12-, 16-, … byte blocks of data to a register that was opened by a previous I²C register write operation, but has not received its complete number of data bytes.

When the correct number of bytes has been received, the TAS5086 starts processing the data.

The procedure to perform a multiple-byte write operation is as follows.

1. Start a normal I²C write operation by sending the device address, write bit, register subaddress, and an integer number of 4-byte data blocks. At the end of that sequence, a stop condition is sent.

   At this point the register has been opened. It then accepts the remaining data sent by one or more write operations, consisting of an integer number of 4-byte blocks. This data should be written to the append subaddress (0xFE).
2. At a later time, one or more append data transfers are performed to incrementally transfer the remaining number of bytes in sequential order to complete the register write operation. Each of these append operations is composed of the device address, write bit, append subaddress (0xFE), and an integer number of four bytes of data, followed by a stop condition.
3. The operation is terminated due to an error condition, and the data is flushed:
   - If a new subaddress is written to the TAS5086 before the correct number of bytes has been written
   - If a noninteger number of 4 bytes is written at the beginning or during any of the append operations
   - If a read bit is sent

SINGLE-BYTE READ

As shown in Figure 25, a single-byte data read transfer begins with the master device transmitting a start condition, followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal

memory address to be read. As a result, the read/write bit is set to a 0. After receiving the TAS5086 address and the read/write bit, the TAS5086 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition, followed by the TAS5086 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. After receiving the TAS5086 and the read/write bit, the TAS5086 again responds with an acknowledge bit. Next, the TAS5086 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge, followed by a stop condition, to complete the single-byte data read transfer.

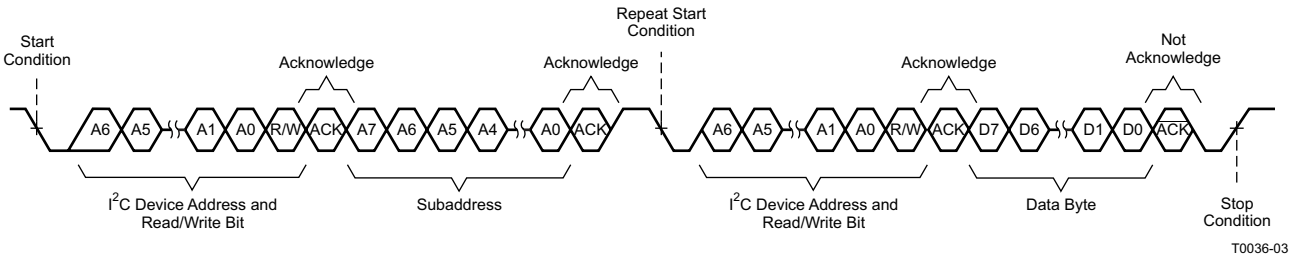


Figure 25. Single-Byte Read Transfer

MULTIPLE-BYTE READ

A multiple-byte data read transfer is identical to a single-byte data read transfer, except that multiple data bytes are transmitted by the TAS5086 to the master device as shown in Figure 26. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

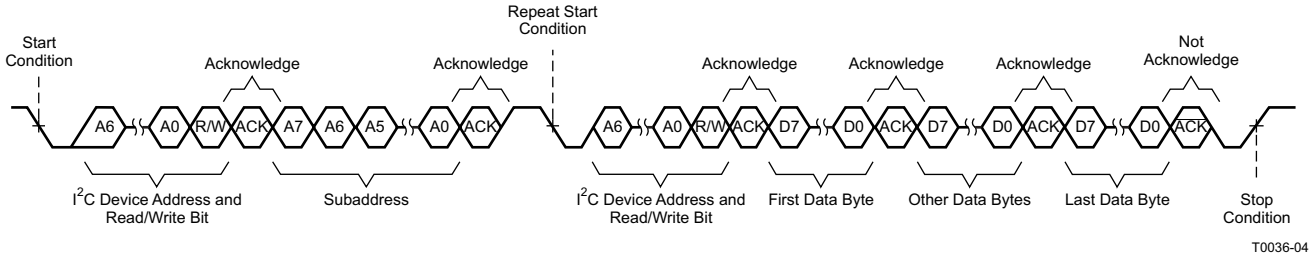


Figure 26. Multiple-Byte Read Transfer

COMMAND CHARACTERISTICS

The TAS5086 has two groups of I²C commands. One set is commands that are designed specifically to be operated while audio is streaming and that have built-in mechanisms to prevent noise, clicks, and pops. The other set does not have this built-in protection.

Commands that are designed to be adjusted while audio is streaming

- Master volume
- Master mute
- Individual channel volume
- Individual channel mute

Commands that the system executes without additional processing to prevent noise, clicks, or pops (in a number of cases this does not produce an audible click and pop)

- Serial data interface format
- De-emphasis
- Sample rate conversion
- Input multiplexer
- Output multiplexer
- Biquads
- Downmix

- Channel delay
- Enable/disable automatic MCLK and data-rate detection
- Manual or automatic MCLK and data-rate setting
- Enable/disable dc blocking
- Hard/soft unmute from clock error

SERIAL CONTROL INTERFACE REGISTER SUMMARY

Default values are in **bold**, table values "X" equals don't care and table values "–" equals an expansion of the table for detailed description of the respective bit.

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
0x00	Clock control register	1	Description shown in subsequent section	6C
0x01	Device ID register	1	Description shown in subsequent section	03
0x02	Error status register	1	Description shown in subsequent section	00
0x03	System control register 1	1	Description shown in subsequent section	A0
0x04	Serial data interface register	1	Description shown in subsequent section	05
0x05	System control register 2	1	Description shown in subsequent section	60
0x06	Soft mute register	1	Description shown in subsequent section	00
0x07	Master volume	1	Description shown in subsequent section	FF (mute)
0x08	Channel 1 vol	1	Description shown in subsequent section	30 (0 dB)
0x09	Channel 2 vol	1	Description shown in subsequent section	30 (0 dB)
0x0A	Channel 3 vol	1	Description shown in subsequent section	30 (0 dB)
0x0B	Channel 4 vol	1	Description shown in subsequent section	30 (0 dB)
0x0C	Channel 5 vol	1	Description shown in subsequent section	30 (0 dB)
0x0D	Channel 6 vol	1	Description shown in subsequent section	30 (0 dB)
0x0E	Volume control register	1	Description shown in subsequent section	B1
0x0F			RESERVED(1)	
0x10	Modulation limit register	1	Description shown in subsequent section	02
0x11–0x17			RESERVED(1)	
0x18	PWM start register	1	Description shown in subsequent section	3F
0x19	Surround register	1	Description shown in subsequent section	00
0x1A	Split cap charge period register	1	Description shown in subsequent section	18
0x1B	OSC_TRIM	1	Oscillator trim register	82
0x1C	BKNDERR register	1	BKNDErr Register	05
0x1D–0x1F			RESERVED(1)	
0x20	Input MUX register	4	Description shown in subsequent section	0x00, 0x01, 0x23, 0x45
0x21	Downmix input MUX register	4	Description shown in subsequent section	0x00, 0x00, 0x40, 0x3F
0x22	AM tuned frequency	4	Description shown in subsequent section	0x00, 0x00, 0x00, 0x00
0x23	ch6_bq[1]	20	b0[25:24] b0[(23:16], b0[15:8], b0[7:0]	0x00, 0x80, 0x00, 0x00
			b1[25:24] b1[23:16], b1[15:8], b1[7:0]	0x00, 0x00, 0x00, 0x00
			b2[25:24] b2[23:16], b2[15:8], b2[7:0]	0x00, 0x00, 0x00, 0x00
			a1[25:24] a1[23:16], a1[15:8], a1[7:0]	0x00, 0x00, 0x00, 0x00
			a2[25:24] a2[23:16], a2[15:8], a2[7:0]	0x00, 0x00, 0x00, 0x00
0x24	ch6_bq[2]	20	b0[25:24] b0[23:16], b0[15:8], b0[7:0]	0x00, 0x80, 0x00, 0x00
			b1[25:24] b1[23:16], b1[15:8], b1[7:0]	0x00, 0x00, 0x00, 0x00
			b2[25:24] b2[23:16], b2[15:8], b2[7:0]	0x00, 0x00, 0x00, 0x00
			a1[25:24] a1[23:16], a1[15:8], a1[7:0]	0x00, 0x00, 0x00, 0x00
			a2[25:24] a2[23:16], a2[15:8], a2[7:0]	0x00, 0x00, 0x00, 0x00

(1) Reserved registers should not be accessed.

Default values are in **bold**, table values "X" equals don't care and table values "–" equals an expansion of the table for detailed description of the respective bit.

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
0x25	PWM MUX register		Description shown in subsequent section	0x00, 0x32, 0x45, 0x10
0x26	1/G register	4	x[25:24] x[23:16], x[15:8], x[7:0]	0x00, 0x80, 0x00, 0x00
0x27			RESERVED(1)	
0x28	Scale register	4	x[25:24] x[23:16], x[15:8], x[7:0]	0x00, 0x80, 0x00, 0x00
0x29–0xFD			RESERVED(1)	
0xFE	Repeat subaddress	4+4N		0x00, 0x00, 0x00, 0x00
0xFF			RESERVED(1)	

CLOCK CONTROL REGISTER (0x00)

In the manual mode, the clock control register provides a way for the system microprocessor to update the data and clock rates, based on the sample rate and associated clock frequencies. In the autodetect mode, the clocks are determined automatically by the TAS5086. In this case, the clock control register contains the autodetected clock status as automatically detected. Bits D7–D5 select the sample rate. Bits D4–D2 select the MCLK frequency. Bit D1 selects the bit clock (SCLK) frequency. Bit D0 is used in manual mode only. In this mode, when the clocks are updated, a 1 must be written to D1 to inform the TAS5086 that the written clocks are valid.

Table 2. Clock Control Register (0x00)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	–	–	–	–	–	f_S = 32-kHz sample rate
0	0	1	–	–	–	–	–	f_S = 38-kHz sample rate
0	1	0	–	–	–	–	–	f_S = 44.1-kHz sample rate
0	**1**	**1**	**–**	**–**	**–**	**–**	**–**	**f_S = 48-kHz sample rate**
1	0	0	–	–	–	–	–	f_S = 88.2- kHz sample rate
1	0	1	–	–	–	–	–	f_S = 96-kHz sample rate
1	1	0	–	–	–	–	–	f_S = 176.4-kHz sample rate
1	1	1	–	–	–	–	–	f_S = 192-kHz sample rate
–	–	–	0	0	0	–	–	MCLK frequency = 64 × f_S(1)
–	–	–	0	0	1	–	–	MCLK frequency = 128 × f_S
–	–	–	0	1	0	–	–	MCLK frequency = 192 × f_S
–	**–**	**–**	**0**	**1**	**1**	**–**	**–**	**MCLK frequency = 256 × f_S**
–	–	–	1	0	0	–	–	MCLK frequency = 384 × f_S
–	–	–	1	0	1	–	–	MCLK frequency = 512 × f_S
–	–	–	1	1	0	–	–	Reserved
–	–	–	1	1	1	–	–	Reserved
–	–	–	–	–	–	1	–	Bit clock (SCLK) frequency = 48 × f_S
–	**–**	**–**	**–**	**–**	**–**	**0**	**–**	**Bit clock (SCLK) frequency = 64 × f_S**
–	**–**	**–**	**–**	**–**	**–**	**–**	**0**	**Clock not valid (in manual mode only)**
–	–	–	–	–	–	–	1	Clock valid (in manual mode only)

(1) MCLK frequency = 64 x f_S is not available for 32-, 44.1-, 48-, 88.2-, and 96-kHz data rates

DEVICE ID REGISTER (0x01)

The device ID register contains the ID code for the TAS5086.

Table 3. General Status Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0								Default
–	**0**	**0**	**0**	**0**	**0**	**1**	**1**	Identification code for the TAS5086

ERROR STATUS REGISTER (0x02)

Note that the error bits are sticky bits that are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if there are any persistent errors.

Table 4. Error Status Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	1	–	–	–	–	–	–	PLL auto lock error
–	–	1	–	–	–	–	–	SCLK error
–	–	–	1	–	–	–	–	LRCLK error
–	–	–	–	1	–	–	–	Frame slip
–	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**No errors**

SYSTEM CONTROL REGISTER 1 (0x03)

System control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled.

If 1, the dc-blocking filter (–3-dB cutoff < 1 Hz) for each channel is enabled (default).

Bit D6: Not used

Bit D5: If 0, use soft unmute on recovery from clock error. This is a slow recovery.

If 1, use hard unmute on recovery from clock error (default). This is a fast recovery.

Bit D4: If 0, the downmix is output on SDOUT as I^2S signal (default).

If 1, SDIN4 is output on SDOUT as I^2S signal.

Bit D3: If 0, clock autodetect is enabled (default).

If 1, clock autodetect is disabled.

Bit D2: If 0, soft start is enabled (default).

If 1, soft start is disabled.

Bits D1–D2: Select de-emphasis

Table 5. System Control Register 1 (0x03)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	PWM high-pass (dc blocking) disabled
1	**–**	**–**	**–**	**–**	**–**	**–**	**–**	**PWM high-pass (dc blocking) enabled**
–	–	0	–	–	–	–	–	Soft unmute on recovery from clock error
–	**–**	**1**	**–**	**–**	**–**	**–**	**–**	**Hard unmute on recovery from clock error**
–	**–**	**–**	**0**	**–**	**–**	**–**	**–**	**Output downmix on SDOUT**
–	–	–	1	–	–	–	–	Output SDIN4 mix on SDOUT
–	**–**	**–**	**–**	**0**	**–**	**–**	**–**	**Enable clock autodetect**
–	–	–	–	1	–	–	–	Disable clock autodetect
–	**–**	**–**	**–**	**–**	**0**	**–**	**–**	**Enable soft start**
–	–	–	–	–	1	–	–	Disable soft start
–	**–**	**–**	**–**	**–**	**–**	**0**	**0**	**No de-emphasis**
–	–	–	–	–	–	0	1	De-emphasis for f_S = 32 kHz
–	–	–	–	–	–	1	0	De-emphasis for f_S = 44.1 kHz
–	–	–	–	–	–	1	1	De-emphasis for f_S = 48 kHz

SERIAL DATA INTERFACE REGISTER (0x04)

As shown in Table 6, the TAS5086 supports nine serial data modes. The default is 24-bit, I^2S mode.

Table 6. Serial Data Interface Control Register (0x04) Format

RECEIVE SERIAL DATA INTERFACE FORMAT	WORD LENGTHS	D7–D4	D3	D2	D1	D0
Right-justified	16	0000	0	0	0	0
Right-justified	20	0000	0	0	0	1
Right-justified	24	0000	0	0	1	0
I^2S	16	0000	0	0	1	1
I^2S	20	0000	0	1	0	0
I^2S	**24**	**0000**	**0**	**1**	**0**	**1**
Left-justified	16	0000	0	1	1	0
Left-justified	20	0000	0	1	1	1
Left-justified	24	0000	1	0	0	0
Reserved		0000	1	0	0	1
Reserved		0000	1	0	1	0
Reserved		0000	1	0	1	1
Reserved		0000	1	1	0	0
Reserved		0000	1	1	0	1
Reserved		0000	1	1	1	0
Reserved		0000	1	1	1	1
Default values are in **bold**						

SYSTEM CONTROL REGISTER 2 (0x05)

Bit D6 is a **control** bit and bit D5 is a **configuration** bit.

When bit D6 is set low, the system starts playing; otherwise, the outputs are shut down.

Bit D5 defines the configuration of the system, i.e., it determines what configuration the system runs in when bit D6 is set low. When this bit is asserted, the system is configured to surround, meaning all channels are switching. Otherwise, only a subset of the PWMs runs, corresponding to a 2.0 or 2.1 configuration as determined by the surround register (0x19).

Bit D5 should be changed only when bit D6 is set to 1, meaning that it is only possible to switch configuration from surround to 2.0/2.1 by resetting the TAS5086 and then restarting it again in the new configuration.

Table 7. System Control Register 2 (0x05)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	1	X	–	–	–	–	–	All channels are shut down (hard mute).
–	**1**	**1**	**–**	**–**	**–**	**–**	**–**	**All channels are shut down (hard mute). VALID1 = 0 and VALID2 = 0**
–	0	1	–	–	–	–	–	When D6 is deasserted, all channels are started. VALID1 = 1 and VALID2 = 1
–	0	0	–	–	–	–	–	When D6 is deasserted, all channels not belonging to shutdown group 1 are started. VALID1 = 0 and VALID2 = 1

SOFT MUTE REGISTER (0x06)

Table 8. Soft Mute Register (0x06)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	–	–	–	1	Soft mute channel 1
–	–	–	–	–	–	1	–	Soft mute channel 2
–	–	–	–	–	1	–	–	Soft mute channel 3
–	–	–	–	1	–	–	–	Soft mute channel 4
–	–	–	1	–	–	–	–	Soft mute channel 5
–	–	1	–	–	–	–	–	Soft mute channel 6
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Unmute all channels**

VOLUME REGISTERS (0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D)

Master volume – 0x07 (default is mute)
Channel 1 volume – 0x08 (default is 0 dB)
Channel 2 volume – 0x09 (default is 0 dB)
Channel 3 volume – 0x0A (default is 0 dB)
Channel 4 volume – 0x0B (default is 0 dB)
Channel 5 volume – 0x0C (default is 0 dB)
Channel 6 volume – 0x0D (default is 0 dB)

Table 9. Volume Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	24 dB
0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0 dB (default for individual channel volume)**
1	1	1	1	1	1	1	0	–103 dB
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**MUTE (default for master volume)**

VOLUME CONTROL REGISTER (0x0E)

Bit D7: Reserved = 1

Bit D6: If 0, then biquad 1 (BQ1) volume compensation part only is disabled (default).

If 1, then BQ1 volume compensation is enabled.

Bit D5: If 0, disable 38-kHz input sample rate detection (38 kHz should be set manually by the microprocessor).

If 1, enable 38-kHz input sample rate detection.

Bit D4: Reserved = 1

Bit D3: Not used

Bits D2–D0: Volume slew rate

Table 10. Volume Control Register (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	Reserved (must be 1)
–	**0**	**–**	**–**	**–**	**–**	**–**	**–**	**Disable biquad volume compensation**
–	1	–	–	–	–	–	–	Enable biquad volume compensation
–	–	**1**	–	–	–	–	–	**Enable 38-kHz input sample rate detection**
–	–	0	–	–	–	–	–	Disable 38-kHz input sample rate detection
–	–	–	**1**	–	–	–	–	**Reserved (must be 1)**
–	–	–	–	–	0	0	0	Volume Slew 512 Steps
–	–	–	–	–	**0**	**0**	**1**	**Volume Slew 1024 Steps**
–	–	–	–	–	0	1	0	Volume Slew 2048 Steps
–	–	–	–	–	0	1	1	Volume Slew 256 Steps

MODULATION LIMIT REGISTER (0x10)

Set modulation limit. See the appropriate power stage data sheet for recommended modulation limits.

Table 11. Modulation Limit Register (0x10)

D7	D6	D5	D4	D3	D2	D1	D0	LIMIT [DCLKs]	MIN WIDTH [DCLKs]	MODULATION LIMIT
–	–	–	–	–	0	0	0	1	2	99.2%
–	–	–	–	–	0	0	1	2	4	98.4%
–	**–**	**–**	**–**	**–**	**0**	**1**	**0**	**3**	**6**	**97.7%**
–	–	–	–	–	0	1	1	4	8	96.9%
–	–	–	–	–	1	0	0	5	10	96.1%
–	–	–	–	–	1	0	1	6	12	95.3%
–	–	–	–	–	1	1	0	7	14	94.5%
–	–	–	–	–	1	1	1	8	16	93.8%

PWM START REGISTER (0x18)

Bits D7 and D6: Define which start sequence is used, either low-Z or mid-Z. Not all power stages are compatible with mid-Z; double-check the power-stage data sheet.

Bits D5–D0: Define which PWMs are used for charging the split capacitors and which PWMs should stay low, indicating the output stages are to be held in Hi-Z under split-capacitor charging.

For most systems, this register is always 0x3F. The setting depends on how the power stage is connected.

Table 12. PWM Start Register (0x18)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**–**	**–**	**–**	**–**	**–**	**–**	**–**	**Use Low-Z sequence for part 1 of the start**
1	–	–	–	–	–	–	–	Use Mid-Z sequence for part 1 of the start
–	**0**	–	–	–	–	–	–	**Use Low-Z sequence for part 2 of the start**
–	1	–	–	–	–	–	–	Use Mid-Z sequence for part 2 of the start
–	–	**1**	–	–	–	–	–	**Start channel 6 under part 1 of the start**
–	–	0	–	–	–	–	–	Start channel 6 under part 2 of the start
–	**–**	**–**	**1**	**–**	**–**	**–**	**–**	**Start channel 5 under part 1 of the start**
–	–	–	0	–	–	–	–	Start channel 5 under part 2 of the start
–	**–**	**–**	**–**	**1**	**–**	**–**	**–**	**Start channel 4 under part 1 of the start**
–	–	–	–	0	–	–	–	Start channel 4 under part 2 of the start
–	**–**	**–**	**–**	**–**	**1**	**–**	**–**	**Start channel 3 under part 1 of the start**
–	–	–	–	–	0	–	–	Start channel 3 under part 2 of the start
–	**–**	**–**	**–**	**–**	**–**	**1**	**–**	**Start channel 2 under part 1 of the start**
–	–	–	–	–	–	0	–	Start channel 2 under part 2 of the start
–	**–**	**–**	**–**	**–**	**–**	**–**	**1**	**Start channel 1 under part 1 of the start**
–	–	–	–	–	–	–	0	Start channel 1 under part 2 of the start

SURROUND REGISTER (0x19)

Defines which channels should be running in the 2.0/2.1 mode.

The channels having their surround register set (HIGH) belong to shutdown group 1. They are associated with VALID1. VALID1 is the signal that is driven low to disable channels when the system is operating in, for example, stereo mode or 2.1 mode.

Example: If

PWM_1 connects to front left
PWM_2 connects to front right
PWM_3 connects to surround left
PWM_4 connects to surround right
PWM_5 connects to center
PWM_6 connects to sub

and you have a 2.1 mode, then VALID1 connects to the reset of surround left, surround right, and center. VALID2 connects to the reset of front left, front right, and sub.

That means that the surround register (0x19) is loaded with 0001 1100b = 0x1C.

Note: You must always change channel modes with all channels shut down (register 0x05 = 60).

Table 13. Surround Register (0x19)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	1	–	–	–	–	–	PWM_6 belongs to shutdown group 1 (VALID1)
–	**–**	**0**	**–**	**–**	**–**	**–**	**–**	PWM_6 **belongs to shutdown group 2 (VALID2)**
–	–	–	1	–	–	–	–	PWM_5 belongs to shutdown group 1 (VALID1)
–	**–**	**–**	**0**	**–**	**–**	**–**	**–**	PWM_5 **belongs to shutdown group 2 (VALID2)**
–	–	–	–	1	–	–	–	PWM_4 belongs to shutdown group 1 (VALID1)
–	**–**	**–**	**–**	**0**	**–**	**–**	**–**	PWM_4 **belongs to shutdown group 2 (VALID2)**
–	–	–	–	–	1	–	–	PWM_3 belongs to shutdown group 1 (VALID1)
–	**–**	**–**	**–**	**–**	**0**	**–**	**–**	PWM_3 **belongs to shutdown group 2 (VALID2)**
–	–	–	–	–	–	1	–	PWM_2 belongs to shutdown group 1 (VALID1)
–	**–**	**–**	**–**	**–**	**–**	**0**	**–**	PWM_2 **belongs to shutdown group 2 (VALID2)**
–	–	–	–	–	–	–	1	PWM_1 belongs to shutdown group 1 (VALID1)
–	**–**	**–**	**–**	**–**	**–**	**–**	**0**	PWM_1 **belongs to shutdown group 2 (VALID2)**

SPLIT-CAPACITOR CHARGE PERIOD REGISTER (0x1A)

This register should contain the code that closely matches the external single-ended split-capacitor charge period. The TAS5086 waits for this period of time before starting the PWM signals. This helps reduce pops and clicks. This is used only with the split-capacitor configuration.

Table 14. Split-Capacitor Charge Period Register (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	0	0	–	–	–	No split-capacitor charge period
–	–	–	0	1	0	0	0	13-ms split-capacitor charge period
–	–	–	0	1	0	0	1	16.9-ms split-capacitor charge period
–	–	–	0	1	0	1	0	23.4-ms split-capacitor charge period
–	–	–	0	1	0	1	1	31.2-ms split-capacitor charge period
–	–	–	0	1	1	0	0	41.6-ms split-capacitor charge period
–	–	–	0	1	1	0	1	54.6-ms split-capacitor charge period
–	–	–	0	1	1	1	0	72.8-ms split-capacitor charge period
–	–	–	0	1	1	1	1	96.2-ms split-capacitor charge period
–	–	–	1	0	0	0	0	130-ms split-capacitor charge period
–	–	–	1	0	0	0	1	156-ms split-capacitor charge period
–	–	–	1	0	0	1	0	234-ms split-capacitor charge period
–	–	–	1	0	0	1	1	312-ms split-capacitor charge period
–	–	–	1	0	1	0	0	416-ms split-capacitor charge period
–	–	–	1	0	1	0	1	546-ms split-capacitor charge period
–	–	–	1	0	1	1	0	728-ms split-capacitor charge period
–	–	–	1	0	1	1	1	962-ms split-capacitor charge period
–	**–**	**–**	**1**	**1**	**0**	**0**	**0**	**1300-ms split-capacitor charge period**
–	–	–	1	1	0	0	1	1690-ms split-capacitor charge period
–	–	–	1	1	0	1	0	2340-ms split-capacitor charge period
–	–	–	1	1	0	1	1	3120-ms split-capacitor charge period
–	–	–	1	1	1	0	0	4160-ms split-capacitor charge period
–	–	–	1	1	1	0	1	5460-ms split-capacitor charge period
–	–	–	1	1	1	1	0	7280-ms split-capacitor charge period
–	–	–	1	1	1	1	1	9620-ms split-capacitor charge period

OSCILLATOR TRIM REGISTER (0x1B)

The TAS5086 PWM processor contains an internal oscillator for PLL reference. This reduces system cost because an external reference is not required. A trim resitor value of 18 kΩ is recomended. This should be connected between TAS5086 pin 14 (OSC_RES) and pin 12 (DVSS).

Two procedures are available for trimming the internal oscillator. The factory-trim procedure is recommended for most users. This procedure simply enables the factory trim that was previously done at the TAS5086 factory.

Note that only one trim procedure should be used. It always should be run following reset of the TAS5086.

Oscillator Factory-Trim Enable Procedure Example

1. Reset the TAS5086 (power up or toggle the RESET pin).
2. Write data 0x00 to register 0x1B (enable factory trim).
3. Write data 0x20 to register 0x05 (start all channels).
4. Write data 0x30 to register 0x07 (unmute and set master volume to 0 dB).

Oscillator Field-Trim Procedure Example (Use only if input LRCLK frequency is known)

1. Reset the TAS5086 (power up or toggle the RESET pin).
2. Provide a known LRCLK (e.g., 48 kHz).
3. Write LRCLK frequency to register 0x00 (e.g., for 48 kHz, write 0x6D to register 0x00).
4. Write data 0x03 to register 0x1B (field-trim command).
5. Write data 0x20 to register 0x05 (start all channels).
6. Write data 0x30 to register 0x07 (unmute and set master volume to 0 dB).

Table 15. Oscillator Trim Register (0x1B)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	0	–	–	–	–	–	–	Oscillator trim not done (read only)
–	1	–	–	–	–	–	–	Oscillator trim done
–	–	0	0	0	0	–	–	Reserved
–	–	–	–	–	–	0	–	Select factory trim
–	–	–	–	–	–	1	–	Select field trim
–	–	–	–	–	–	–	1	Trim oscillator command

BKNDERR REGISTER (0x1C)

When a back-end error signal is received ($\overline{\text{BKND\_ERR}}$ = LOW), all the output stages are reset by setting all PWM, VALID1, and VALID2 signals LOW. Subsequently, the modulator waits approximately for the time listed in Table 16 before initiation of a reset.

Table 16. BKNDERR Register (0x1C)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	0	0	0	0	Set back-end reset period to < 1.3 ms
–	–	–	–	0	0	0	1	Set back-end reset period to 1.3 ms
–	–	–	–	0	0	1	0	Set back-end reset period to 2.6 ms
–	–	–	–	0	0	1	1	Set back-end reset period to 3.9 ms
–	–	–	–	0	1	0	0	Set back-end reset period to 5.2 ms
–	**–**	**–**	**–**	**0**	**1**	**0**	**1**	**Set back-end reset period to 6.5 ms**
–	–	–	–	0	1	1	0	Set back-end reset period to 7.8 ms
–	–	–	–	0	1	1	1	Set back-end reset period to 9.1 ms
–	–	–	–	1	0	0	0	Set back-end reset period to 10.4 ms
–	–	–	–	1	0	0	1	Set back-end reset period to 11.7 ms
–	–	–	–	1	0	1	0	Set back-end reset period to 13 ms

Table 16. BKNDERR Register (0x1C) (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	1	0	1	1	Set back-end reset period to 13 ms
–	–	–	–	1	1	X	X	Set back-end reset period to 13 ms

INPUT MULTIPLEXER REGISTER (0x20)

The hexadecimal value for each nibble is the channel number. For each input multiplexer, any input from SDIN1, SDIN2, and SDIN3 can be mapped to any internal TAS5086 channel.

Default is 0x0001 2345.

Table 17. Input Multiplexer Register (0x20)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved = 0x00**
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	**0**	**0**	**–**	**–**	**–**	**–**	**SDIN1-L to channel 1**
0	0	0	1	–	–	–	–	SDIN1-R to channel 1
0	0	1	0	–	–	–	–	SDIN2-L to channel 1
0	0	1	1	–	–	–	–	SDIN2-R to channel 1
0	1	0	0	–	–	–	–	SDIN3-L to channel 1
0	1	0	1	–	–	–	–	SDIN3-R to channel 1
0	1	1	0	–	–	–	–	Ground (0) to channel 1
0	1	1	1	–	–	–	–	No connection
–	–	–	–	0	0	0	0	SDIN1-L to channel 2
–	**–**	**–**	**–**	**0**	**0**	**0**	**1**	**SDIN1-R to channel 2**
–	–	–	–	0	0	1	0	SDIN2-L to channel 2
–	–	–	–	0	0	1	1	SDIN2-R to channel 2
–	–	–	–	0	1	0	0	SDIN3-L to channel 2
–	–	–	–	0	1	0	1	SDIN3-R to channel 2
–	–	–	–	0	1	1	0	Ground (0) to channel 2
–	–	–	–	0	1	1	1	No connection
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	0	0	0	–	–	–	–	SDIN1-L to channel 3
0	0	0	1	–	–	–	–	SDIN1-R to channel 3
0	**0**	**1**	**0**	**–**	**–**	**–**	**–**	**SDIN2-L to channel 3**
0	0	1	1	–	–	–	–	SDIN2-R to channel 3
0	1	0	0	–	–	–	–	SDIN3-L to channel 3
0	1	0	1	–	–	–	–	SDIN3-R to channel 3
0	1	1	0	–	–	–	–	Ground (0) to channel 3
0	1	1	1	–	–	–	–	No connection
–	–	–	–	0	0	0	0	SDIN1-L to channel 4
–	–	–	–	0	0	0	1	SDIN1-R to channel 4
–	–	–	–	0	0	1	0	SDIN2-L to channel 4
–	**–**	**–**	**–**	**0**	**0**	**1**	**1**	**SDIN2-R to channel 4**
–	–	–	–	0	1	0	0	SDIN3-L to channel 4
–	–	–	–	0	1	0	1	SDIN3-R to channel 4
–	–	–	–	0	1	1	0	Ground (0) to channel 4
–	–	–	–	0	1	1	1	No connection

Table 17. Input Multiplexer Register (0x20) (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	–	–	–		SDIN1-L to channel 5
0	0	0	1	–	–	–	–	SDIN1-R to channel 5
0	0	1	0	–	–		–	SDIN2-L to channel 5
0	0	1	1	–	–		–	SDIN2-R to channel 5
0	**1**	**0**	**0**	**–**		**–**	**–**	**SDIN3-L to channel 5**
0	1	0	1	–	–	–	–	SDIN3-R to channel 5
0	1	1	0	–	–	–	–	Ground (0) to channel 5
0	1	1	1	–	–	–	–	No connection
–	–	–	–	0	0	0	0	SDIN1-L to channel 6
–	–	–	–	0	0	0	1	SDIN1-R to channel 6
–	–	–	–	0	0	1	0	SDIN2-L to channel 6
–	–	–	–	0	0	1	1	SDIN2-R to channel 6
–	–	–	–	0	1	0	0	SDIN3-L to channel 6
–	**–**	**–**	**–**	**0**	**1**	**0**	**1**	**SDIN3-R to channel 6**
–	–	–	–	0	1	1	0	Ground (0) to channel 6
–	–	–	–	0	1	1	1	No connection

DOWNMIX INPUT MULTIPLEXER REGISTER (0x21)

Bits D31–D16: Unused

Bits D15–D13: For this description, see Figure 6.

Bit D12: If 1, selects downmix data L' to TAS5086 internal channel 1

If 0, selects channel 1 data (from input multiplexer 1) to the TAS5086 internal channel 1

Bit D11: If 1, selects downmix data R' to the TAS5086 internal channel 2

If 0, selects channel 2 data (from input multiplexer 2) to the TAS5086 internal channel 2

Bit D10: If 1, selects downmix data (L'+R')/2 to the TAS5086 internal channel 5

If 0, selects channel 5 data (from input multiplexer 5) to the TAS5086 internal channel 5

Bits D9-D8: Selects either channel 6 data (from input multiplexer 6) or channel 6 data that has been processed through bass management block or downmix data (L'+R')/2 to the TAS5086 internal channel 6

Bits D7–D5: Unused.

Bit D4: If 1, enable data from input multiplexer 5 to downmix block

If 0, disable data from input multiplexer 5 to downmix block

Bit D3: If 1, enable data from input multiplexer 4 to downmix block

If 0, disable data from input multiplexer 4 to downmix block

Bit D2: If 1, enable data from input multiplexer 3 to downmix block

If 0, disable data from input multiplexer 3 to downmix block

Bit D1: If 1, enable data from input multiplexer 2 to downmix block

If 0, disable data from input multiplexer 2 to downmix block

Bit D0: If 1, enable data from input multiplexer 1 to downmix block

If 0, disable data from input multiplexer 1 to downmix block

Table 18. Downmix Input Multiplexer Register

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
–	–	–	–	–	–	–	–	**Unused**
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
–	–	–	–	–	–	–	–	**Unused**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	1	0	–	–	–	–	–	RESERVED
–	–	–	1	–	–	–	–	Enable downmix data L' to channel 1
–	**–**	**–**	**0**	**–**	**–**	**–**	**–**	**Enable channel 1 data to channel 1**
–	–	–	–	1	–	–	–	Enable downmix data R' to channel 2
–	**–**	**–**	**–**	**0**	**–**	**–**	**–**	**Enable channel 2 data to channel 2**
–	–	–	–	–	1	–	–	Enable downmix data (L'+R')/2 to channel 5
–	**–**	**–**	**–**	**–**	**0**	**–**	**–**	**Enable channel 5 data to channel 5**
–	**–**	**–**	**–**	**–**	**–**	**0**	**0**	**Enable channel 6 data to channel 6**
–	–	–	–	–	–	0	1	Bass management on channel 6
–	–	–	–	–	–	1	x	Enable downmix data (L'+R')/2 to channel 6

Table 18. Downmix Input Multiplexer Register (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	–	–	–	**1**	**Enable data from input multiplexer 1 to downmix block**
–	–	–	–	–	–	–	0	Disable data from input multiplexer 1 to downmix block
–	–	–	–	–	–	**1**	–	**Enable data from input multiplexer 2 to downmix block**
–	–	–	–	–	–	0	–	Disable data from input multiplexer 2 to downmix block
–	–	–	–	–	**1**	–	–	**Enable data from input multiplexer 3 to downmix block**
–	–	–	–	–	0	–	–	Disable data from input multiplexer 3 to downmix block
–	–	–	–	**1**	–	–	–	**Enable data from input multiplexer 4 to downmix block**
–	–	–	–	0	–	–	–	Disable data from input multiplexer 4 to downmix block
–	–	–	**1**	–	–	–	–	**Enable data from input multiplexer 5 to downmix block**
–	–	–	0	–	–	–	–	Disable data from input multiplexer 5 to downmix block

AM Mode REGISTER (0x22)

See the *PurePath Digital™ AM Interference Avoidance* application report (SLEA040).

Table 19. AM Mode Register (0x22)

D20	D19	D18	D17	D16	FUNCTION
0	**–**	**–**	**–**	**–**	**AM mode disabled**
1	–	–	–	–	AM mode enabled
–	**0**	**0**	**–**	**–**	**Select sequence 1**
–	0	1	–	–	Select sequence 2
–	1	0	–	–	Select sequence 3
–	1	1	–	–	Select sequence 4
–	**–**	**–**	**0**	**–**	**IF frequency = 455 kHz**
–	–	–	1	–	IF frequency = 262.5 kHz
–	**–**	**–**	**–**	**0**	**Use BCD tuned frequency**
–	–	–	–	1	Use binary tuned frequency

Table 20. AM Tuned Frequency Register in BCD Mode

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	X	–	–	–	–	BCD frequency (1000s kHz)
–	–	–	–	–	–	–	–	
–	–	–	–	X	X	X	X	BCD frequency (100s kHz)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	–	–	–	–	BCD frequency (10s kHz)
–	–	–	–	–	–	–	–	
–	–	–	–	X	X	X	X	BCD frequency (1s kHz)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**

OR

Table 21. AM Tuned Frequency Register in Binary Mode

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	0	X	X	X	Binary frequency
–	–	–	–	–	–	–	–	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	X	Binary frequency
–	–	–	–	–	–	–	–	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**

PWM OUTPUT MUX REGISTER (0x25)

This TAS5086 output multiplexer selects which internal PWM channel is output to which pin. Any channel can be output to any pin. The default values are used in systems with the TAS5186.

Bits D31–D25: Reserved = 0x00

Bits D23–D20: Select which PWM channel is output to PWM_1 (pin 38)

Bits D19–D16: Select which PWM channel is output to PWM_2 (pin 37)

Bits D15–D12: Select which PWM channel is output to PWM_3 (pin 36)

Bits D11–D08: Select which PWM channel is output to PWM_4 (pin 35)

Bits D07–D04: Select which PWM channel is output to PWM_5 (pin 34)

Bits D03–D00: Select which PWM channel is output to PWM_6 (pin 33)

Note that channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, …, channel 6 = 0x05.

Table 22. PWM Output Multiplex Register (0x25)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved = 0x00**
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	0	0	–	–	–	–	Multiplex channel 1 to PWM_1 (pin 38)
0	0	0	1	–	–	–	–	Multiplex channel 2 to PWM_1 (pin 38)
0	0	1	0	–	–	–	–	Multiplex channel 3 to PWM_1 (pin 38)
0	**0**	**1**	**1**	**–**	**–**	**–**	**–**	**Multiplex channel 4 to PWM_1 (pin 38)**
0	1	0	0	–	–	–	–	Multiplex channel 5 to PWM_1 (pin 38)
0	1	0	1	–	–	–	–	Multiplex channel 6 to PWM_1 (pin 38)
–	–	–	–	0	0	0	0	Multiplex channel 1 to PWM_2 (pin 37)
–	–	–	–	0	0	0	1	Multiplex channel 2 to PWM_2 (pin 37)
–	**–**	**–**	**–**	**0**	**0**	**1**	**0**	**Multiplex channel 3 to PWM_2 (pin 37)**
–	–	–	–	0	0	1	1	Multiplex channel 4 to PWM_2 (pin 37)
–	–	–	–	0	1	0	0	Multiplex channel 5 to PWM_2 (pin 37)
–	–	–	–	0	1	0	1	Multiplex channel 6 to PWM_2 (pin 37)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	0	0	0	–	–	–	–	Multiplex channel 1 to PWM_3 (pin 36)
0	0	0	1	–	–	–	–	Multiplex channel 2 to PWM_3 (pin 36)
0	0	1	0	–	–	–	–	Multiplex channel 3 to PWM_3 (pin 36)
0	0	1	1	–	–	–	–	Multiplex channel 4 to PWM_3 (pin 36)
0	**1**	**0**	**0**	**–**	**–**	**–**	**–**	**Multiplex channel 5 to PWM_3 (pin 36)**
0	1	0	1	–	–	–	–	Multiplex channel 6 to PWM_3 (pin 36)
–	–	–	–	0	0	0	0	Multiplex channel 1 to PWM_4 (pin 35)
–	–	–	–	0	0	0	1	Multiplex channel 2 to PWM_4 (pin 35)
–	–	–	–	0	0	1	0	Multiplex channel 3 to PWM_4 (pin 35)
–	–	–	–	0	0	1	1	Multiplex channel 4 to PWM_4 (pin 35)
–	–	–	–	0	1	0	0	Multiplex channel 5 to PWM_4 (pin 35)
–	**–**	**–**	**–**	**0**	**1**	**0**	**1**	**Multiplex channel 6 to PWM_4 (pin 35)**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	–	–	–		Multiplex channel 1 to PWM_5 (pin 34)
0	**0**	**0**	**1**	**–**	**–**	**–**	**–**	**Multiplex channel 2 to PWM_5 (pin 34)**
0	0	1	0	–	–		–	Multiplex channel 3 to PWM_5 (pin 34)
0	0	1	1	–	–		–	Multiplex channel 4 to PWM_5 (pin 34)
0	1	0	0	–		–	–	Multiplex channel 5 to PWM_5 (pin 34)
0	1	0	1	–	–	–	–	Multiplex channel 6 to PWM_5 (pin 34)
–	**–**	**–**	**–**	**0**	**0**	**0**	**0**	**Multiplex channel 1 to PWM_6 (pin 33)**
–	–	–	–	0	0	0	1	Multiplex channel 2 to PWM_6 (pin 33)
–	–	–	–	0	0	1	0	Multiplex channel 3 to PWM_6 (pin 33)
–	–	–	–	0	0	1	1	Multiplex channel 4 to PWM_6 (pin 33)
–	–	–	–	0	1	0	0	Multiplex channel 5 to PWM_6 (pin 33)
–	–	–	–	0	1	0	1	Multiplex channel 6 to PWM_6 (pin 33)

APPENDIX A. TAS5086 APPLICATIONS

For detailed application information, see the *TAS5086-5186V6EVM* application report (SLEA054).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN200608044	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TAS5086 B	Samples
TAS5086DBT	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TAS5086 B	Samples
TAS5086DBTG4	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TAS5086 B	Samples
TAS5086DBTR	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TAS5086 B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

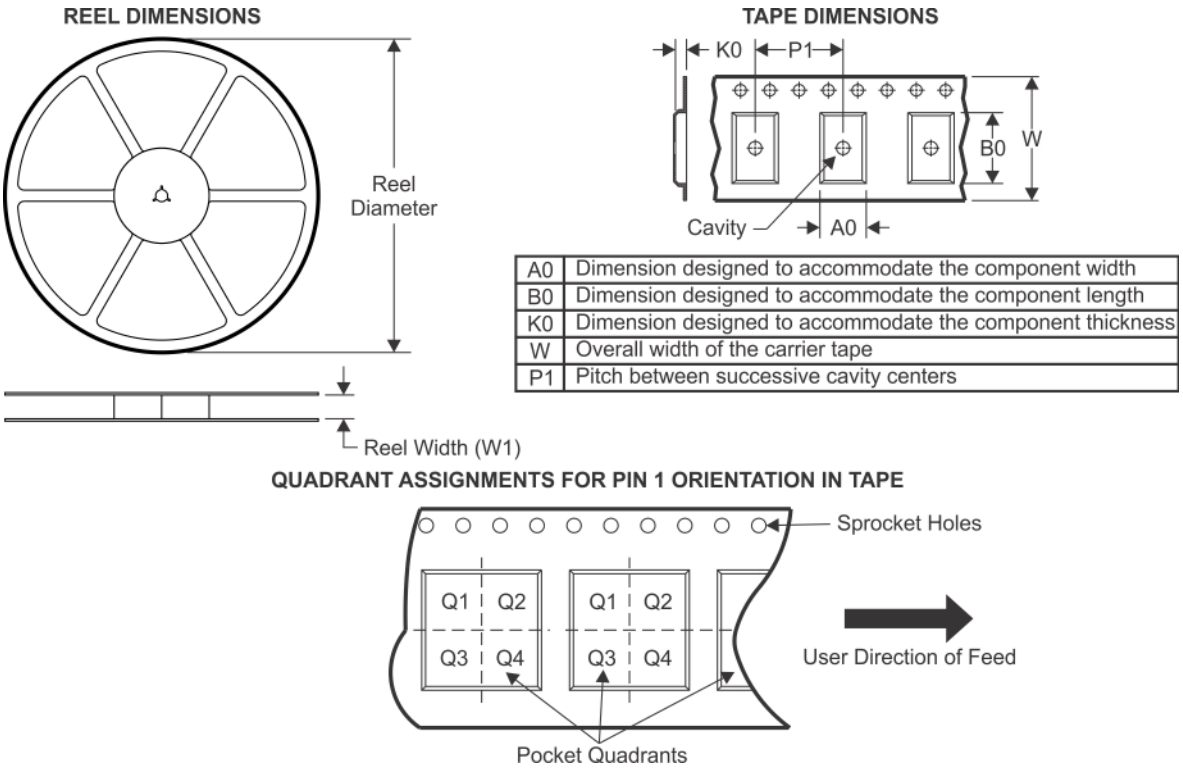
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

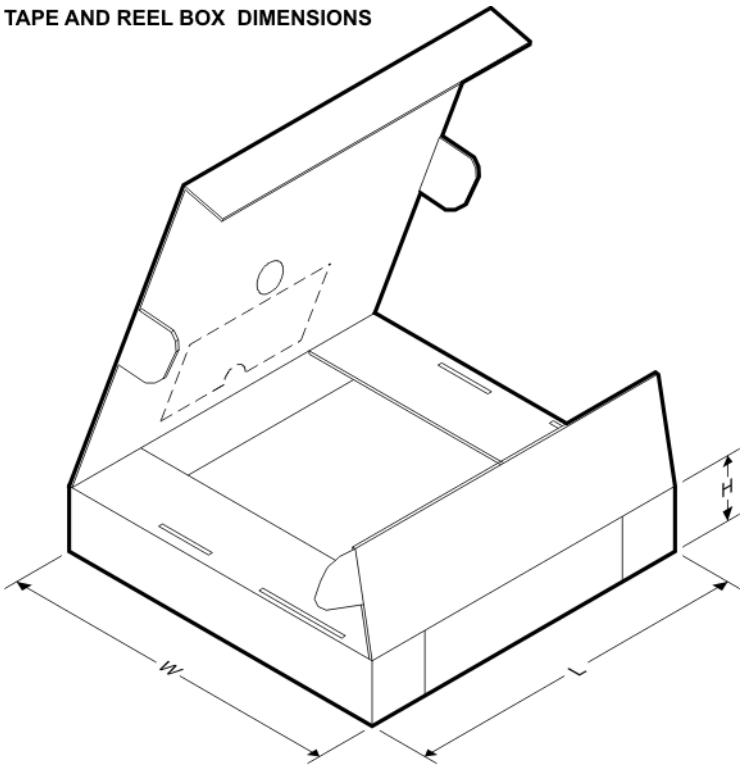


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5086DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

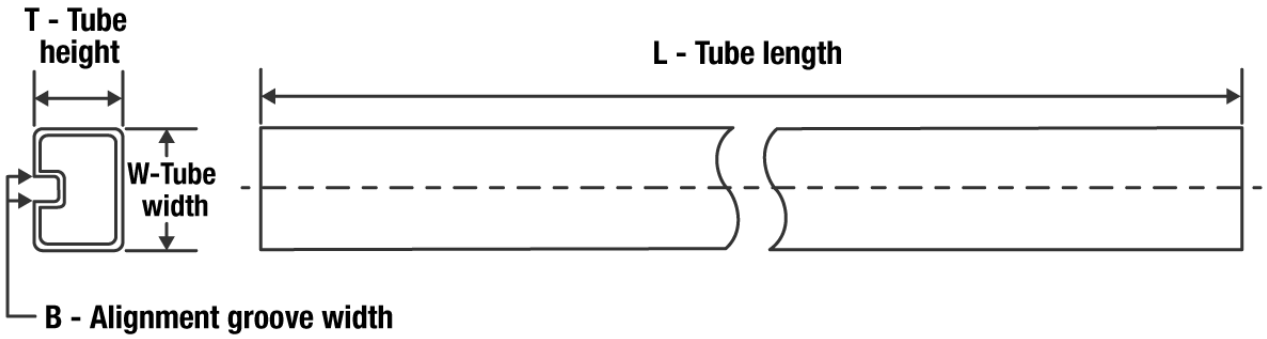
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5086DBTR	TSSOP	DBT	38	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

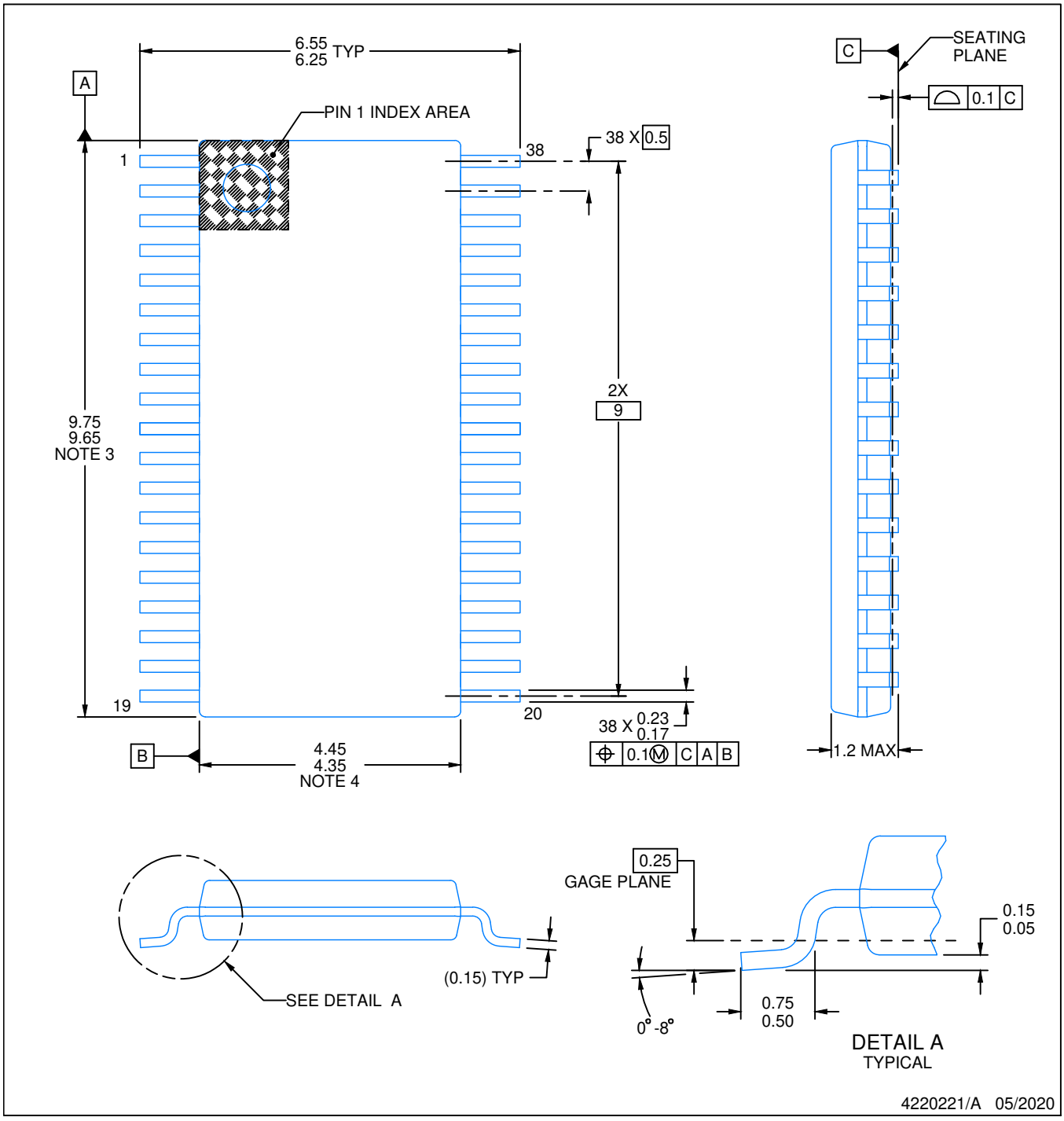
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS5086DBT	DBT	TSSOP	38	50	530	10.2	3600	3.5
TAS5086DBTG4	DBT	TSSOP	38	50	530	10.2	3600	3.5

PACKAGE OUTLINE

DBT0038A

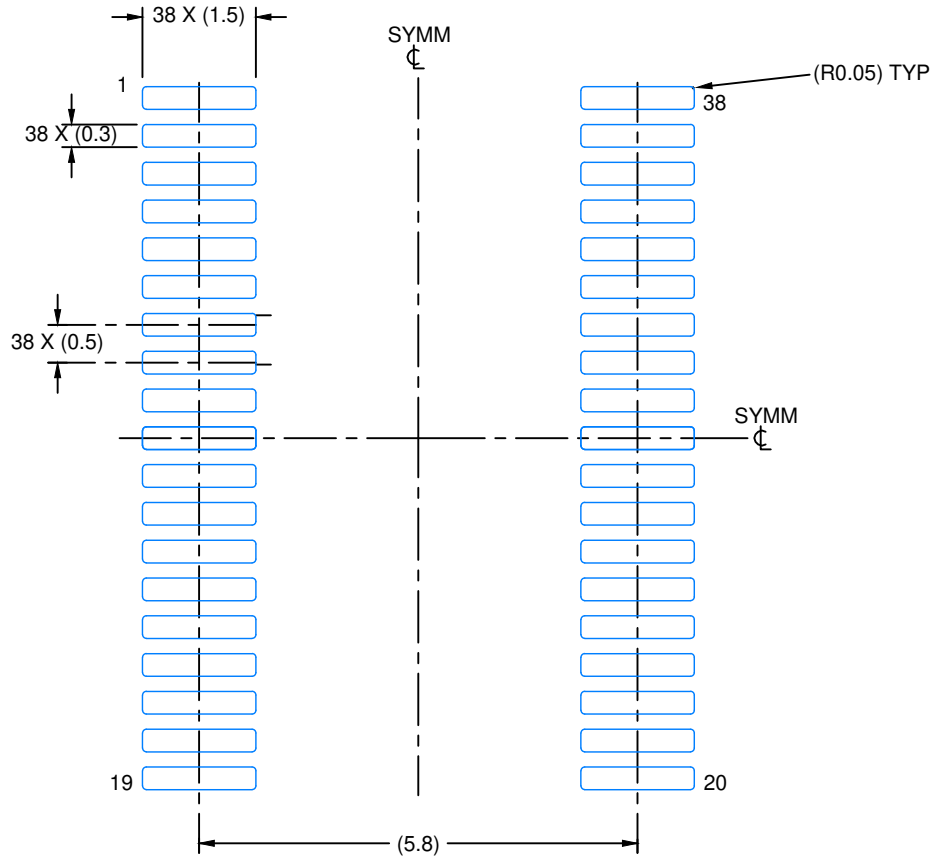
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

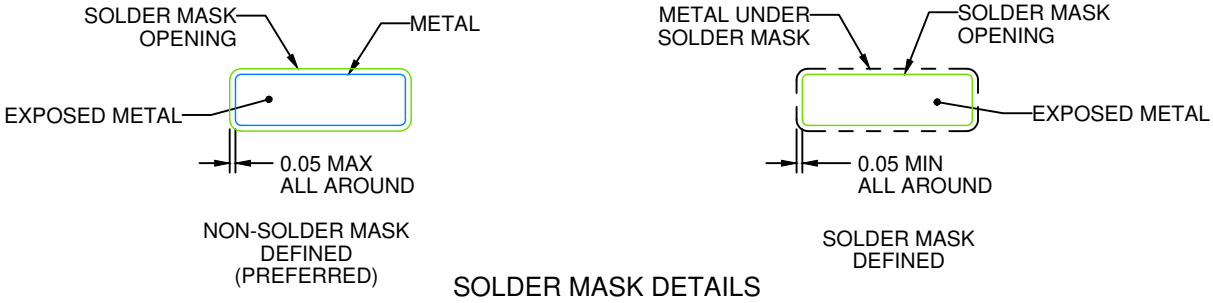


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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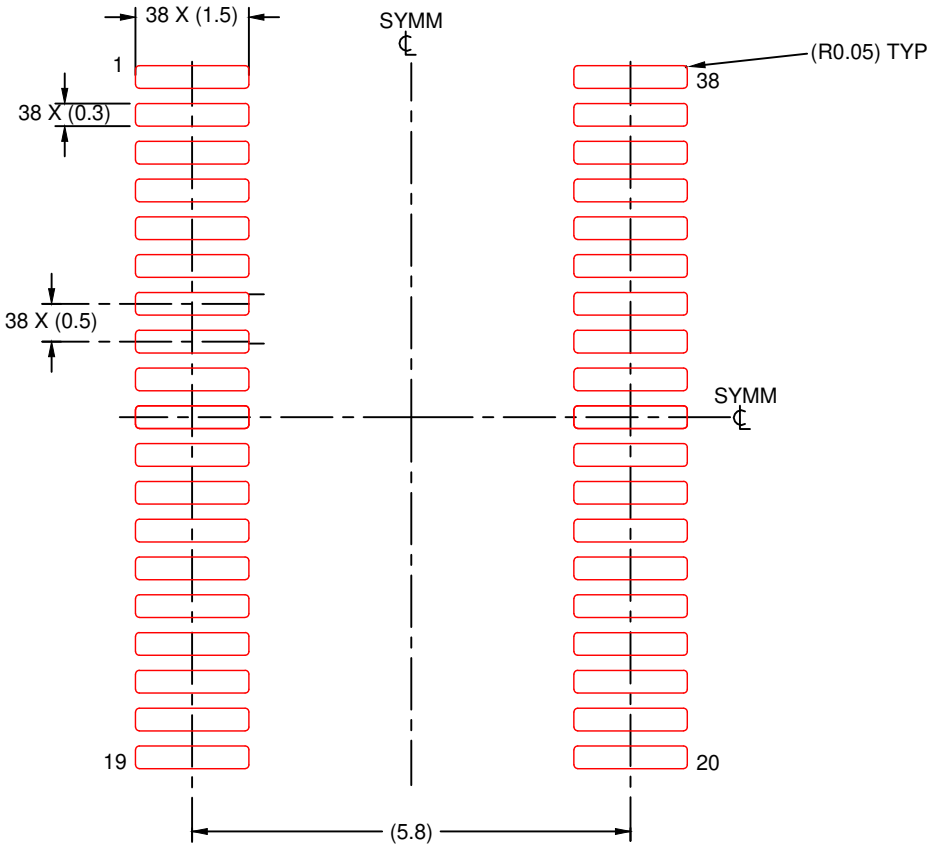
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220221/A 05/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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