40Gbit/s QSFP-QSFP AOC
ICD040GVP1630-XY, ICD040GVP163D-XY

FEATURES

- Full duplex 4 channel 850nm parallel active optical cable
- Transmission data rate up to 10.3Gbit/s per channel
- SFF-8436 QSFP+ compliant housing and hot pluggable electrical interface.
- Management Interface and digital diagnostic monitoring (DDM) through I2C
- Support Rx output pre-emphasis
- 4ch 850nm VCSEL array
- 4ch PIN photo detector array
- Helix type multi-mode optical fibre cable of up to 100m
- OFNP (Optical Fibre Non-Conductive Plenum) rated cable
- Differential AC-coupled high speed data interface
- Low power consumption of typical 0.8W per end
- Housing isolated from connector ground
- Easy to use release mechanism
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant
- Laser Class 1

APPLICATIONS

- Infiniband transmission at 4ch SDR(2.5Gbit/s), DDR(5Gbit/s) and QDR(10Gbit/s)
- Multi-channel 10Gb Ethernet transmission up to 4 channels
- Fiber Channel transmission at 8.5Gbit/s per channel, up to 4 channels

SUPPORTED STANDARDS

- SFF-8436 QSFP+
- Infiniband IB-4x-SDR-SX, IB-4x-DDR-SX, IB-4x-QDR-SX
- Ethernet 40GBASE-SR4

Scope

This specification describes the performance characteristics of the 40Gbps FCI QSFP+ Active Optical Cable (AOC).

The status of this document is preliminary.

Product Description

FCI QSFP+ AOC is a hot pluggable active optical cable for full duplex high speed data interconnections up to 40 Gbit/s. Each end of the active optical cable is terminated into an electro optical transceiver module.

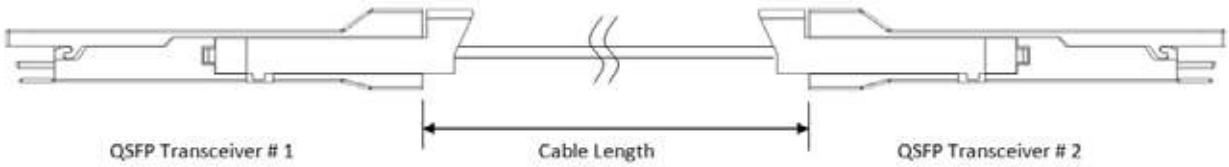


Figure 1 Principle of Cable Assembly

The receiving end of the Transceiver Module comprises of a Quad Transimpedance / Limiting Amplifier (TIA/LIA). Through the Optical Coupling Unit (CU), parallel incoming optical data signals are directed to the PIN diode array and in combination with the TIA/LIA, converted to parallel electrical data signals.

The transmitting end of the Transceiver Module comprises of a Quad Laser Driver, parallel electrical signals from the HOST board modulate a 850nm VCSEL laser array which, in turn, generates parallel optical data signals to be launched into the AOC.

Both receiver output buffer and transmitter input buffer support CML compatible data bus. All differential data lines are AC coupled and matched for 100 Ohm operation.

The on-board microcontroller provides a serial two wire interface and handles the low speed signals applied at the electrical edge connector.

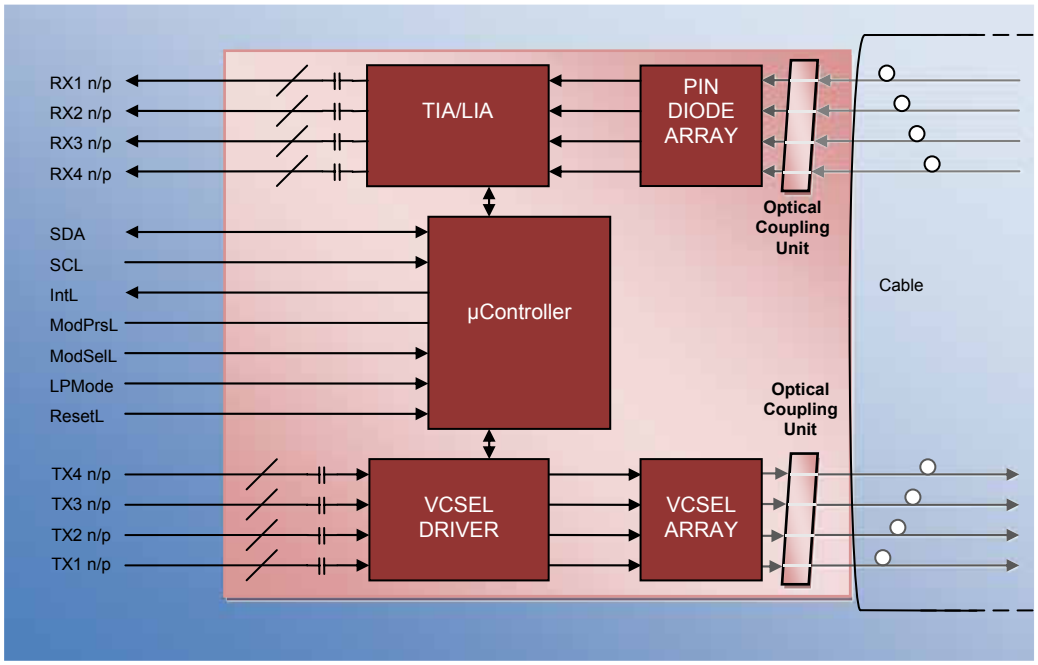


Figure 2 Block Diagram of one of the QSFP End Module

Reference

Industry Documents

- SFF-8436 Revision 3.5
- Infiniband™ Architecture Volume 2-2006 Chapter 6
- IEEE-802.3ba -2010
- IEC 60825-1 Laser Class 1
- 21 CFR 1040.10 Laser Class 1
- RoHS-6 (lead-free)
- IEC 60950-1
- JEDEC JESD22-A114-B
- EN 61000-4-2 ESD Immunity
- EN 61000-4-3 EMI Immunity
- EN 55022 Class B (FCC Part 15 Class B)

Electrical Connector

Figure 3 shows the contact numbering and signals for the 38pin QSFP AOC Module edge connector compliant to SFF-8436 Specification.

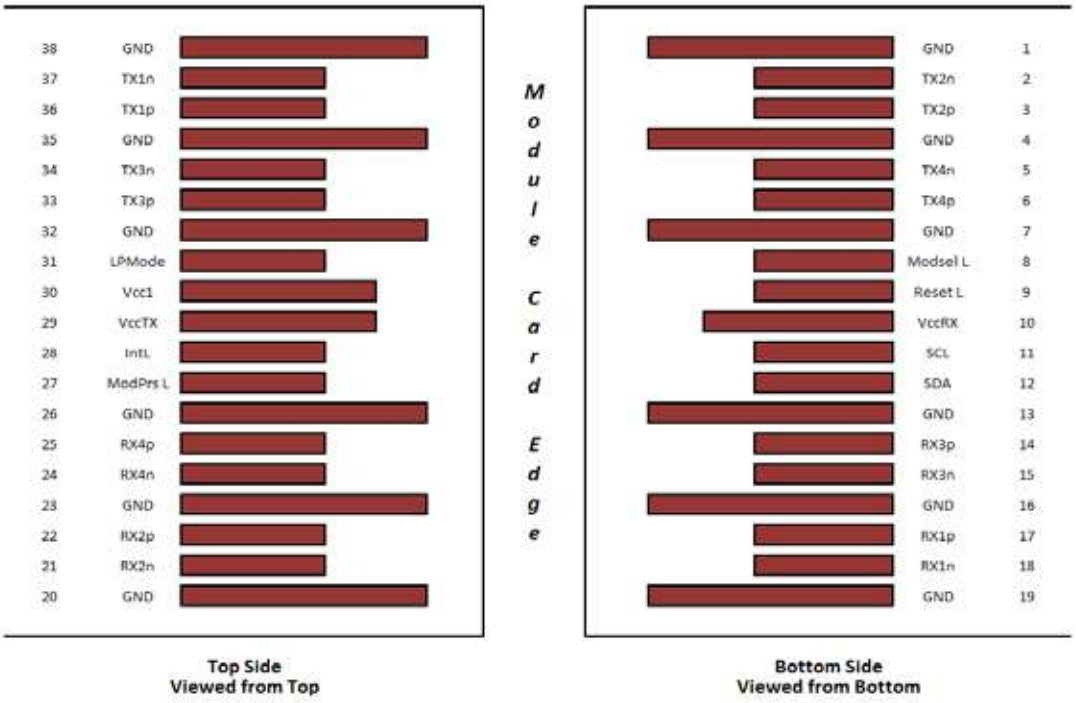


Figure 3 Edge Connector Pad Layout

Pinning Function Definition

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input, AC coupled
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input, AC coupled
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input, AC coupled
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input, AC coupled
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select, pulled up with 10kOhm inside module
9	LVTTL-I	ResetL	Module Reset, pulled up with 10kOhm inside module
10		Vcc Rx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-wire serial interface clock, place 4.7kΩ -10kΩ Pull up Resistor to +3.3V on Host board
12	LVCMOS-I/O	SDA	2-wire serial interface data, place 4.7kΩ -10kΩ Pull up Resistor to +3.3V on Host board
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output, AC coupled
15	CML-O	Rx3n	Receiver Inverted Data Output, AC coupled
16		GND	Ground
17	CML-O	Rxlp	Receiver Non-Inverted Data Output, AC coupled
18	CML-O	RxIn	Receiver Inverted Data Output, AC coupled
19		GND	Ground

Table 1 Pin Function Definition for Bottom Side of Edge Connector

Pin	Logic	Symbol	Description
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output, AC coupled
22	CML-O	Rx2p	Receiver Non-Inverted Data Output, AC coupled
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output, AC coupled
25	CML-O	Rx4p	Receiver Non-Inverted Data Output, AC coupled
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present, place 4.7kΩ -10kΩ Pull up Resistor to +3.3V on Host board
28	LVTTL-O	IntL	Interrupt, place 4.7kΩ -10kΩ Pull up Resistor to +3.3V on Host board
29		Vcc Tx	+3.3V Power supply transmitter
30		Vccl	+3.3V Power supply
31	LVTTL-I	LPMode	Low Power Mode, pulled up with 10kOhm inside module
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input, AC coupled
34	CML-I	Tx3n	Transmitter Inverted Data Input, AC coupled
35		GND	Ground
36	CML-I	Txlp	Transmitter Non-Inverted Data Input, AC coupled
37	CML-I	TxIn	Transmitter Inverted Data Input, AC coupled
38		GND	Ground

Table 2 Pin Function Definition for Top Side of Edge Connector

Electrical Hardware Pin Description

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", module does not respond to 2-wire interface communication from the host. ModSelL has an internal pull-up resistor inside the module.

ResetL Pin

A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.
Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host disregards all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.
ResetL has an internal pull-up resistor inside the module.

LPMode Pin

FCI QSFP+ modules always operate in the low power mode (Power class 1), thus, this pin has no function.

ModPrsL Pin

Pin is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When the out put is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Absolute Maximum Ratings

Exceeding one or more of these values may cause permanent damage.

Parameter	Conditions	Symbol	Min	Max	Units
Storage temperature		ϑ_{St}	-25	75	°C
Powered case temperature range	Non-condensing	ϑ_{C}	-5	70	°C
Relative Humidity		RH	5	85	%
Power supply voltage at 3.3V		V_{CC1}	-0.3	3.63	V
Voltage on Low Speed Inputs		V_{IN}	-0.3	3.63	V
Two wire Sink Current		I_{SINK}		10	mA
DC voltage at High Speed Pins	At hot plugging	V_D	V_{cc1}-0.5	V_{cc1}+0.5	V
Differential Input Swing		v_{DDI}		1.6	V_{pp}
Static discharge voltage on low-speed signal and power pins	Human body model per JEDEC JESD22-A114-B			2000	V
Static discharge voltage on high speed signal pins	Charged device model per JEDEC JESD22-C101C			500	V
	Human body model per JEDEC JESD22-A114-B			500	V
Air discharge to housing	EN61000-4-2 Criterion B Test			15	kV
Contact discharge to housing	EN61000-4-2 Criterion B Test			8	kV

Table 3 Absolute Maximum Ratings

Recommended Operating Conditions

Unless otherwise noted under the recommended operating condition range.
Module operates with factory default settings.

Parameter	Conditions	Symbol	Min	Typ.	Max	Units
Case temperature		ϑ_C	0	35	70	°C
3.3V Supply Voltage		V_{CC1}	3.135	3.3	3.465	V
Power supply noise including ripples	1kHz to frequency of operation at input of recommended supply filter	v_{CCAC}			50	mV_{pp}
Data rate per lane	8B/10B Data Line Coding (Infiniband)	DR	2.5	10	10.5	GBd
	64B/66B Data Line Coding (Ethernet)	DR	8	10	10.5	GBd
Differential AC Data Input Swing	Differential Peak-to-Peak-Amplitude, at TP6	v_{DDI}	250		1200	mV_{pp}
Common Mode Input Voltage	RMS Value of frequency range 1kHz to frequency of operation, at TP6	V_{ACCM}			25	mV
Deterministic Input Jitter	PRBS7, per lane, at TP6	J_{D1I}			0.15	UI
Total Input Jitter	Peak-to-peak, 10^{-12}-points, PRBS7, per lane, at TP6	J_{T1I}			0.3	UI

Table 4 General Operating Conditions

Electrical Characteristics

General Electrical Characteristics

Unless otherwise noted under the recommended operating condition range.
Module operates with factory default settings.

Parameter	Conditions	Symbol	Min	Typ.	Max	Units
Power Consumption per Plug	factory default settings	P_{Plug}		0.8	1.2	W
Power Consumption End to End	factory default settings	P_{AOC}		1.6	2.4	W
3.3V-Supply Current Tx	factory default settings	I_{CCTx}		0.08	0.13	A
3.3V-Supply Current Rx	factory default settings	I_{CCRx}		0.16	0.21	A

Table 5 General Electrical Characteristics

Data Input Characteristics

Unless otherwise noted under the recommended operating condition range and referred according to Infiniband specification at TP5. All high speed lines are AC- coupled.
Module operates with factory default settings.

Parameter	Conditions		Symbol	Min	Typ	Max	Units
Differential Termination Resistance	per lane		R_{Idiff}	85	100	115	Ω
Data Input Coupling Capacitance	per lane		C_K	64	100	144	nF
Differential Input Return Loss	Referred to R_G=100Ω	f=1MHz…100MHz	S_{d11}			-10	dB
		f=100MHz…4,1GHz				$-12+2\sqrt{\frac{f}{11GHz}}$	dB
		f=4,1GHz…11,1GHz				$-6.5+13.3\log\frac{f}{5.5GHz}$	dB
Common Mode Return Loss	R_G=25Ω; f=100MHz…7.5GHz		S_{CC11}			-6	dB
Mode Conversion	Common to Differential Conversion; f=100MHz…7.5GHz		S_{CD11}			-20	dB

Table 6 Data Input Characteristics

Data Output Characteristics

Unless otherwise noted under the recommended operating condition range and measured at TP7 referred to Infiniband Annex 6. All high speed lines are AC- coupled.
Module operates with factory default settings.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Differential Termination Resistance	per lane	R_{Idiff}	85	100	115	Ω
Output Coupling Capacitance	per lane	C_K	64	100	144	nF
Differential Output Voltage	100Ω differentially terminated, factory setting	v_{DDO}	350	580	800	mV_{pp}
	Output Squelch active	v_{DDOq}			50	mV_{pp}
AC-Common Mode Output Voltage	100Ω differential terminated, RMS				25	mV
Rise/Fall Time	20% to 80%	t_{r28}; t_{f28}	28			ps
Deterministic Jitter	per lane	J_{DO}			0.4	UI
Total Jitter	Peak-to-Peak Value, 10^{-12}-Jitter, per lane	J_{TO}			0.72	UI

Table 7 Output Characteristics

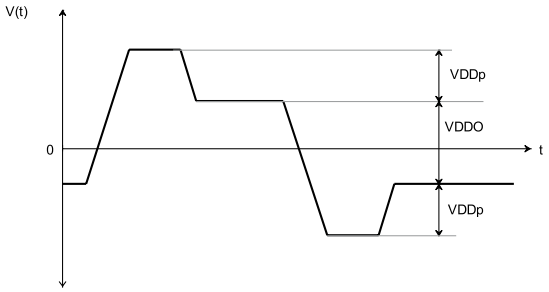


Figure 4 Differential Cable Output Signal

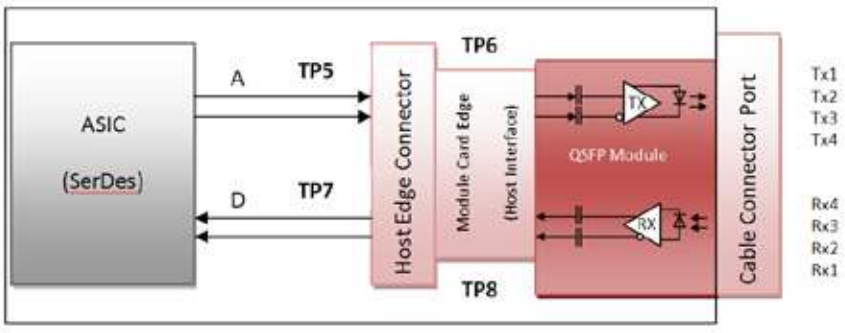


Figure 5 Reference Points

Low Speed Electrical Specification

Parameter	Conditions	Symbol	Min	Typ	Max	Units
ResetL, ModSelL, LPMode	$\|I_{in}\|$ <= 125µA for 0V< V_{in} < Vcc	V_{IL}	-0.3		0.8	V
		V_{IH}	2		Vcc+ 0.3	V
ModPRSL, IntL	I_{OL} = 2mA	V_{OL}	0		0.4	V
		V_{OH}	Vcc – 0.5		Vcc +0.3	V
SCL, SDA		V_{IL}	-0.3		Vcc*0.3	V
		V_{IH}	Vcc*0.7		Vcc +0.5	V
SCL, SDA	I_{OL}(max) = 3mA	V_{OL}	0		0.4	V
		V_{OH}	Vcc-0.5		Vcc+0.3	V
Capacitance for SCL and SDA I/O Pin		C_i			14	pF
Total bus capacitive load for SCL and SDA	3.0kΩ Pullup resistor, max				100	pF
	1.6kΩ Pullup resistor, max				200	pF

Table 8 Low Speed Electrical Specification

Host Board Power Supply Filtering

Host Board should use the power supply filtering shown in Figure 6.

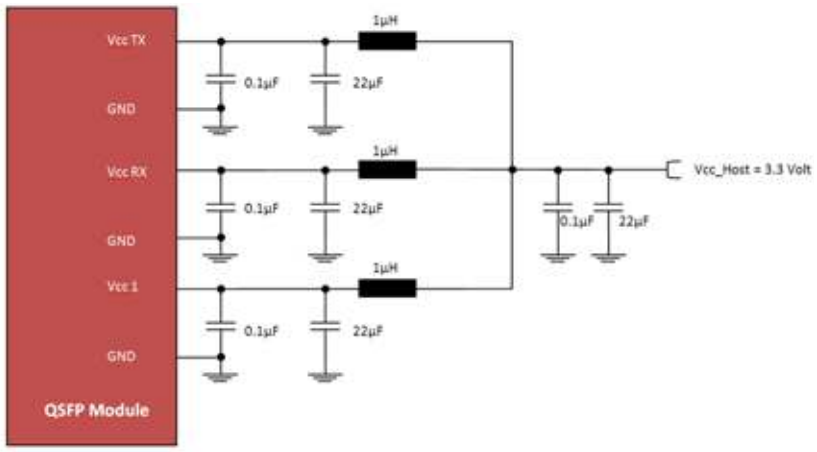


Figure 6 Recommended Host Power Supply Filtering

General Cable Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Propagation Delay Time	For informational purposes only	tP		5		ns/m
Cable Skew	Absolute skew between any individual channel, w/o any input skew	Δtpd			1	ns
Cable Diameter				3		mm
Min. Bend radius while service		rInst_min		45		mm
Min. Operational Bend radius		rmin		30		mm
Cable length Range	Supported length range	l	5		100	m
Cable length	5m Cable	l	4.9	5	5.4	m
	10m Cable	l	9.85	10	10.4	m
	20m Cable	l	19.5	20	20.5	m
	50m Cable	l	49.4	50	51	m
	100m Cable	l	98.5	100	102	m
Plug Insertion Force		FI	0		40	N
Plug Extraction Force		FE	0		30	N
Plug Retention Force	No damage below 90N	FR	90		N/A	N
Plug Insertion/ removal cycles		n	50		N/A	Cycles

Table 9 General Cable Characteristics

1) For Definition of Cable Length see. Specific Cable Lengths within specified range are orderable. Shown cable lengths are available standard lengths.
2) Specified values are met when QSFP compliant plug receptacles/cages are used.

Serial Interface

Two wire Memory Map

FCI QSFP+ AOC supports the memory mapping defined in SFF-8436. Memory space is organised into one lower page (Register Address 0-127) and three upper pages (Register Address 128-255).

2wire serial address is A0h (1010 000x)

Register	Field	Bytes
0-2	ID and Status	2
3-21	Interrupt Flags	19
22-33	Module Monitors	12
34-81	Channel Monitors	48
82-85	Reserved	4
86-97	Control	12
98-99	Reserved	2
100-106	Module and Channel Mask	7
107-118	reserved	12
119-122	Password Change Entry Area (Optional)	4
123-126	Password Change Area (Optional)	4
127	Page Select Byte	1

Page 00

Register	Field	Bytes
128-191	Basic ID Fields	64
192-223	Extended ID	32
224-255	Vendor Specific ID	32

Page 02

Register	Field	Bytes
128-255	User Data	128

Page 03

Register	Field	Bytes
128-175	Module Threshold	48
176-223	Channel Threshold	48
224-225	Reserved	2
226-241	Vendor Specific Channel Controls	16
242-253	Channel Monitor Masks	12
254-255	Reserved	2

Figure 7 Two wire Memory Map

Lower Page 00 Description

Default Register Content is '00h' unless noted otherwise.
'r' stands for Read Only Register and 'r/w' stands for Read/Writeable Register.

ID and Status

Byte	Bit	Name	r/w	Description
0	All	Identifier	r	0Dh = QSFP+
1	All	Reserved	r	
2	7	Reserved	r	
	6	Reserved	r	
	5	Reserved	r	
	4	Reserved	r	
	3	Reserved	r	
	2	Flat_Mem	r	'0' = Paging
	1	IntL	r	Digital state of the IntL Interrupt output pin
	0	Data_Not Ready	r	Indicates Module has not yet achieved power up and memory data is not ready. Bit remains high until data is ready to be read at which time the device sets the bit low.

Table 10 Lower Page 00 ID and Status

Interrupt Flags Channel/Module

Byte	Bit	Name	r/w	Description
3	7-4	Reserved	r	
	3	L_Rx4 LOS	r	Latched RX LOS indicator, channel 4
	2	L_Rx3 LOS	r	Latched RX LOS indicator, channel 3
	1	L_Rx2 LOS	r	Latched RX LOS indicator, channel 2
	0	L_Rx1 LOS	r	Latched RX LOS indicator, channel 1
4	7-4	Reserved	r	
	3	L_Tx4 Fault	r	Latched TX fault indicator, channel 4
	2	L_Tx3 Fault	r	Latched TX fault indicator, channel 3
	1	L_Tx2 Fault	r	Latched TX fault indicator, channel 2
	0	L_Tx1 Fault	r	Latched TX fault indicator, channel 1
5		Reserved	r	
6	7	L-Temp High Alarm	r	Latched high Temperature alarm
	6	L-Temp Low Alarm	r	Latched low Temperature alarm
	5	L-Temp High Warning	r	Latched high Temperature warning
	4	L-Temp Low Warning	r	Latched low Temperature warning
	3-0	Reserved	r	
7	7	L-VCC High Alarm	r	Latched high supply voltage alarm
	6	L-VCC Low Alarm	r	Latched low supply voltage alarm
	5	L-VCC High Warning	r	Latched high supply voltage warning
	4	L-VCC Low Warning	r	Latched low supply voltage warning
	3-0	Reserved	r	
8	All	Vendor Specific	r	
9-18	All	Reserved	r	
19-21	All	Vendor Specific	r	

Table 11 Lower Page 00 Interrupt Flags Channel/Module

Real Time Monitoring Values

Byte	Bit	Name	r/w	Description
22	All	Temperature MSB	r	Internally measured module Temperature
23	All	Temperature LSB	r	
24-25	All	Reserved	r	
26	All	Supply Voltage MSB	r	Internally measured module supply voltage
27	All	Supply Voltage LSB	r	
28-85	All	Reserved / Vendor Specific	r	

Table 12 Lower Page 00 Real Time Monitoring Values

Control Bytes

Byte	Bit	Name	r/w	Description
86	7-4	Reserved	r/w	
	3	Tx4 Disable	r/w	'1' disables the laser, channel 4
	2	Tx3 Disable	r/w	'1' disables the laser, channel 3
	1	Tx2 Disable	r/w	'1' disables the laser, channel 2
	0	Tx1 Disable	r/w	'1' disables the laser, channel 1
87-92	All	Reserved	r	
93	7-2	Reserved	r/w	
	1	Power Set	r/w	Since module always running in low power mode (Power Class 1) setting of these bits does not have any effect
	0	Power Override	r/w	
94-99	All	Reserved	r/w	

Table 13 Lower Page 00 Control Bytes

IntL Masking Bits for Module and Channel Status Interrupts

Byte	Bit	Name	r/w	Description
100	7-4	Reserved	r/w	
	3	M-Rx4 LOS	r/w	Masking bit for Rx LOS indicator, channel 4
	2	M-Rx3 LOS	r/w	Masking bit for Rx LOS indicator, channel 3
	1	M-Rx2 LOS	r/w	Masking bit for Rx LOS indicator, channel 2
	0	M-Rx1 LOS	r/w	Masking bit for Rx LOS indicator, channel 1
101	7-4	Reserved	r/w	
	3	M-Tx4 Fault	r/w	Masking bit for Tx Fault Indicator, channel 4
	2	M-Tx3 Fault	r/w	Masking bit for Tx Fault Indicator, channel 3
	1	M-Tx2 Fault	r/w	Masking bit for Tx Fault Indicator, channel 2
	0	M-Tx1 Fault	r/w	Masking bit for Tx Fault Indicator, channel 1
102	All	Reserved	r/w	
103	7	M-Temp High	r/w	Masking bit for high Temperature alarm
	6	M-Temp Low	r/w	Masking bit for low Temperature alarm
	5	M- Temp High Warning	r/w	Masking bit for high Temperature warning
	4	M-Temp Low Warning	r/w	Masking bit for low Temperature warning
	3-0	Reserved	r/w	
104	7	M-Vcc High alarm	r/w	Masking bit for high Vcc alarm
	6	M-Vcc Low alarm	r/w	Masking bit for low Vcc alarm
	5	M-Vcc High Warning	r/w	Masking bit for high Vcc warning
	4	M-Vcc Low Warning	r/w	Masking bit for low Vcc warning
	3-0	Reserved	r/w	
105-118	All	Reserved/ Vendor Specific	r/w	
119-122	32	Password Change	w	Password Change Entry Area
123-126	32	Password	w	Password Entry Area

Table 14 Lower Page 00 Masking Bits

Page Select

Byte	Bit	Name	r/w	Description
127	All	Page Select	r/w	'00h'= Upper page 0 '02h'= Upper page 2 '03h'= Upper page 3

Table 15 Lower Page 00 Page Select

Upper Page 00 Description

'r' stands for Read Only Register and 'r/w' stands for Read/Writeable Register.

Memory Map Upper Page 00

Dec	HEX	Byte	Name	Description	r/w	HEX	DEC	ASCII	Comment
128	80	1	identifer value	QSFP+ = 0Dh	r	D	13		
129	81	1	ext. Identifer	Power Class 1 = '0'	r	0	0		
130	82	1	Connector	No separable connector =23h	r	23	35		
131	83	8	Module	40GBase-SR4 = 04h	r	4	4		
132	84			Sonet Compliance Code	r	0	0		
133	85			SAS/SATA Compliance Code	r	0	0		
134	86			Gigabit Ethernet Compliance Code	r	0	0		
135	87			Fibre Channel Link Length	r	0	0		
136	88			Fibre Channel Transmitter Technology	r	0	0		
137	89			Fibre Channel Transmission Media	r	0	0		
138	8A			Fibre Channel Speed	r	0	0		
139	8B	1	Encoding	Code Description of encoding mechanism 00h Unspecified 01h 8B10B 02h 4B5B **03h NRZ** 04h SONET Scrambled 05h 64B66B 06h Manchester 07h-FFh Reserved	r	3	3		
140	8C	1	BR, nominal	10.00 Gbit/s	r	64	100		Data rate in 100Mbit/s
141	8D	1	Extended	Rate Select	r	0	0		
142	8E	1	Length(SMF) m		r	0	0		not specified
143	8F	1	Length(50µ) m	with OM3 fiber	r	0	0		
144	90	1	Length(50µ) m	with OM2 fiber	r	0	0		not specified
145	91	1	Length(62.5µ) m	with OM1 fiber	r	0	0		not specified
146	92	1	Length (Copper)	eg. 0Ah,32h,64h	r				Cable length in meters
147	93	1	Device Tech	Pin,VCSEL@850nm,uncooled no wavelength control = 00h	r	0	0		

Table 16 Upper Page 00 Description 128-147

Dec	HEX	Byte	Name	Description	r/w	HEX	DEC	ASCII	Comment
148	94	16	Vendor name		r	46	70	F	
149	95				r	43	67	C	
150	96				r	49	73	I	
151	97				r	20	32		
152	98				r	4D	77	M	
153	99				r	65	101	e	
154	9A				r	72	114	r	
155	9B				r	67	103	g	
156	9C				r	65	101	e	
157	9D				r	4F	79	O	
158	9E				r	70	112	p	
159	9F				r	74	116	t	
160	A0				r	69	105	i	
161	A1				r	63	99	c	
162	A2				r	73	115	s	
163	A3				r	20	32		
164	A4	1	Extended Module	Supports SDR,DDR and QDR	r	7	7		
165	A5	3	Vendor OUI	FCI Merge Optics OUI = 00-0A-0D	r	0	0		IEEE based OUI
166	A6				r	A	10		
167	A7				r	D	13		
168	A8	16	Vendor PN	Product Type	r	49	73	I	IC = Interconnect D= Duplex 040G= 40Gbit/s V = VCSEL P = Photodiode
169	A9				r	43	67	C	
170	AA				r	44	68	D	
171	AB				r	30	48	0	
172	AC				r	34	52	4	
173	AD				r	30	48	0	
174	AE				r	47	71	G	
175	AF				r	56	86	V	
176	B0				r	50	80	P	
177	B1			Product Generation	r	31	49	1	
178	B2			Optical Standard	r	36	54	6	
179	B3			Electrical or MSA	r	33	51	3	
180	B4				r	30	48	0	0 = without DDM D = with DDM
181	B5			*Cable length (in meters)*	r	20	32	-	XY
182	B6				r	20	32	X	
183	B7				r	20	32	Y	

Table 17 Upper Page 00 Description 148-183

Dec	HEX	Byte	Name	Description	r/w	HEX	DEC	ASCII	Comment
184	B8	2	Vendor rev	FCI Revision Code	r				
185	B9				r				
186	BA	2	Wavelength	850	r	42	66		
187	BB				r	68	104		
188	BC	2	Wavelength Tol	10	r	7	7		
189	BD				r	D0	208		
190	BE	1	Max Case Temp	70°C = 70 = 46h	r	46	70		
191	BF	1	CC_Base	Check Code, low order 8 bits of sum of register 128 to 190	r				
192	C0	4	Options	Reserved	r	0	0		
193	C1				r	1	1		Rx output amplitude programming supported
194	C2				r	4	4		RxOutput Disable supported
195	C3				r	98	152		TxDisable,TxFault, Memory Page 02 supported
196	C4	16	Vendor SN	Serial Number in ASCII code	r				Variable
197	C5				r				
198	C6				r				
199	C7				r				
200	C8				r				
201	C9				r				
202	CA				r				
203	CB				r				
204	CC				r				
205	CD				r				
206	CE				r				
207	CF				r				
208	D0				r				
209	D1				r				
210	D2				r				
211	D3				r				

Table 18 Upper Page 00 Description 184-211

Dec	HEX	Byte	Name	Description	r/w	HEX	DEC	ASCII	Comment
212	D4	8	Date Code	ASCII code, YEAR	r				Content depends on manufaturing date
213	D5				r				
214	D6			ASCII code, MONTH	r				
215	D7				r				
216	D8			ASCII code, Day	r				
217	D9				r				
218	DA			ASCII code, vendor specific lot code, may be uses 20h ('ASCII space')	r				
219	DB				r				
220	DC	1	Diag. Mon. Type		r	0	0		
221	DD	1	Enhanced options		r	0	0		
222	DE	1	Reseved		r	0	0		
223	DF	1	CC_EXT	Check Code, low order 8 bits of sum of register 192 to 222	r	0	0		
224	E0	32	Vendor Spec		r	0	0		
225	E1				r	0	0		
226	E2				r	0	0		
...	...			...					
255	FF				r	0	0		

Table 19 Upper Page 00 Description 212-255

Upper Page 03 Description

'r' stands for Read Only Register and 'r/w' stands for Read/Writeable Register.

Module and Channel Threshold

Byte	Bit	Name	r/w	Description
128	All	Temp High Alarm MSB	r	Temperature High Alarm Threshold
129	All	Temp High Alarm LSB	r	
130	All	Temp Low Alarm MSB	r	Temperature Low Alarm Threshold
131	All	Temp Low Alarm LSB	r	
132	All	Temp High Warning MSB	r	Temperature High Warning Threshold
133	All	Temp High Warning LSB	r	
134	All	Temp Low Warning MSB	r	Temperature Low Warning Threshold
135	All	Temp Low Warning LSB	r	
136-143	All	Reserved	r	
144	All	Vcc High Alarm MSB	r	Vcc High Alarm Threshold
145	All	Vcc High Alarm LSB	r	
146	All	Vcc Low Alarm MSB	r	Vcc Low Alarm Threshold
147	All	Vcc Low Alarm LSB	r	
148	All	Vcc High Warning MSB	r	Vcc High Warning Threshold
149	All	Vcc High Warning LSB	r	
150	All	Vcc Low Warning MSB	r	Vcc Low Warning Threshold
151	All	Vcc Low Warning LSB	r	
152-225	All	Reserved	r	

Table 20 Upper Page 03 Module and Channel Threshold

Vendor Specific and Optional Channel Control

Byte	Bit	Name	r/w	Description
226-235	All	Vendor Specific/Reserved	r/w	
236	7-4	RX1 Output Preemphasis	r/w	‘00h' = no Preemphasis '01h' = low Preemphasis '02h' = mid Preemphasis '03h' = high Preemphasis
	3-0	RX2 Output Preemphasis	r/w	
237	7-4	RX3 Output Preemphasis	r/w	
	3-0	RX4 Output Preemphasis	r/w	
238	7-4	RX1 Output Amplitude	r/w	‘00h','01h' = low level '02h' = mid level '03h' = high level
	3-0	RX2Output Amplitude	r/w	
239	7-4	RX3 Output Amplitude	r/w	
	3-0	RX4 Output Amplitude	r/w	
240	All	Reserved	r/w	
241	7	Rx4 Output Disable	r/w	Rx Output Disable channel 4 [1)]
	6	Rx3 Output Disable	r/w	Rx Output Disable channel 3 [1)]
	5	Rx2 Output Disable	r/w	Rx Output Disable channel 2 [1)]
	4	Rx1 Output Disable	r/w	Rx Output Disable channel 1 [1)]
	3-0	Reserved	r/w	

Table 21 Upper Page 03 Vendor Specific and Optional Channel Control

Note:

1) Rx(X) Output Disable turns off data channel and disables Channel RxLOS detection

Register 242 to 255 are reserved.

Dimensions

Refer to SFF-8436 specification drawing for the related dimensional, material, plating, and marking information.

Housing Drawings

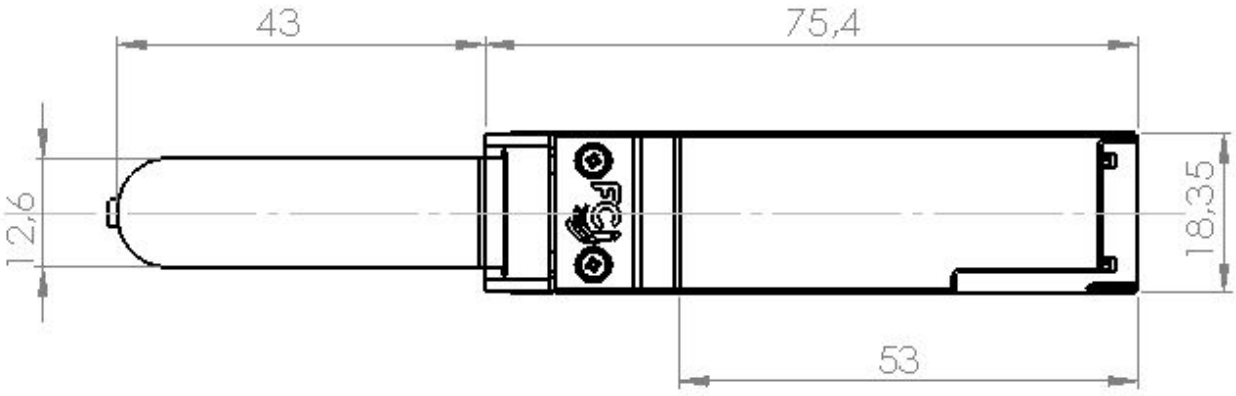


Figure 8 Housing Top View

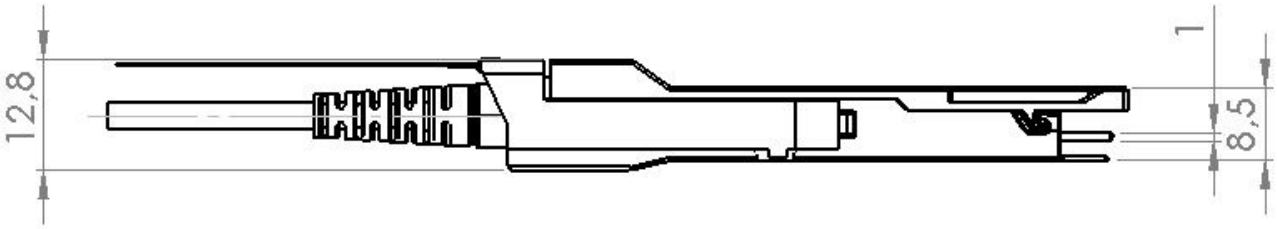


Figure 9 Housing Side View

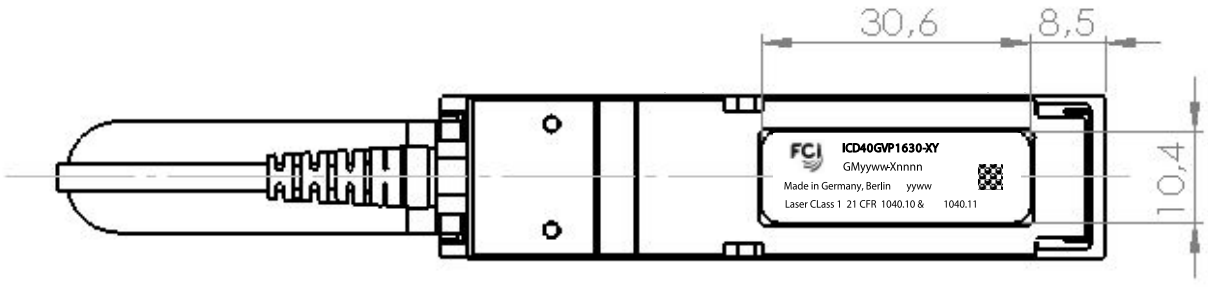


Figure 10 Housing Bottom View

Housing Features

The QSFP module has the following features:

- EMI shielded cage/module
- Intuitive "pull to release mechanism"
- Zinc die-cast housing
- Plating nickel over copper

Label Definition

Label Material

PET adhesive film, 50µ thickness, single sheet, permanent adhesive

Label Color

Silver satin-finished

Font, Print

Franklin Gothic Book, single colored black

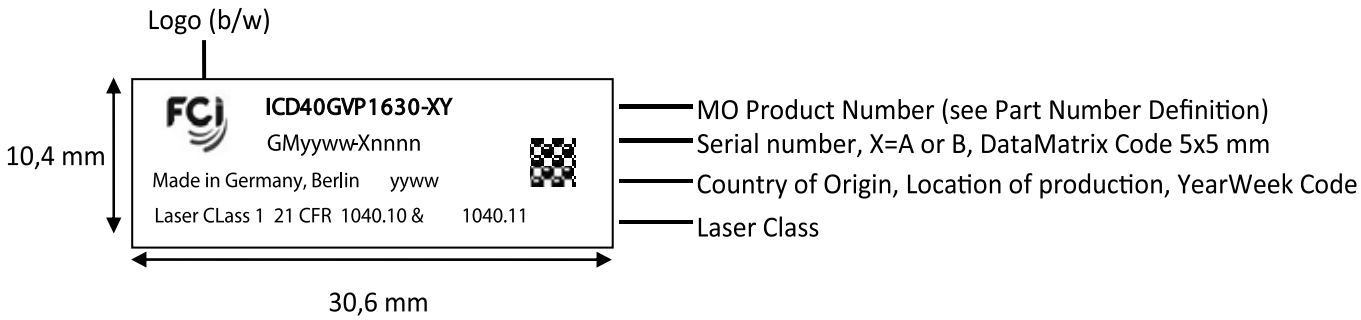


Figure 11 Label Position on Bottom Side of Housing

Warnings

Attention: Observe precautions for handling of electrostatic sensitive devices.

- For removal of the connector from its host, do not pull on the cable itself. Only use the pull strap for this purpose.
- Do not open the housing of the connectors and do not cut into the cable.
- Take assemblies with mechanically damaged jacket out of service.
- Take assemblies with mechanically damaged connector housings out of service.

Note : Since under normal conditions the laser power is not accessible for customers, the AOC is provided without an automatic laser shut down mechanism. In case of a damaged cable, the active optical cable has to be powered off immediately. Note that for damaged cables the laser class is changed to 3R (EN 60825-1).

Eye Safety

This laser based AOC is a CLASS 1 LASER PRODUCT, classified acc. IEC 60825-1:2007. The unit complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to laser notice no. 50, dated June 24, 2007

Caution: use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation. To meet laser safety requirements the transceiver shall be operated within the Absolute Maximum Ratings

Note: All adjustments have been made at the factory prior to shipment of the devices. No maintenance, service, or alteration of the product is required. Tampering with of modifying the performance of the device will result in voided product warranty.

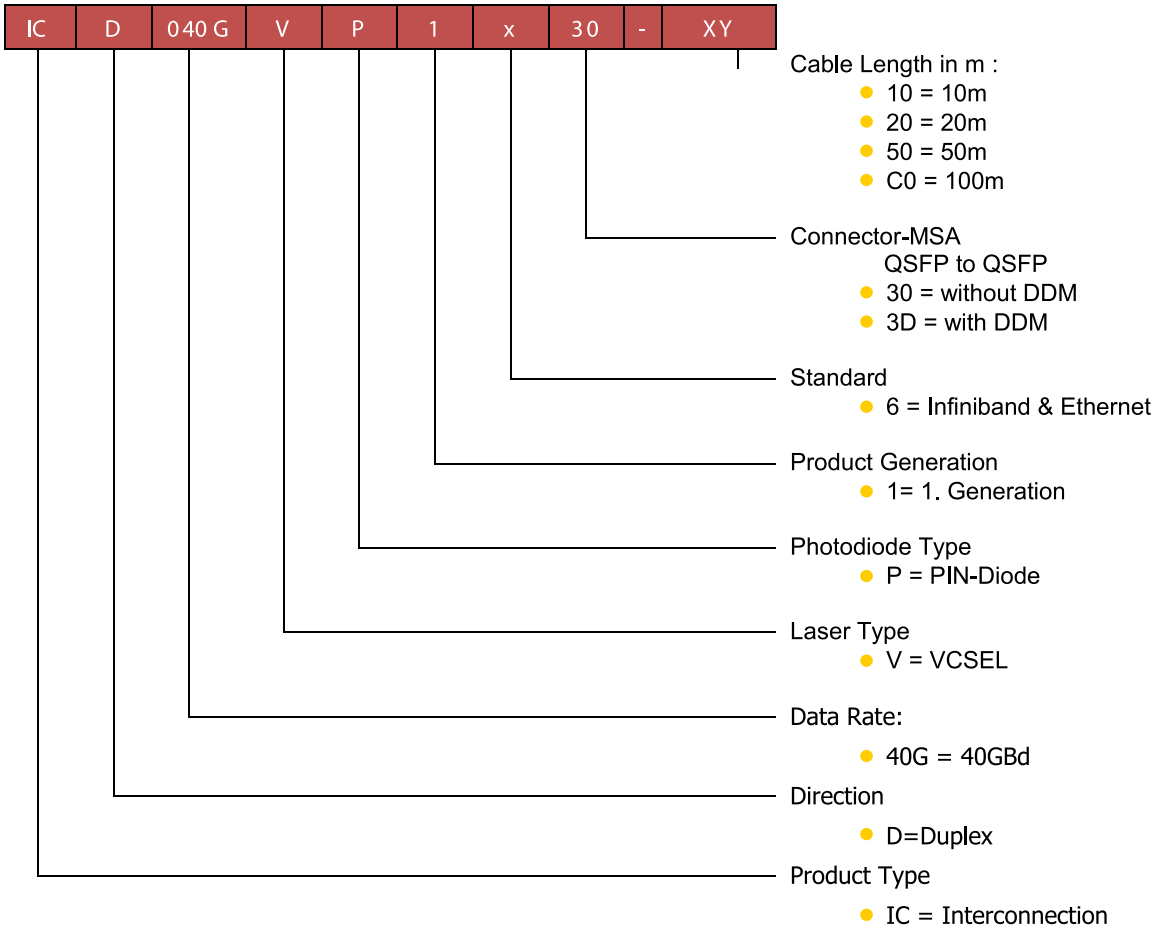
Failure to adhere to the above restrictions could result in a modification that is considered an act of "manufacturing", and will require, under law, recertification of the modified product with the U.S. Food and Drug Administration (ref. 21 CFR 1040.10).

Laser Emission Data

Wavelength	850 nm
Accessible Emission Limit (as defined by IEC: 7 mm aperture at 70 mm distance)	0
Beam divergence (full angle)	n. a.

Part Number Definition

Part Number Coding Scheme



Contact info

EUROPE

FCI Deutschland GmbH
Wernerwerkdamm 16
13629 Berlin, Germany
Ph: +49 30 750 795 00
Fax: +49 30 386 37 54

AMERICAS

MergeOptics
1551 McCarthy Blvd, Suite 116
Milpitas, CA 95035 USA
Phone: 408-493-9970

More information about FCI's complete range of High Speed Input/Output products can be found on www.fciconnect.com/hsio

For more information about e-catalog or FCI sales offices, headquarters, agents and local distributors, visit www.fciconnect.com

ELX.....EA4