QLX4600-S30

Quad Lane Extender

FN6979
Rev 2.00
June 23, 2016

The QLX4600-S30 is a settable quad receive-side equalizer with extended functionality for advanced protocols operating with line rates up to 6.25Gb/s such as DisplayPort v1.2 (HBR1/2), InfiniBand (SDR and DDR), PCI Express and 10GBase-CX4. The QLX4600-S30 compensates for the frequency dependent attenuation of copper twin-axial cables, extending the signal reach up to 30m on a 24AWG cable.

The small form factor, highly-integrated quad design is ideal for high-density data transmission applications including active copper cable assemblies. The four equalizing filters within the QLX4600-S30 can each be set to one of 32 compensation levels, providing optimal signal fidelity for a given media and length. The compensation level for each filter can be set by either (a) three external control pins or (b) a serial bus interface. When the external control pins are used, 18 of the 32 boost levels are available for each channel. If the serial bus is used, all 32 compensation levels are available.

Operating on a single 1.2V power supply, the QLX4600-S30 enables per channel throughputs of up to 6.25Gb/s while supporting lower data rates including 5, 4.25, 3.125 and 2.5Gb/s. The QLX4600-S30 uses Current Mode Logic (CML) inputs/outputs and is packaged in a 4mmx7mm 46 Ld TQFN. Individual channel power-down support is included for PCI Express applications.

Features

- Supports data rates up to 6.25Gb/s
- Low power (78mW per channel)
- Low latency (<500ps)
- Four equalizers in a 4mmx7mm TQFN package for straight route-through architecture and simplified routing
- Each equalizer boost is independently pin selectable and programmable
- Beacon signal support and line silence preservation
- Channel power-down for each equalizer
- 1.2V supply voltage

Applications

- DisplayPort v1.2 active copper cable modules
- InfiniBand (SDR and DDR)
- 10GBase-CX4
- PCI Express Gen 1 and 2
- XAUI and RXAUI, SAS (1.0 and 2.0)
- High-speed active cable assemblies
- High-speed Printed Circuit Board (PCB) traces

Benefits

- Thinner gauge cable
- Extends cable reach greater than 3x
- Improved BER

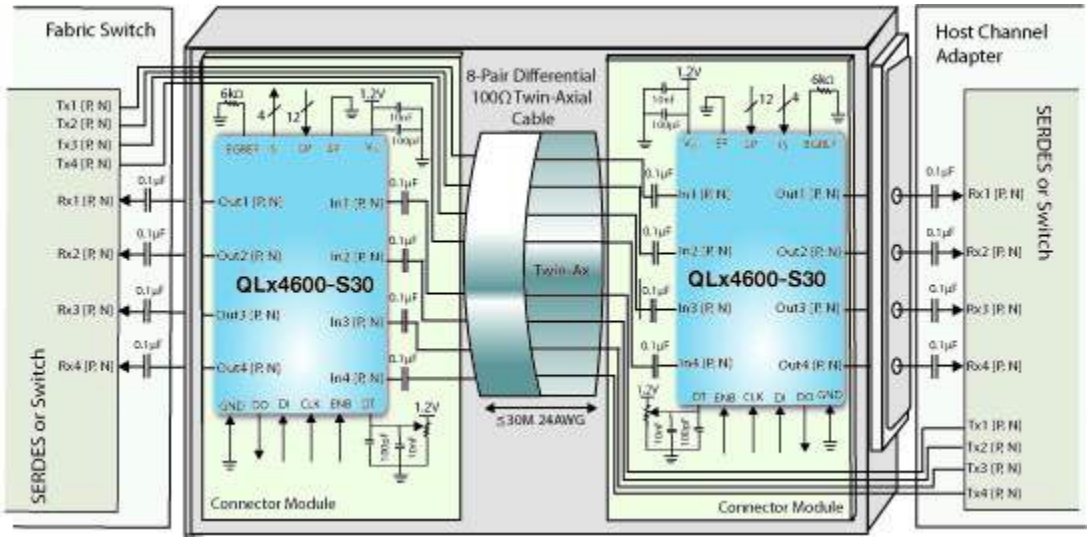


FIGURE 1. TYPICAL APPLICATION CIRCUIT

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
QLX4600SIQT7	QLX4600SIQ	0 to +70	1k	46 Ld TQFN	L46.4x7
QLX4600SIQSR	QLX4600SIQ	0 to +70	100	46 Ld TQFN	L46.4x7

NOTES:

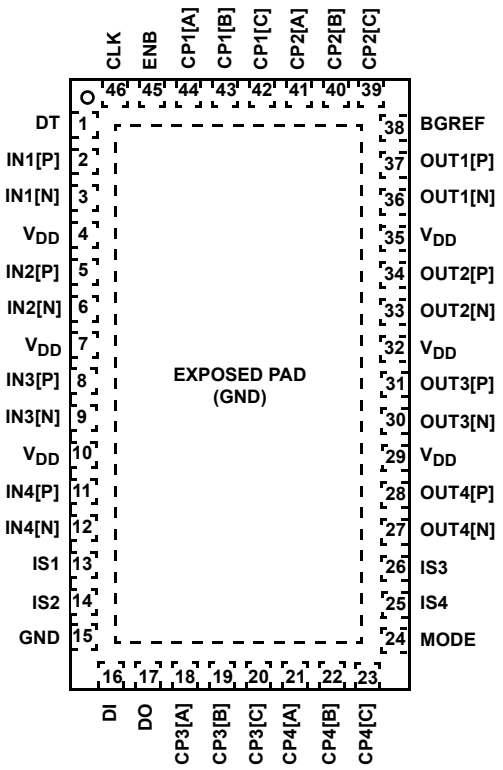
1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for QLX4600-S30. For more information on MSL, please see tech brief TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	DATA RATE (Gb/s)	NUMBER OF Tx OR Rx	POWER CONSUMPTION (mW)	MAXIMUM CABLE LENGTH (24AWG) (m)	DIFFERENTIAL O/P SWING (mV_{P-P})	DE-EMPHASIS (dB)	EQUALIZATION (dB)	DIFFERENCES BETWEEN QLX PARTS	TARGET MARKET
ISL36411	11	4x Rx	440	20	650	N/A	30	N/A	DP1.3, 40GbE, QSFP+
ISL35411	11	4x Tx	340	20	600	4	N/A	N/A	DP1.3, 40GbE, QSFP+
QLX4600-SL30	6.25	4x Rx	312	30	600	N/A	30	4 pins for Loss of Signal (LOS)	DP1.2, SAS-6Gb, PCIe 2.0
QLX4600-S30	6.25	4x Rx	312	30	600	N/A	30	4 pins for Impedance Selection (= Power Down)	DP1.2, SAS-6Gb, PCIe 2.0

Pin Configuration

QLX4600-S30
(46 LD 4x7 TQFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
DT	1	Detection Threshold. Reference DC CURRENT threshold for input signal power detection. Data output OUT[k] is muted when the power of the equalized version of IN[k] falls below the threshold. Tie to ground to disable electrical idle preservation and always enable the limiting amplifier.
IN1[P,N]	2, 3	Equalizer 1 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
V_{DD}	4, 7, 10, 29, 32, 35	Power supply. 1.2V supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for each of these pins for broad high-frequency noise suppression.
IN2[P,N]	5, 6	Equalizer 2 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
IN3[P,N]	8, 9	Equalizer 3 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
IN4[P,N]	11, 12	Equalizer 4 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
IS1	13	Impedance Select 1. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of IN1[P] and IN1[N] each go above 200kΩ and powers down the channel. This pin should be connected to the Fundamental Reset signal in PCI Express™. Otherwise, connect to V_{DD} to hold the input impedance at 50Ω.
IS2	14	Impedance Select 2. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of IN2[P] and IN2[N] each go above 200kΩ and powers down the channel. This pin should be connected to the Fundamental Reset signal in PCI Express™. Otherwise, connect to V_{DD} to hold the input impedance at 50Ω.
GND	15	Ground

Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	DESCRIPTION
DI	16	Serial data input, CMOS logic. Input for serial data stream to program internal registers controlling the boost for all four equalizers. Synchronized with clock (CLK) on pin 46. Overrides the boost setting established on CP control pins. Internally pulled down.
DO	17	Serial data output, CMOS logic. Output of the internal registers controlling the boost for all four equalizers. Synchronized with clock on pin 46. Equivalent to serial data input on DI but delayed by 21 clock cycles.
CP3[A,B,C]	18, 19, 20	Control pins for setting equalizer 3. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP4[A,B,C]	21, 22, 23	Control pins for setting equalizer 4. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
MODE	24	Boost-level control mode input, CMOS logic. Allows serial programming of internal registers through pins DI, ENB, and CLK when set HIGH. Resets all internal registers to zero and uses boost levels set by CP pins when set LOW. If serial programming is not used, this pin should be grounded.
IS4	25	Impedance Select 4. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of IN4[P] and IN4[N] each go above 200kΩ and powers down the channel. This pin should be connected to the Fundamental Reset signal in PCI Express™. Otherwise, connect to V_{DD} to hold the input impedance at 50Ω.
IS3	26	Impedance Select 3. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of IN3[P] and IN3[N] each go above 200kΩ and powers down the channel. This pin should be connected to the Fundamental Reset signal in PCI Express™. Otherwise, connect to V_{DD} to hold the input impedance at 50Ω.
OUT4[N,P]	27, 28	Equalizer 4 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
OUT3[N,P]	30, 31	Equalizer 3 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
OUT2[N,P]	33, 34	Equalizer 2 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
OUT1[N,P]	36, 37	Equalizer 1 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
BGREF	38	External bandgap reference resistor. Recommended value of 6.04kΩ ±1%.
CP2[C,B,A]	39, 40, 41	Control pins for setting equalizer 2. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP1[C,B,A]	42, 43, 44	Control pins for setting equalizer 1. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
ENB	45	Serial data enable (active low), CMOS logic. Internal registers can be programmed with DI and CLK pins only when the ENB pin is 'LOW'. Internally pulled down.
CLK	46	Serial data clock, CMOS logic. Synchronous clock for serial data on DI and DO pins. Data on DI is latched on the rising clock edge. Clock speed is recommended to be between 10MHz and 20MHz. Internally pulled down.
EXPOSED PAD	-	Exposed ground pad. For proper electrical and thermal performance, this pad should be connected to the PCB ground plane.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND). . . . . -0.3V to 1.3V
Voltage at All Input Pins. . . . . -0.3V to V_{DD} + 0.3V
ESD Rating at All Pins . . . . . 2kV (HBM)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
46 Ld TQFN Package (Note 4)	32	2.3

Operating Ambient Temperature Range. . . . . 0°C to +70°C
Storage Ambient Temperature Range. . . . . -55°C to +150°C
Maximum Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Supply Voltage	V_{DD}		1.1	1.2	1.3	V
Operating Ambient Temperature	T_A		0	25	70	°C
Bit Rate		NRZ data applied to any channel	1.5		6.25	Gb/s

Control Pin Characteristics

Typical values are at V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 800mV_{P-P}, unless otherwise noted. V_{DD} = 1.1V to 1.3V, T_A = 0°C to +70°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT	NOTES
Input 'LOW' Logic Level	V_{IL}	DI, CLK, ENB	0	0	350	mV	
Input 'HIGH' Logic Level	V_{IH}	DI, CLK, ENB	750		V_{DD}	mV	
Output 'LOW' Logic Level	V_{OL}	IS[k], DO, MODE	0	0	250	mV	
Output 'HIGH' Logic Level	V_{OH}	IS[k], DO, MODE	1000		V_{DD}	mV	
'LOW' Resistance State		CP[k][A,B,C]	0		1	kΩ	6
'MID' Resistance State		CP[k][B,C]	22.5	25	27.5	kΩ	6
'HIGH' Resistance State		CP[k][A,B,C]	500			kΩ	6
Input Current		Current draw on digital pin, i.e., CP[k][A,B,C], DI, CLK, ENB or MODE		30	100	µA	

NOTE:

6. If four CP pins are tied together, the resistance values in this table should be divided by four.

Electrical Specifications

Typical values are at V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 800mV$_{P-P}$, unless otherwise noted. V_{DD} = 1.1V to 1.3V, T_A = 0°C to +70°C.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT	NOTES
Supply Current	I_{DD}			260		mA	
Cable Input Amplitude Range	V_{IN}	Measured differentially at data source before encountering channel loss	800	1200	1600	mV$_{P-P}$	8
DC Differential Input Resistance		Measured on input channel IN[k]	80	100	120	Ω	
DC Single-Ended Input Resistance		Measured on input channel IN[k]P or IN[k]N	40	50	60	Ω	
Input Return Loss (Differential)	$S_{DD}11$	50MHz to 3.75GHz	10			dB	9
Input Return Loss (Common-Mode)	$S_{CC}11$	50MHz to 3.75GHz	6			dB	9
Input Return Loss (Common-Mode to Differential Conversion)	$S_{DC}11$	50MHz to 3.75GHz	20			dB	9
Output Amplitude Range	V_{OUT}	Active data transmission mode; Measured differentially at OUT[k]P and OUT[k]N with 50Ω load on both output pins	450	550	650	mV$_{P-P}$	
		Line Silence mode; Measured differentially at OUT[k]P and OUT[k]N with 50Ω load on both output pins		10	20	mV$_{P-P}$	
Differential Output Impedance		Measured on OUT[k]	80	105	120	Ω	
Output Return Loss (Differential)	$S_{DD}22$	50MHz to 3.75GHz	10			dB	9
Output Return Loss (Common-Mode)	$S_{CC}22$	50MHz to 3.75GHz	5			dB	9
Output Return Loss (Common-Mode to Differential Conversion)	$S_{DC}22$	50MHz to 3.75GHz	20			dB	9
Output Residual Jitter		2.5Gb/s, 3.125Gb/s, 4.25Gb/s, 5Gb/s; Up to 20m 24AWG standard twin-axial cable (approximately -25dB at 2.5GHz); 800mV$_{P-P}$ ≤ V_{IN} ≤ 1600mV$_{P-P}$		0.15	0.25	UI	8, 10, 11
		2.5Gb/s, 3.125Gb/s, 4.25Gb/s, 5Gb/s; 12m 30AWG standard twin-axial cable (approximately -30dB at 2.5GHz); 800mV$_{P-P}$ ≤ V_{IN} ≤ 1600mV$_{P-P}$		0.20	0.30	UI	8, 10, 11
		2.5Gb/s, 3.125Gb/s, 4.25Gb/s, 5Gb/s; 20m 28AWG standard twin-axial cable (approximately -35dB at 2.5GHz); 1200mV$_{P-P}$ ≤ V_{IN} ≤ 1600mV$_{P-P}$		0.25	0.35	UI	8, 10, 11
		6.25Gb/s, Up to 15m 28AWG standard twin-axial cable (approximately -30dB at 3.2GHz); 1200mV$_{P-P}$ ≤ V_{IN} ≤ 1600mV$_{P-P}$		0.25	0.35	UI	8, 10, 11
Output Transition Time	t_r, t_f	20% to 80%	30	60	80	ps	12
Lane-to-Lane Skew					50	ps	
Propagation Delay		From IN[k] to OUT[k]			500	ps	
LOS Assert Time		Time to assert Loss-of-Signal (LOS) indicator when transitioning from active data mode to line silence mode			100	µs	13

Electrical Specifications

Typical values are at V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 800mV_{P-P}, unless otherwise noted. V_{DD} = 1.1V to 1.3V, T_A = 0°C to +70°C. **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT	NOTES
LOS Deassert Time		Time to assert Loss-of-Signal (LOS) indicator when transitioning from line silence mode to active data mode			100	µs	13
Data-to-Line Silence Response Time	t_{DS}	Time to transition from active data to line silence (muted output) on 20m 24AWG standard twin-axial cable at 5Gb/s			15	ns	13, 16
		Time from last bit of ALIGN(0) for SAS OOB signaling to line silence (<20mV_{P-P} output); Meritec 24AWG 20m; 3Gb/s			14	ns	17
Line Silence-to-Data Response Time	t_{SD}	Time to transition from line silence mode (muted output) to active data on 20m 24AWG standard twin-axial cable at 5Gb/s			20	ns	13, 16
		Time from first bit of ALIGN(0) for SAS OOB signaling to 450mV_{P-P} output; Meritec 24AWG 20m; 3Gb/s			19	ns	17
Timing Difference (SAS)	$\lvert t_{DS} - t_{SD} \rvert$	For SAS OOB signaling support; Meritec 24AWG 20m			5	ns	17

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. After channel loss, differential amplitudes at QLX4600-S30 inputs must meet the input voltage range specified in "Absolute Maximum Ratings" on page 5.
9. Temperature = +25°C, V_{DD} = 1.2V.
10. Output residual jitter is the difference between the total jitter at the lane extender output and the total jitter of the transmitted signal (as measured at the input to the channel). Total jitter (T_J) is DJ_{P-P} + 14.1 x RJ_{RMS}.
11. Measured using a PRBS (2^7-1) pattern. Deterministic jitter at the input to the lane extender is due to frequency-dependent, media-induced loss only.
12. Rise and fall times measured using a 1GHz clock with a 20ps edge rate.
13. For active data mode, cable input amplitude is 400mV_{P-P} (differential) or greater. For line silence mode, cable input amplitude is 20mV_{P-P} (differential) or less.
14. Measured differentially across the data source.
15. During line silence, transmitter noise in excess of this voltage range may result in differential output amplitudes from the QLX4600 that are greater than 20mV_{P-P}.
16. The data pattern preceding line silence mode is comprised of the PCIe Electrical Idle Ordered Set (EIOS). The data pattern following line silence mode is comprised of the PCIe Electrical Idle Exit Sequence (EIES).
17. The data pattern preceding or following line silence mode is comprised of the SAS-2 ALIGN (0) sequence for OOB signaling at 3Gb/s, and amplitude of 800mV_{P-P}.

Serial Bus Timing Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
CLK Set-Up Time	t_{SCK}	From the falling edge of ENB	10			ns
DI Set-Up Time	t_{SDI}	Prior to the rising edge of CLK	10			ns
DI Hold Time	t_{HDI}	From the rising edge of CLK	6			ns
ENB 'HIGH'	t_{HEN}	From the falling edge of the last data bit's CLK	10			ns
Boost Setting Operational	t_D	From ENB 'HIGH'			10	ns
DO Hold Time	t_{CQ}	From the rising edge of CLK to DO transition	12			ns
Clock Rate	f_{CLK}	Reference clock for serial bus EQ programming			20	MHz

Typical Performance Characteristics

V_{DD} = 1.2V, T_A = +25°C, unless otherwise noted. Performance was characterized using the system testbed shown in Figure 2. Unless otherwise noted, the transmitter generated a Non-Return-to-Zero (NRZ) PRBS-7 sequence at 800mV_{P-P} (differential) with 10ps of peak-to-peak deterministic jitter. This transmit signal was launched into twin-axial cable test channels of varying gauges and lengths. The loss characteristics of these test channels are plotted as a function of frequency in Figure 3. The received signal at the output of these test channels was then processed by the QLX4600-S30 before being passed to a receiver. Eye diagram measurements were made with 4000 waveform acquisitions and include random jitter.

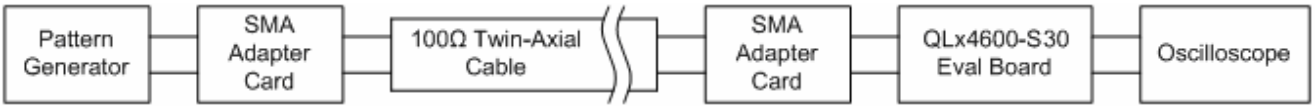


FIGURE 2. DEVICE CHARACTERIZATION TEST SETUP

TEST CHANNEL LOSS CHARACTERISTICS

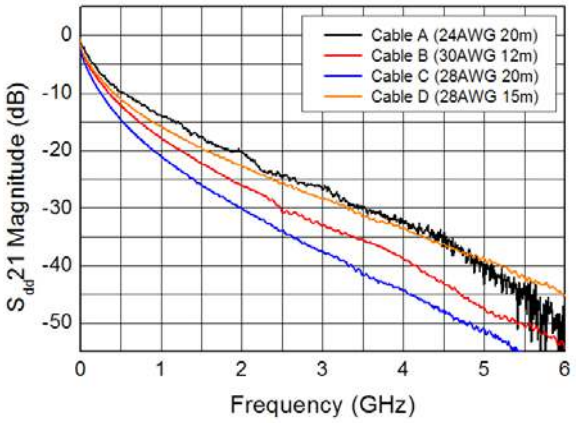


FIGURE 3. TWIN-AXIAL CABLE LOSS AS A FUNCTION OF FREQUENCY FOR VARIOUS TEST CHANNELS

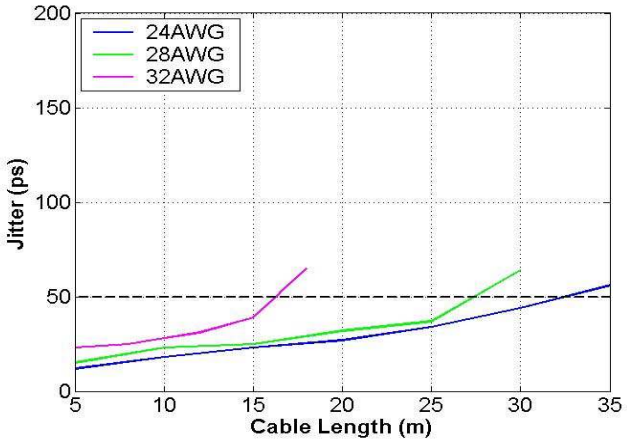


FIGURE 4A. JITTER vs CABLE LENGTH, 5Gb/s

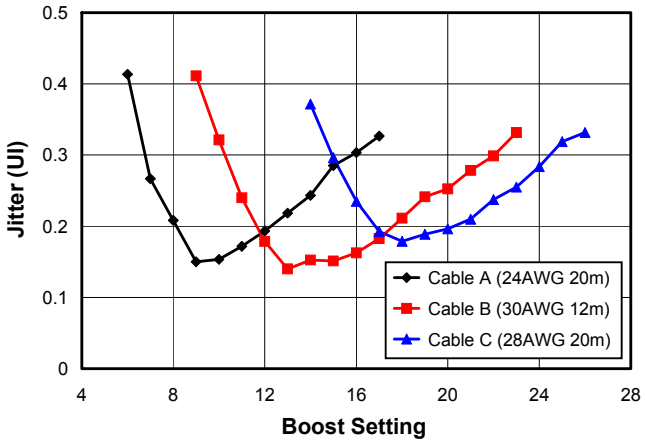


FIGURE 4B. JITTER vs BOOST SETTING, 5Gb/s

FIGURE 4. JITTER VS CABLE LENGTH AND JITTER VS BOOST SETTING AT 5Gb/s

Typical Performance Characteristics (Continued)

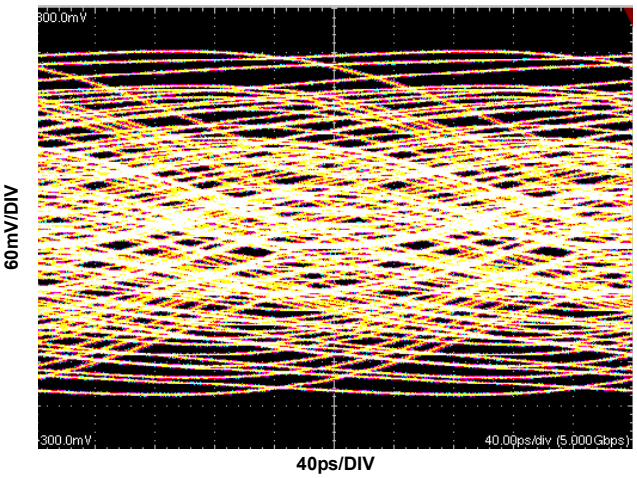


FIGURE 5. RECEIVED SIGNAL AFTER 20m OF 24AWG TWIN-AXIAL CABLE (CABLE A), 5Gb/s

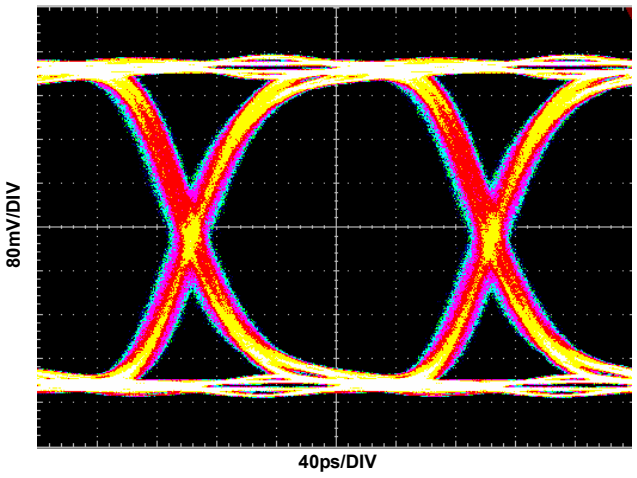


FIGURE 6. QLX4600-S30 OUTPUT AFTER 20m OF 24AWG TWIN-AXIAL CABLE (CABLE A), 5Gb/s

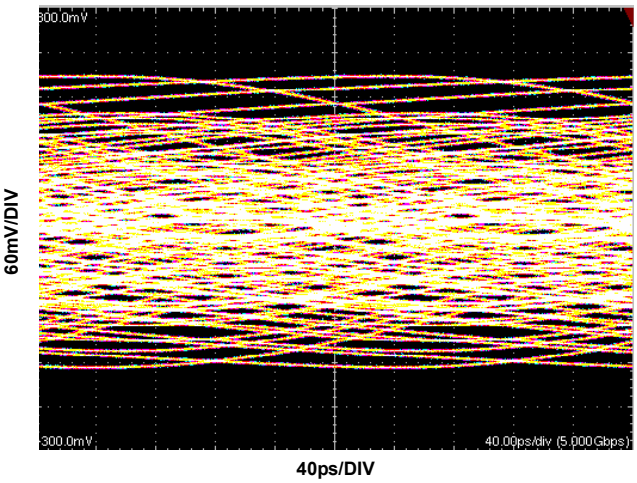


FIGURE 7. RECEIVED SIGNAL AFTER 12m OF 30AWG TWIN-AXIAL CABLE (CABLE B), 5Gb/s

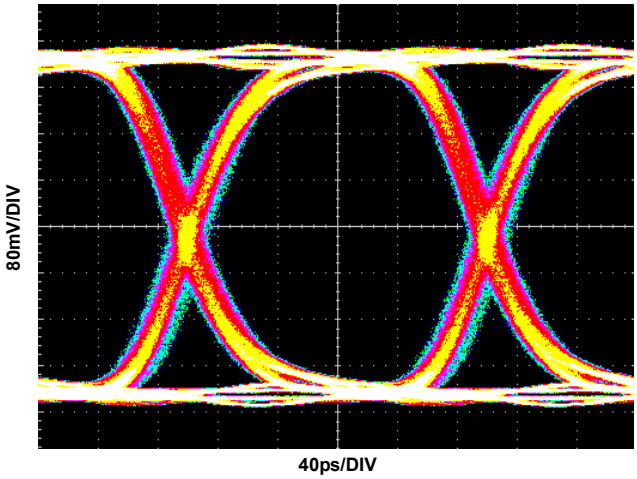


FIGURE 8. QLX4600-S30 OUTPUT AFTER 12m OF 30AWG TWIN-AXIAL CABLE (CABLE B), 5Gb/s

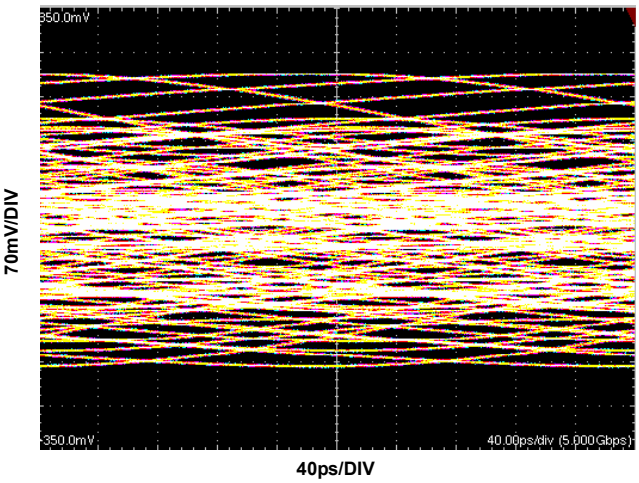


FIGURE 9. RECEIVED SIGNAL AFTER 20m OF 28AWG TWIN-AXIAL CABLE (CABLE C) (Note 18), 5Gb/s

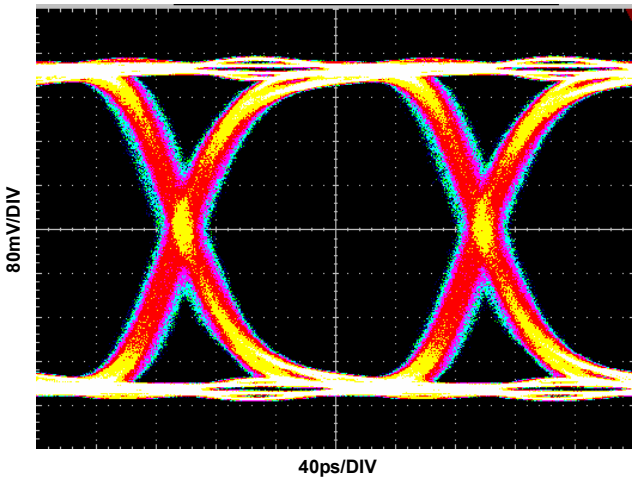


FIGURE 10. QLX4600-S30 OUTPUT AFTER 20m OF 28AWG TWIN-AXIAL CABLE (CABLE C) (Note 18), 5Gb/s

Typical Performance Characteristics (Continued)

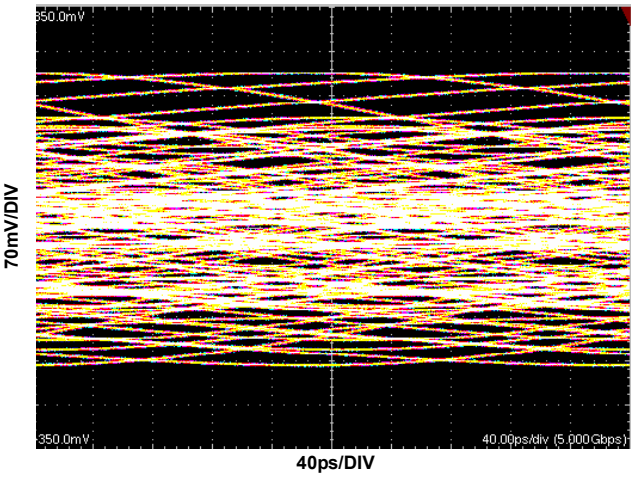


FIGURE 11. RECEIVED SIGNAL AFTER 30m OF 24AWG TWIN-AXIAL CABLE (Note 18), 5Gb/s

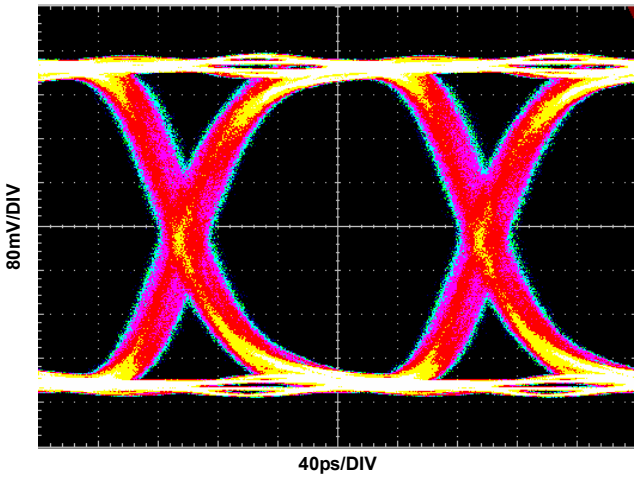


FIGURE 12. QLX4600-S30 OUTPUT AFTER 30m OF 24AWG TWIN-AXIAL CABLE (Note 18), 5Gb/s

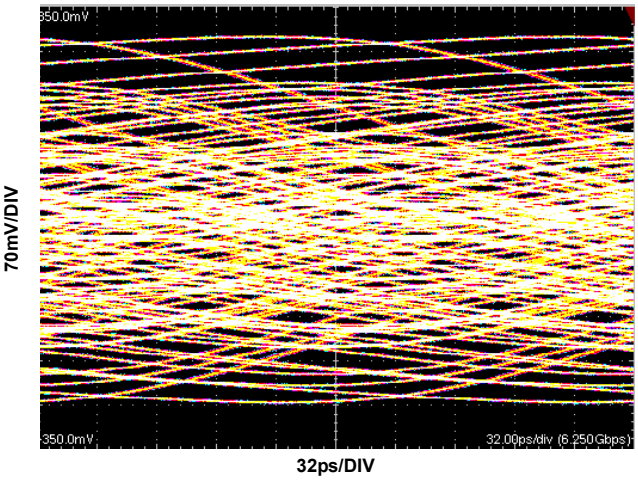


FIGURE 13. RECEIVED SIGNAL AFTER 15m OF 28AWG TWIN-AXIAL CABLE (CABLE D) (Note 18), 6.25Gb/s

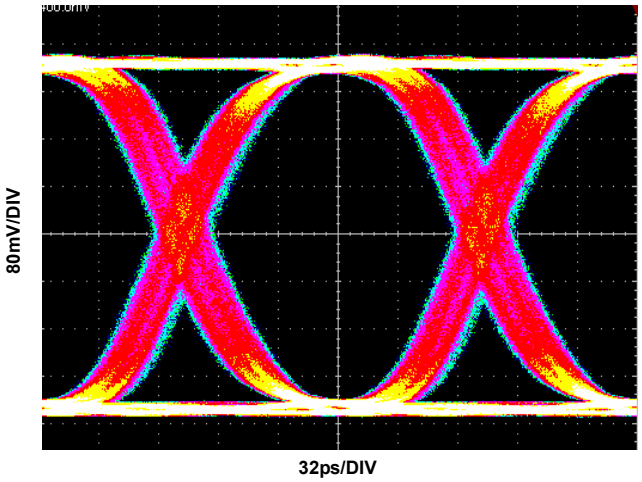


FIGURE 14. QLX4600-S30 OUTPUT AFTER 15m OF 28AWG TWIN-AXIAL CABLE (CABLE D) (Note 18), 6.25Gb/s

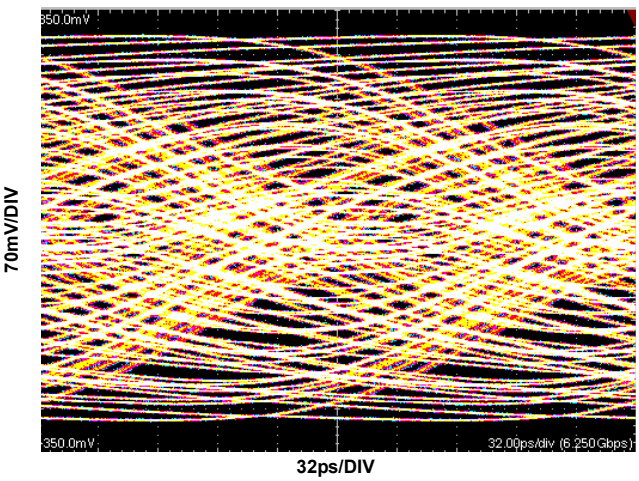


FIGURE 15. RECEIVED SIGNAL AFTER 40" FR4, 6.25Gb/s

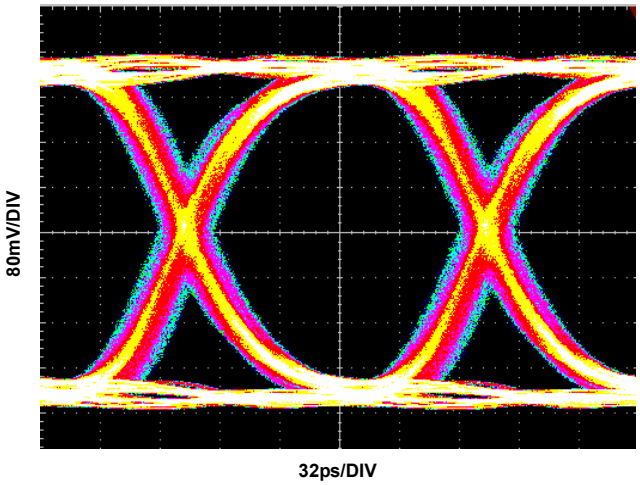


FIGURE 16. QLX4600-S30 OUTPUT AFTER 40" FR4, 6.25Gb/s

Typical Performance Characteristics (Continued)

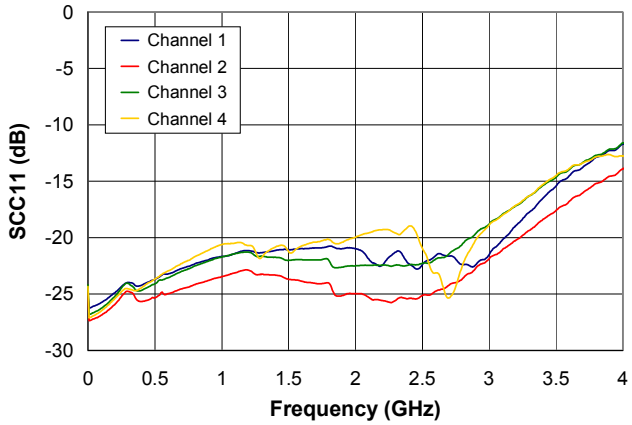


FIGURE 17. INPUT COMMON-MODE RETURN LOSS

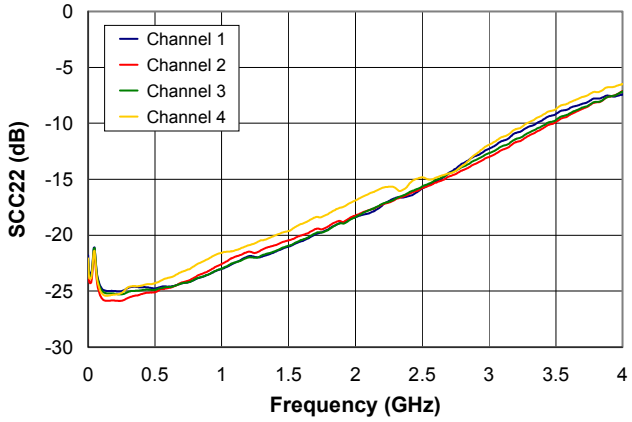


FIGURE 18. OUTPUT COMMON-MODE RETURN LOSS

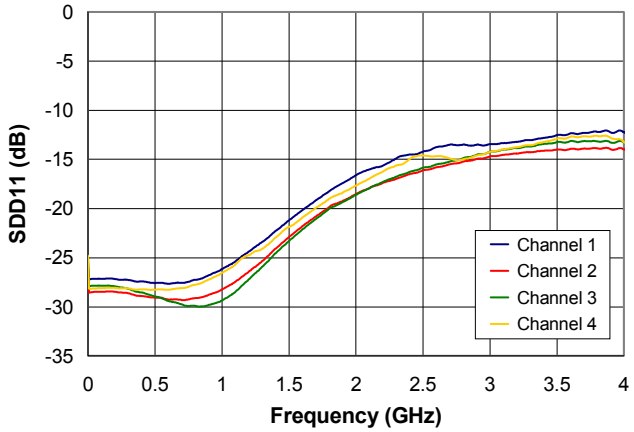


FIGURE 19. INPUT DIFFERENTIAL RETURN LOSS

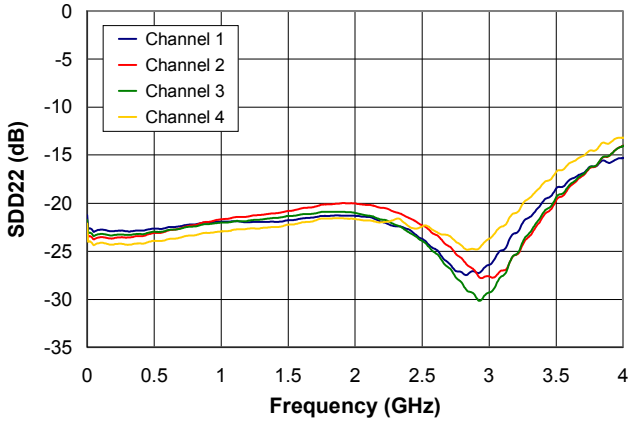


FIGURE 20. OUTPUT DIFFERENTIAL RETURN LOSS

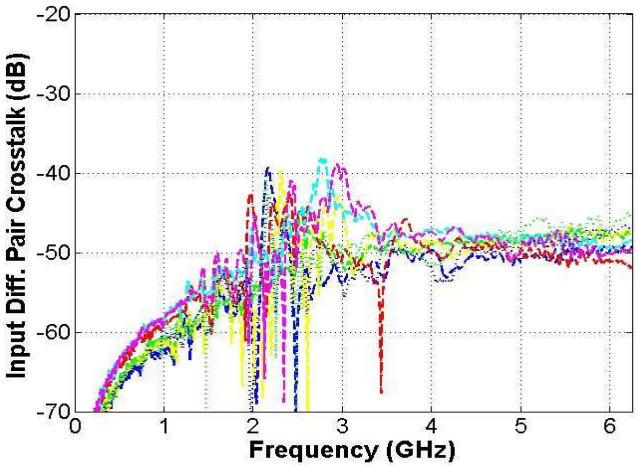


FIGURE 21. DIFFERENTIAL CROSSTALK BETWEEN ADJACENT INPUT CHANNEL

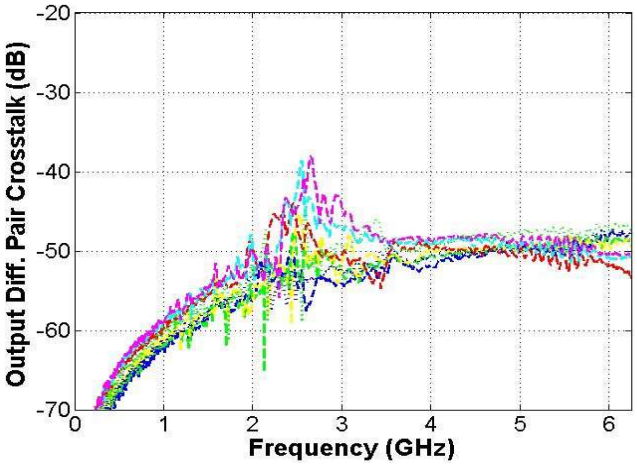


FIGURE 22. DIFFERENTIAL CROSSTALK BETWEEN ADJACENT INPUT CHANNELS

NOTE:

18. Differential transmit amplitude = 1200mV$_{P-P}$.

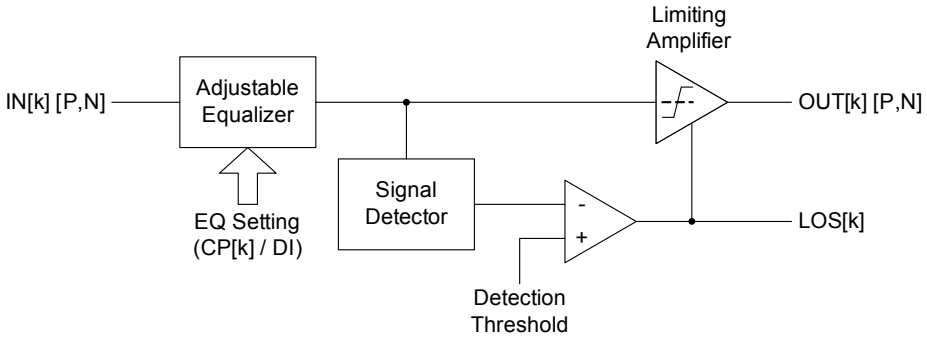


FIGURE 23. FUNCTIONAL DIAGRAM OF A SINGLE CHANNEL WITHIN THE QLX4600-S30

Operation

The QLX4600-S30 is an advanced quad lane-extender for high-speed interconnects. A functional diagram of one of the four channels in the QLX4600-S30 is shown in Figure 23. In addition to a robust equalization filter to compensate for channel loss and restore signal fidelity, the QLX4600-S30 contains unique integrated features to preserve special signaling protocols typically broken by other equalizers. The signal detect function is used to mute the channel output when the equalized signal falls below the level determined by the Detection Threshold (DT) pin voltage. This function is intended to preserve periods of line silence (“quiescent state” in InfiniBand contexts).

As illustrated in Figure 23, the core of each high-speed signal path in the QLX4600-S30 is a sophisticated equalizer followed by a limiting amplifier. The equalizer compensates for skin loss, dielectric loss, and impedance discontinuities in the transmission channel. Each equalizer is followed by a limiting amplification stage that provides a clean output signal with full amplitude swing and fast rise-fall times for reliable signal decoding in a subsequent receiver.

Individually Adjustable Equalization Boost

Each channel in the QLX4600-S30 features an independently settable equalizer for custom signal restoration. Each equalizer can be set to one of 32 levels of compensation when the serial bus is used to program the boost level and one of 18 compensation levels when the CP[k] pins are used to set the level. The equalizer transfer functions for a subset of these compensation levels are plotted in Figure 24. The flexibility of this adjustable compensation architecture enables signal fidelity to be optimized on a channel-by-channel basis, providing support for a wide variety of channel characteristics and data rates ranging from 2.5 to 6.25 Gb/s. Because the boost level is externally set rather than internally adapted, the QLX4600-S30 provides reliable communication from the very first bit transmitted. There is no time needed for adaptation and control loop convergence. Furthermore, there are no pathological data patterns that will cause the QLX4600-S30 to move to an incorrect boost level.

“Applications Information” on page 13 details how to set the boost level by both the CP-pin voltage approach and the serial programming approach.

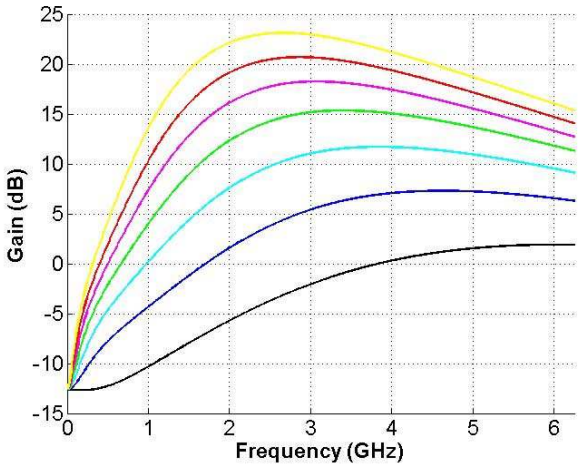


FIGURE 24. EQUALIZER TRANSFER FUNCTIONS FOR SETTINGS 0, 5, 10, 15, 20, 25, AND 31 IN THE QLX4600-S30

CML Input and Output Buffers

The input and output buffers for the high-speed data channels in the QLX4600-S30 are implemented using CML. Equivalent input and output circuits are shown in Figures 25 and 26, respectively.

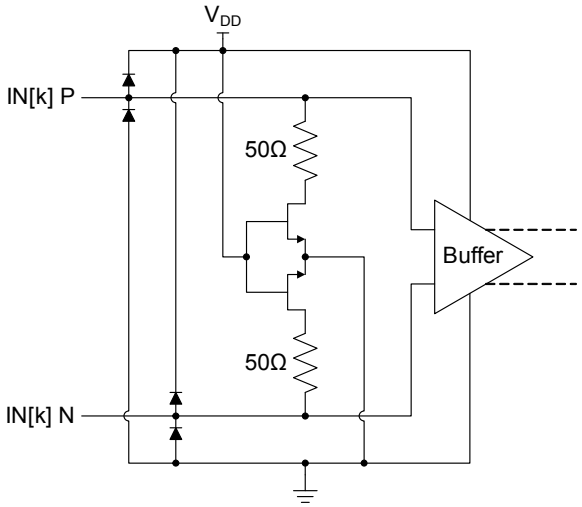


FIGURE 25. CML INPUT EQUIVALENT CIRCUIT FOR THE QLX4600-S30

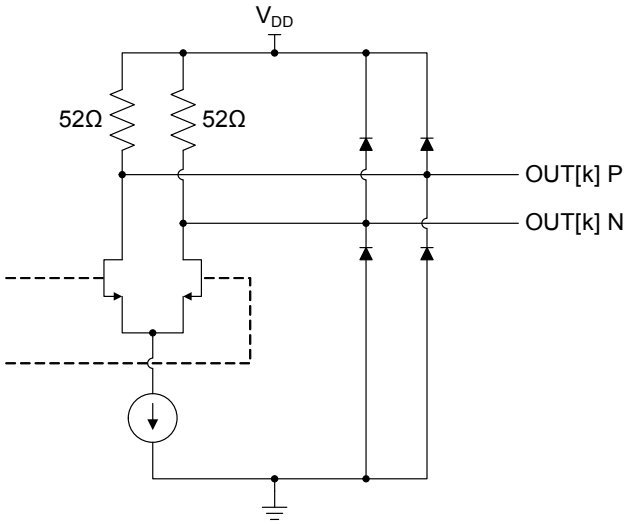


FIGURE 26. CML OUTPUT EQUIVALENT CIRCUIT FOR THE QLX4600-S30

NOTE: The load value of 52Ω is used to internally match $S_{DD}22$ for a characteristic impedance of 50Ω.

Line Silence/Electrical Idle/Quiescent Mode

Line silence is commonly broken by the limiting amplification in other equalizers. This disruption can be detrimental in many systems that rely on line silence as part of the protocol. The QLX4600-S30 contains special lane management capabilities to detect and preserve periods of line silence while still providing the fidelity-enhancing benefits of limiting amplification during active data transmission. Line silence is detected by measuring the amplitude of the equalized signal and comparing that to a threshold set by the current at the DT pin. When the amplitude falls below the threshold, the output driver stages are muted and held at their nominal common-mode voltage.

NOTE: The output common-mode voltage remains constant during both active data transmission and output muting modes.

Input Impedance Select

The input impedance of a channel on the QLX4600-S30 is set high (>200k) when powered down or when the IS[k] pin is pulled low. This provides compatibility with the Fundamental Reset signal and receiver detection/link initialization in the PCI Express protocol.

Channel Power-Down

In addition to controlling the input impedance, the IS[k] pin powers down the equalizer channel when pulled low. This feature allows a system controller individually to power down unused channels and to minimize power consumption. Example: the signal to power down a channel could come from an Intelligent Platform Management controller in ATCA applications for E-Keying. The current draw for a channel is reduced from 50mA to 3.8mA when powered down.

Applications Information

Several aspects of the QLX4600-S30 are capable of being dynamically managed by a system controller to provide maximum flexibility and optimum performance. These functions are controlled by interfacing to the highlighted pins in Figure 27. The specific procedures for controlling these aspects of the QLX4600-S30 are the focus of this section.

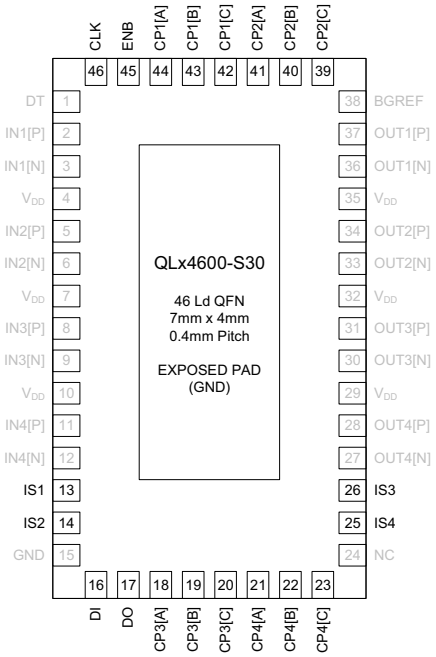


FIGURE 27. PIN DIAGRAM HIGHLIGHTING PINS USED FOR DYNAMIC CONTROL OF THE QLX4600-S30

Equalization Boost Level

Channel equalization for the QLX4600-S30 can be individually set to either (a) one of 18 levels through the DC voltages on external control pins or (b) one of 32 levels via a set of registers programmed by a low speed serial bus. The pins used to control the boost level are highlighted in Figure 27. Descriptions of these pins are listed in Table 2 on page 14. Please refer to "Pin Descriptions" on page 3 for descriptions of all other pins on the QLX4600-S30.

TABLE 2. DESCRIPTIONS OF PINS THAT CAN BE USED TO SET EQUALIZATION BOOST LEVEL

PIN NAME	PIN NUMBER	DESCRIPTION
DI	16	Serial data input, CMOS logic. Input for serial data stream to program internal registers controlling the boost for all four equalizers. Synchronized with clock (CLK) on pin 46. Overrides the boost setting established on CP control pins. Internally pulled down.
DO	17	Serial data output, CMOS logic. Output of the internal registers controlling the boost for all four equalizers. Synchronized with clock on pin 46. Equivalent to serial data input on DI but delayed by 21 clock cycles.
CP3[A,B,C]	18, 19, 20	Control pins for setting equalizer 3. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP4[A,B,C]	21, 22, 23	Control pins for setting equalizer 4. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
MODE	24	Boost-level control mode input, CMOS logic. Allows serial programming of internal registers through pins DI, ENB and CLK when set HIGH. Resets all internal registers to zero and uses boost levels set by CP pins when set LOW. If serial programming is not used, this pin should be grounded.
CP2[C,B,A]	39, 40, 41	Control pins for setting equalizer 2. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP1[C,B,A]	42, 43, 44	Control pins for setting equalizer 1. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
ENB	45	Serial data enable (active low), CMOS logic. Internal registers can be programmed with DI and CLK pins only when the ENB pin is 'LOW'. Internally pulled down.
CLK	46	Serial data clock, CMOS logic. Synchronous clock for serial data on DI and DO pins. Data on DI is latched on the rising clock edge. Clock speed is recommended to be between 10MHz and 20MHz. Internally pulled down.

The boost setting for equalizer Channel k can be read as a three digit ternary number across CP[k][A,B,C]. The ternary value is established by the value of the resistor between V_{DD} and the CP[k][A,B,C] pin.

As a second option, the equalizer boost setting can be taken from a set of registers programmed through a serial bus interface (pins 16, 17, 45, and 46). Using this interface, a set of registers is programmed to store the boost level. A total of 21 registers are used. Registers 2 through 21 are parsed into four 5-bit words. Each 5-bit word determines which of 32 boost levels to use for the corresponding equalizer. Register 1 instructs the QLX4600-S30 to use registers 2 through 21 to set the boost level rather than the control pins CP[k][A,B,C].

Both options have their relative advantages. The control pin option minimizes the need for external controllers as the boost level can be set in the board design resulting in a compact layout. The register option is more flexible for cases in which the optimum boost level will not be known and can be changed by a host bus adapter with a small number of pins. It is noted that the serial bus interface can also be daisy-chained among multiple QLX4600-S30 devices to afford a compact programmable solution even when a large number of data lines need to be equalized.

Upon power-up, the default value of all the registers (and register 1 in particular) is zero, and thus, the CP pins are used to set the boost level. This permits an alternate interpretation on setting the boost level. Specifically, the CP pins define the default boost level until the registers are (if ever) programmed via the serial bus.

TABLE 3. MAPPING BETWEEN CP-SETTING RESISTOR AND PROGRAMMED BOOST LEVELS

RESISTANCE BETWEEN CP PIN AND V_{DD}			SERIAL BOOST LEVEL
CP[A]	CP[B]	CP[C]	
Open	Open	Open	0
Open	Open	25kΩ	2
Open	Open	0Ω	4
Open	25kΩ	Open	6
Open	25kΩ	25kΩ	8
Open	25kΩ	0Ω	10
Open	0Ω	Open	12
Open	0Ω	25kΩ	14
Open	0Ω	0Ω	15
0Ω	Open	Open	16
0Ω	Open	25kΩ	17
0Ω	Open	0Ω	19
0Ω	25kΩ	Open	21
0Ω	25kΩ	25kΩ	23
0Ω	25kΩ	0Ω	24
0Ω	0Ω	Open	26
0Ω	0Ω	25kΩ	28
0Ω	0Ω	0Ω	31

Control Pin Boost Setting

When register 1 of the QLX4600-S30 is zero (the default state on power-up), the voltages at the CP pins are used to determine the boost level of each channel. For each of the four channels, k, the [A], [B], and [C] control pins (CP[k]) are associated with a 3-bit non binary word. While [A] can take one of two values, 'LOW' or 'HIGH', [B] and [C] can take one of three different values: 'LOW', 'MIDDLE', or 'HIGH'. This is achieved by changing the value of a resistor connected between the VDD and CP pins, which is internally pulled low with a 25kΩ resistor. Thus, a 'HIGH' state is achieved by using a 0Ω resistor, 'MIDDLE' is achieved with a 25kΩ resistor, and 'LOW' is achieved with an open resistance. Table 3 on page 14 defines the mapping from the 3-bit CP word to the 18 out of 32 possible levels available via the serial interface.

If all four channels are to use the same boost level, then a minimum number of board resistors can be realized by tying together like the CP[k][A,B,C] pins across all channels. For instance, all four CP[k][A] pins can be tied to the same resistor running to VDD. Consequently, only three resistors are needed to control the boost of all four channels. If the CP Pins are tied together and the 25kΩ is used, the value changes to a 6.25kΩ resistor because the 25kΩ is divided by 4.

Optimal Cable Boost Settings

The settable equalizing filter within the QLX4600 enables the device to optimally compensate for frequency-dependent attenuation across a wide variety of channels, data rates and encoding schemes. For the reference channels plotted in Figure 3, Table 4 shows the optimal boost setting when transmitting a PRBS-7 signal. The optimal boost setting is defined as the equalizing filter setting that minimizes the output residual jitter of the QLX4600. The settings in Table 4 represent the optimal settings for the QLX4600C across an ambient temperature range of 0°C to +70°C. The optimal setting at room temperature (+20°C to +40°C) is generally one to two settings lower than the values listed in Table 5 on page 16.

TABLE 4. OPTIMAL CABLE BOOST SETTINGS

CABLE	APPROX. LOSS AT 2.5GHz (dB)	QLX4600-S30 BOOST
Cable A	22	10
Cable B	27	14
Cable C	35	19

NOTE: Optimal boost settings should be determined on an application-by-application basis to account for variations in channel type, loss characteristics and encoding schemes. The settings in Table 4 are presented as guidelines to be used as a starting point for application-specific optimization.

Register Description

The QLX4600-S30's internal registers are listed in Table 5. Register 1 determines whether the CP pins or register values 2 through 21 are used to set the boost level. When this register is set, the QLX4600-S30 uses registers 2-6, 7-11, 12-16, and 17-21 to set the boost level of equalizers 1, 2, 3, and 4. When register 1 is not set, the CP pins are used to determine the boost level for each equalizer channel. The use of five registers for each equalizer channel allows all 32 boost levels as candidate boost levels.

TABLE 5. DESCRIPTION OF INTERNAL SERIAL REGISTERS

REGISTER	EQUALIZER CHANNEL	DESCRIPTION
1	1-4	CP control override – Use registers 2 through 21 (rather than CP pins) to establish the boost levels when this bit is set.
2	1	Equalizer setting Bit 0 (LSB).
3		Equalizer setting Bit 1.
4		Equalizer setting Bit 2.
5		Equalizer setting Bit 3.
6		Equalizer setting Bit 4 (MSB).
7	2	Equalizer setting Bit 0 (LSB).
8		Equalizer setting Bit 1.
9		Equalizer setting Bit 2.
10		Equalizer setting Bit 3.
11		Equalizer setting Bit 4 (MSB).
12	3	Equalizer setting Bit 0 (LSB).
13		Equalizer setting Bit 1.
14		Equalizer setting Bit 2.
15		Equalizer setting Bit 3.
16		Equalizer setting Bit 4 (MSB).
17	4	Equalizer setting Bit 0 (LSB).
18		Equalizer setting Bit 1.
19		Equalizer setting Bit 2.
20		Equalizer setting Bit 3.
21		Equalizer setting Bit 4 (MSB).

Serial Bus Programming

Pins 16 (DI), 45 (ENB), and 46 (CLK) are used to program the registers inside the QLX4600-S30. Figure 28 on page 17 shows an exemplary timing diagram for the signals on these pins. The serial bus can be used to program a single QLX4600-S30 according to the following steps:

1. The ENB pin is pulled ‘LOW’.
   - While this pin is ‘LOW’, the data input on DI are read into registers but not yet latched.
   - A setup time of t_{SCK} is needed between ENB going ‘LOW’ and the first rising clock edge.
2. At least 21 values are read from DI on the rising edge of the CLK signal.
   - If more than 21 values are passed in, then only the last 21 values are kept in a FIFO fashion.
   - The data on DI should start by sending the value destined for register 21 and finish by sending the value destined for register 1.
   - A range of clock frequencies can be used. A typical rate is 10MHz. The clock should not exceed 20MHz.
   - Setup (t_{SDI}) and hold (t_{HDI}) times are needed around the rising clock edge.
3. The ENB pin is pulled ‘HIGH’ and the contents of the registers are latched and take effect.
   - After clocking in the last data bit, an additional t_{HEN} should elapse before pulling the ENB signal ‘HIGH’.
   - After completing these steps, the new values will affect within t_D.

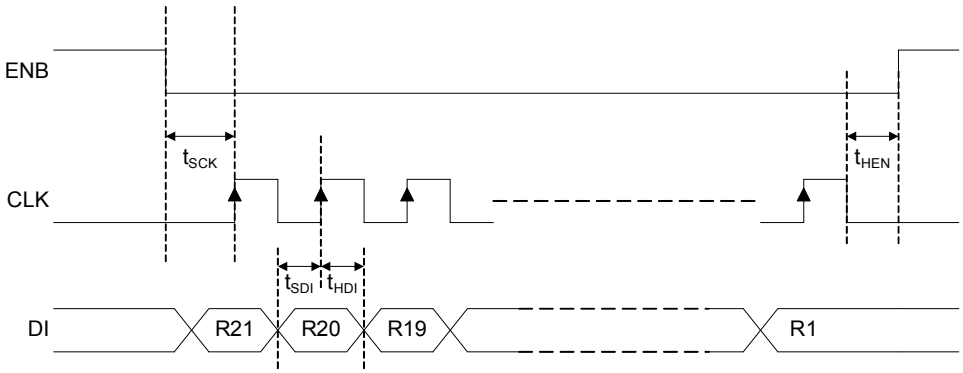


FIGURE 28. TIMING DIAGRAM FOR PROGRAMMING THE INTERNAL REGISTERS OF THE QLX4600-S30

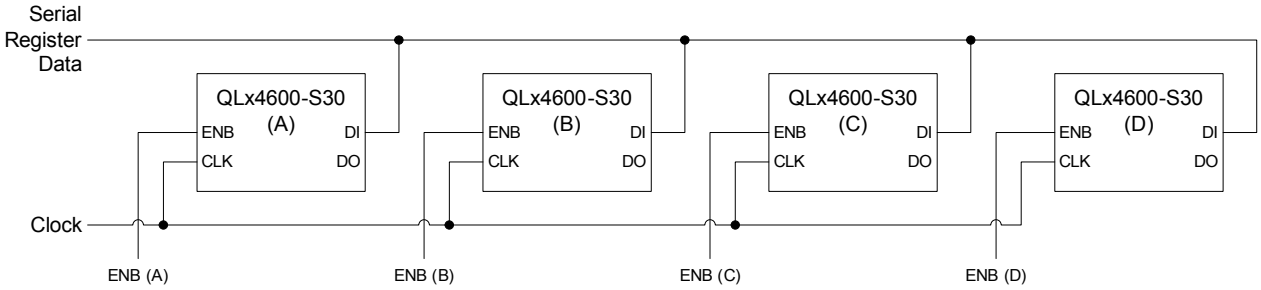


FIGURE 29. SERIAL BUS PROGRAMMING MULTIPLE QLX4600-S30 DEVICES USING SEPARATE ENB SIGNALS

Programming Multiple QLX4600-S30 Devices

The serial bus interface provides a simple means of setting the equalizer boost levels with a minimal amount of board circuitry. Many of the serial interface signals can be shared among the QLX4600-S30 devices on a board and two options are presented in this section. The first uses common clock and serial data signals along with separate ENB signals to select which QLX4600-S30 accepts the programmed changes. The second method uses a common ENB signal as the serial data is carried-over from one QLX4600-S30 to the next.

Separate ENB Signals

Multiple QLX4600-S30 devices can be programmed from a common serial data stream as shown in Figure 29. Here, each QLX4600-S30 is provided its own ENB signal, and only one of these ENB signals is pulled 'LOW', and hence accepting the register data, at a time. In this situation, the programming of each equalizer follows the steps outlined in Figure 30 on page 18.

DI/DO Carryover

The DO pin (pin 17) can be used to daisy-chain the serial bus among multiple QLX4600-S30 chips. The DO pin outputs the overflow data from the DI pin. Specifically, as data is pipelined into a QLX4600-S30, it proceeds according to the following flow. First, a bit goes into shadow register 1. Then, with each clock cycle, it shifts over into subsequent higher numbered registers. After shifting into register 21, it is output on the DO pin on the same clock cycle. Thus, the DO signal is equal to the DI signal, but delayed by 20 clock cycles. The timing diagram for the DO pin is shown in Figure 30 on page 18 where the first 20 bits output from the DO are indefinite and subsequent bits are the data fed into the DI pin. The delay between the rising clock edge and the data transition is t_{CQ}.

A diagram for programming multiple QLX4600-S30s is shown in Figure 31 on page 18. It is noted that the board layout should ensure that the additional clock delay experienced between subsequent QLX4600-S30s should be no more than the minimum value of t_{CQ}, i.e., 12ns.

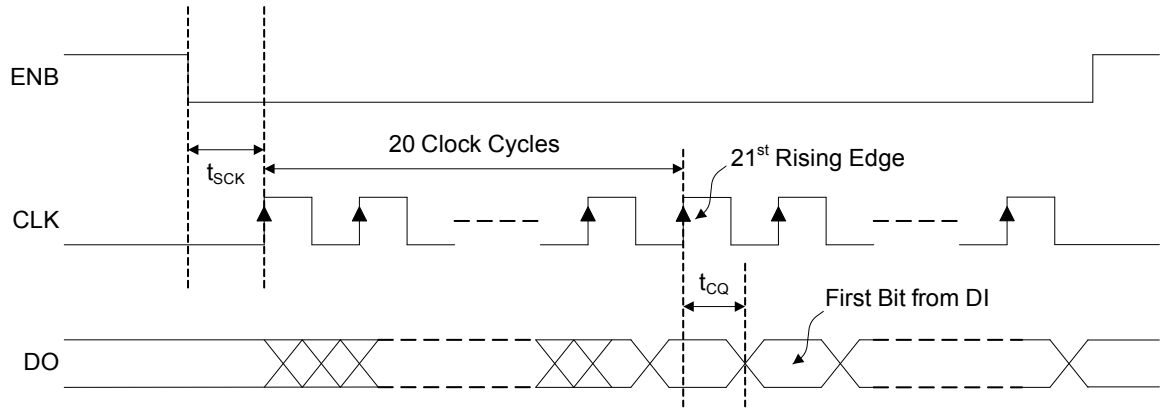


FIGURE 30. TIMING DIAGRAM FOR DI/DO CARRYOVER

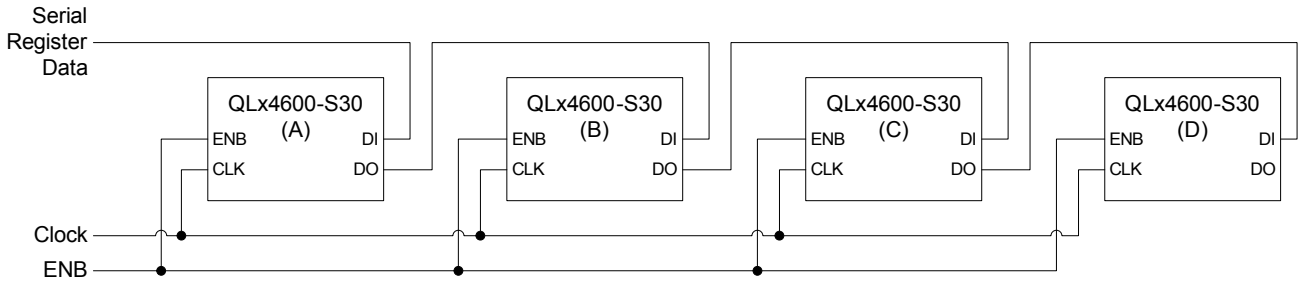


FIGURE 31. SERIAL BUS PROGRAMMING MULTIPLE QLX4600-S30 DEVICES USING DI/DO CARRYOVER

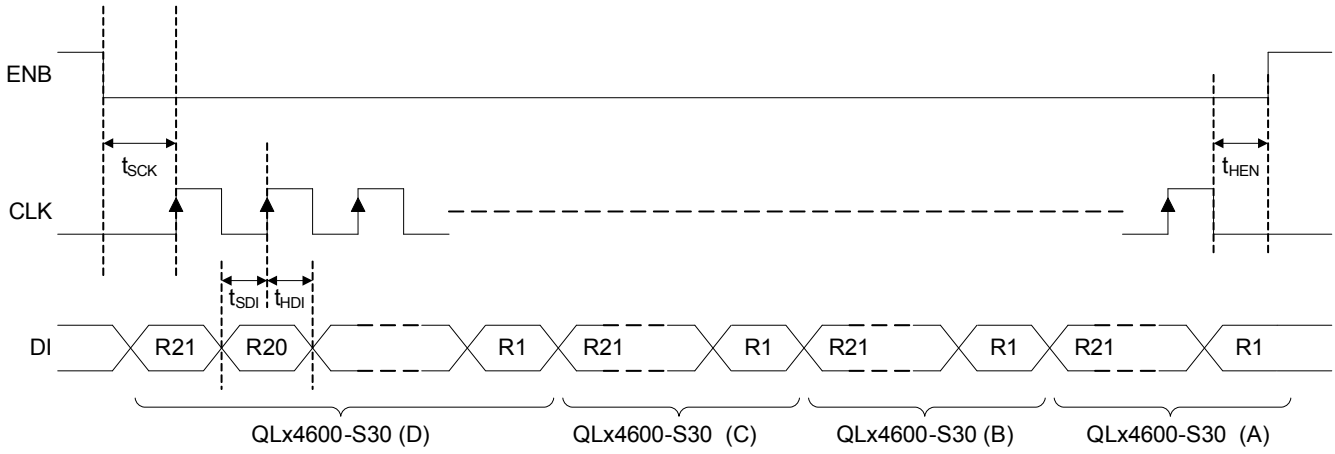


FIGURE 32. TIMING DIAGRAM FOR PROGRAMMING MULTIPLE QLX4600-S30 DEVICES USING DI/DO CARRYOVER

Detection Threshold (DT) Pin Functionality

The QLX4600-S30 is capable of maintaining periods of line silence on any of its four channels by monitoring each channel for Loss Of Signal (LOS) conditions and subsequently muting the outputs of a respective channel when such a condition is detected. A reference current applied to the Detection Threshold (DT) pin is used to set the LOS threshold of the internal signal detection circuitry. Current control on the DT pin is done via one or two external resistors. Nominally, both a pull-up and pull-down resistor are tied to the DT pin (Figure 33A), but if adequate control of the supply voltage is maintained to within ±3% of 1.2V, then a simple pull-down resistor is adequate (as in Figure 33B). Resistors used should be at least 1/16W, with ±1% precision.

The internal bias point of the DT pin, nominally 1.05V, is used in conjunction with the voltage divider (R_1 and R_2) shown in Figure 33A to set the reference current on the DT pin.

Case 1: Channels with less than or equal to 25dB loss at 2.5GHz (1Gb/s to 6Gb/s):

For signals transmitted on channels having less than or equal to 25dB of loss at 2.5GHz, the optimal DT reference current is 0µA. This optimal reference current may be achieved by either leaving the DT pin floating, or tying the DT pin to ground (GND) with a 10MΩ resistor.

Case 2: Channels with greater than 25dB loss at 2.5GHz (1Gb/s to 6Gb/s):

For channels exhibiting more than 25dB of total loss (this includes cable or FR-4 loss) the DT pin should be configured for a reference sink current (coming out of the DT pin) of approximately 2µA. A typical configuration for a 2µA sink current is given in Figure 33C. If the configuration in Figure 33B is utilized, a 525kΩ resistor would be used.

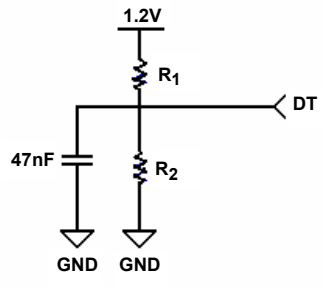


FIGURE 33A.

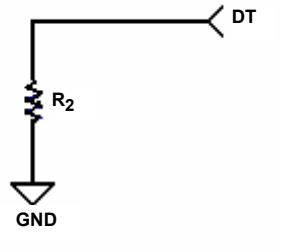


FIGURE 33B.

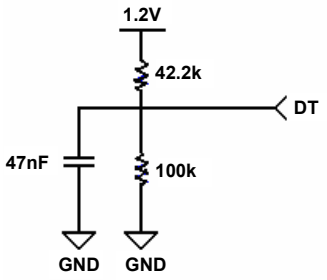


FIGURE 33C.

FIGURE 33.

Typical Application Reference Designs

Figures 34 and 35 show reference design schematics for a QLX4600-S30 evaluation board with an SMA connector interface. Figure 34 shows the schematic for the case when the equalizer boost level is set via the CP pins. Figure 35 shows the schematic for the case when the level is set via the serial bus interface.

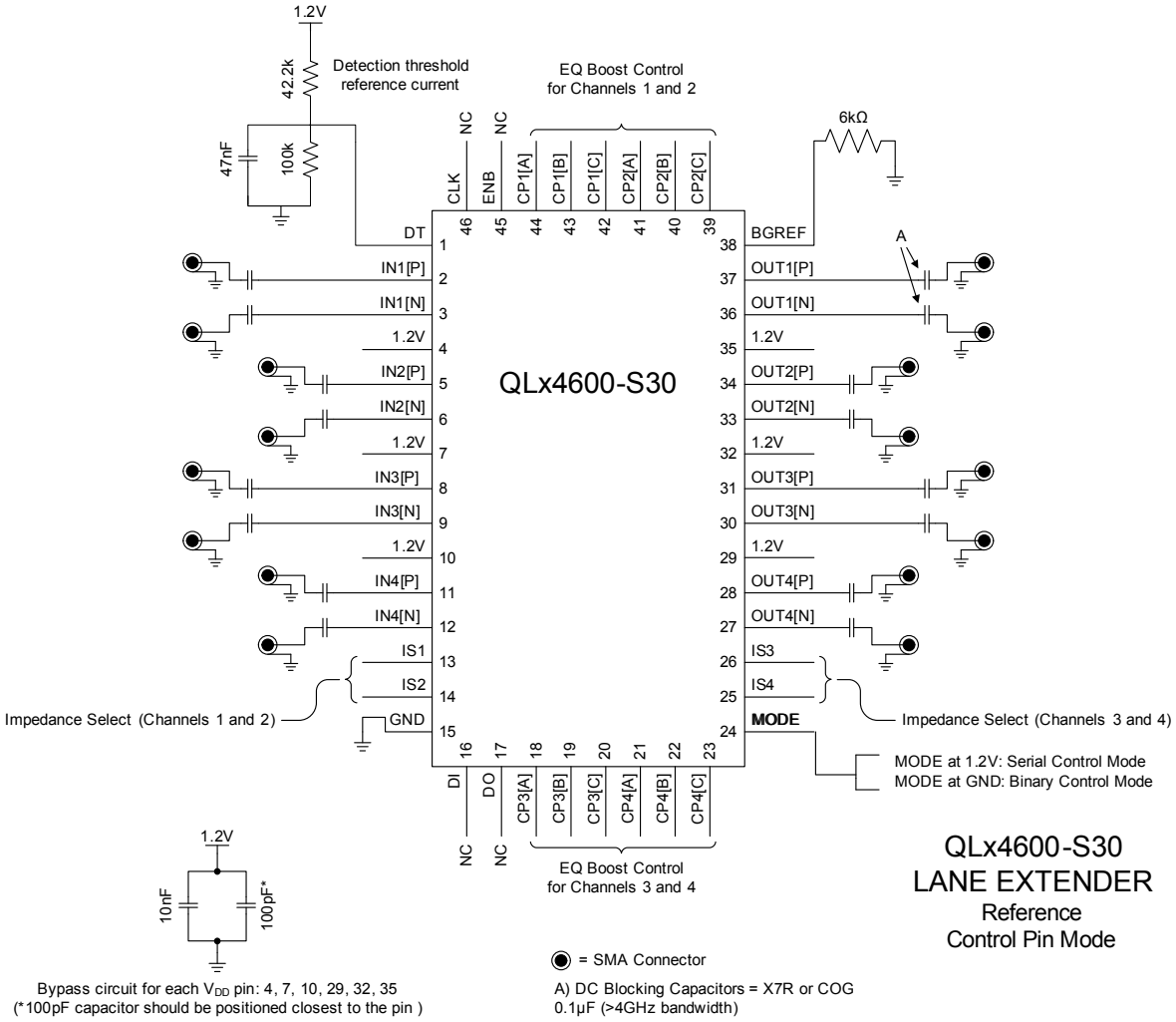


FIGURE 34. APPLICATION CIRCUIT FOR THE QLX4600-S30 EVALUATION BOARD USING THE CONTROL PINS FOR SETTING THE EQUALIZER COMPENSATION LEVEL

Typical Application Reference Designs (Continued)

Figures 34 and 35 show reference design schematics for a QLX4600-S30 evaluation board with an SMA connector interface. Figure 34 shows the schematic for the case when the equalizer boost level is set via the CP pins. Figure 35 shows the schematic for the case when the level is set via the serial bus interface.

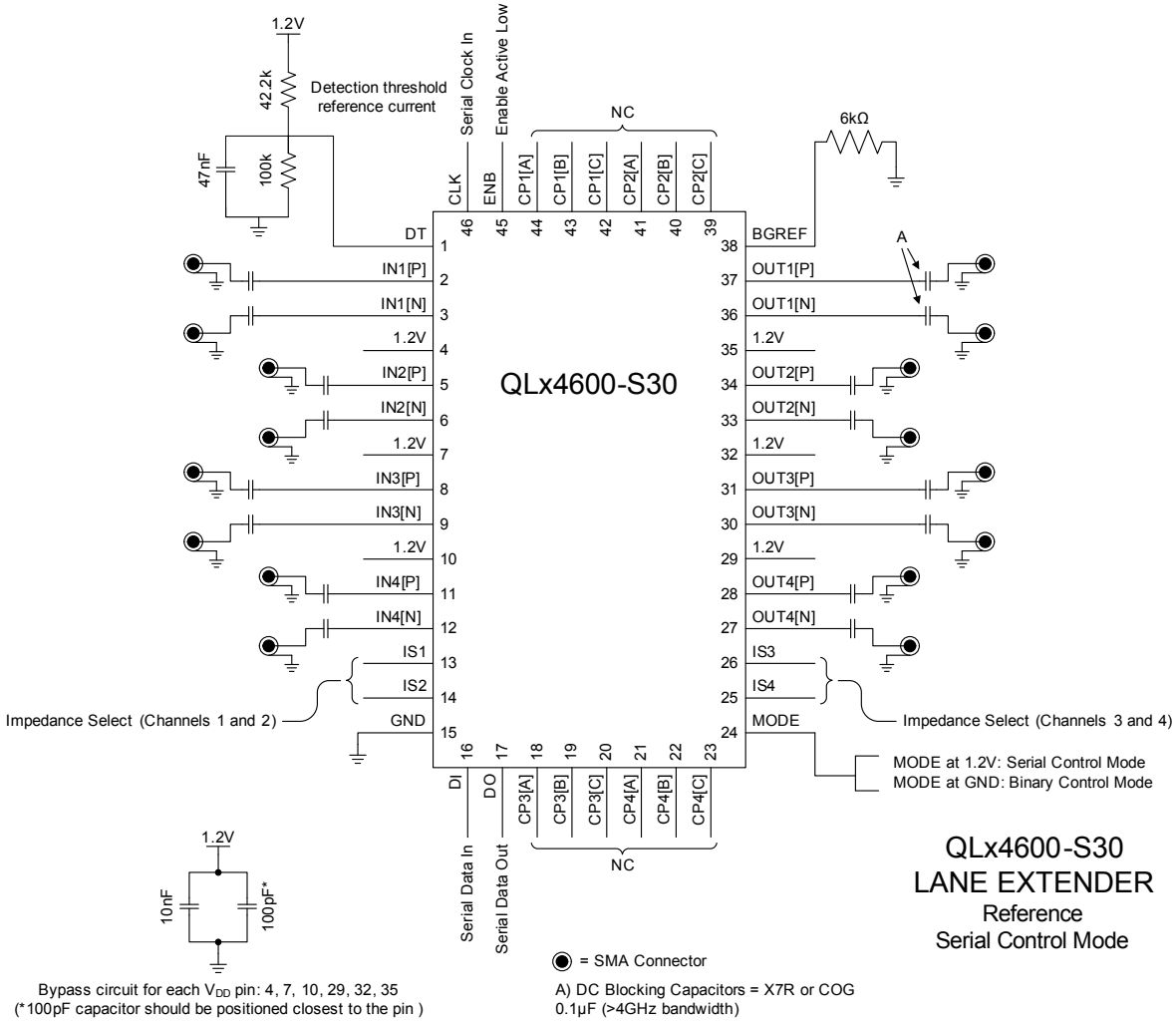


FIGURE 35. APPLICATION CIRCUIT FOR THE QLX4600-S30 EVALUATION BOARD USING THE SERIAL BUS INTERFACE FOR SETTING THE EQUALIZER COMPENSATION LEVEL

About Q:ACTIVE™

Intersil has long realized that to enable the complex server clusters of next generation datacenters, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE™ product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency and cable gauge size as well as increased airflow in tomorrow's datacenters. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding datacenter.

Intersil Lane Extenders allow greater reach over existing cabling, while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow and reduces power consumption.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
June 23, 2016	FN6979.2	Updated entire datasheet applying Intersil's new standards. Updated the first paragraph on page 1 by adding "DisplayPort v1.2 (HBR1/2),". Updated applications bullet replaced QSFP with "DisplayPort v1.2" Combined "XAUI and RXAUI" and "SAS (1.0 and 2.0)" application bullets. Added Notes 1 and 3 to the ordering information table on page 2. Added Note 5 on page 5. Removed ∞ symbol from Maximum specification for "'HIGH' Resistance State" on page 5. Added Note 7 on page 7 and referenced in specification tables. Updated Figure 27 on page 13. Added Revision History and About Intersil sections. Updated POD L46.4x7 to the latest revision changes are as follows: -3/15/13 Side view, changed pkg thickness from 0.70+/-0.05 to 0.75+/-0.05 Detail x, changed from 0.152 REF to 0.203 REF.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

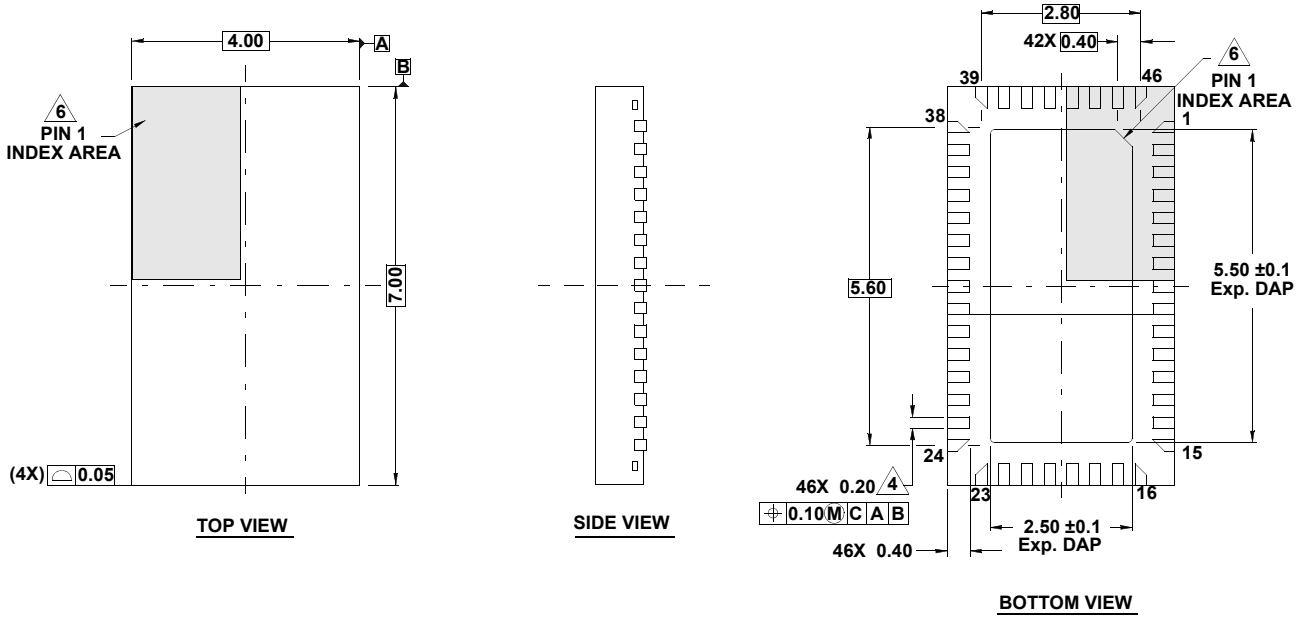
Reliability reports are also available from our website at www.intersil.com/support.

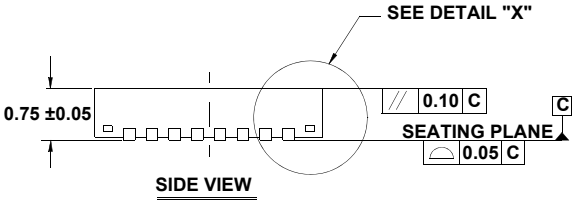
Package Outline Drawing

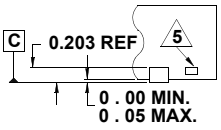
L46.4x7

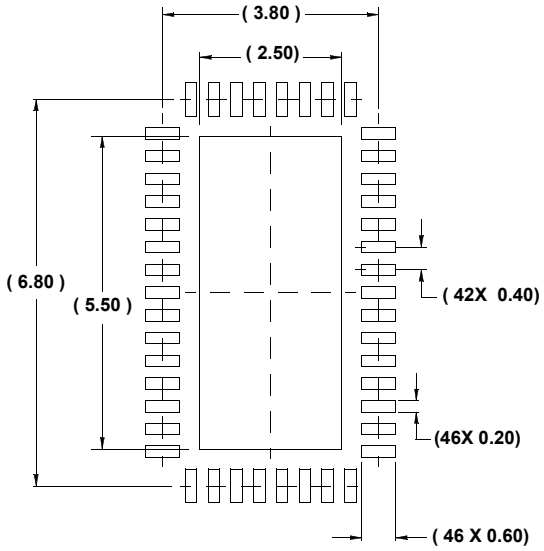
46 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (TQFN)

Rev 1, 3/13









NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.