TEXAS INSTRUMENTS

User's Guide
SLVU243–May 2008

TPS5430EVM-342 2.25-A, Inverting Buck-Boost Regulator Evaluation Module

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1 Introduction

This guide contains TPS5430 background information and TPS5430EVM-342 evaluation module (EVM) support documentation. Also the performance specifications, a schematic diagram, and the bill of materials for the TPS5430EVM-342 are included.

1.1 Background

The TPS5430 dc/dc converter is designed to provide up to a 3.0 A output from an input voltage source of 5.5 V to 36 V. Table 1 provides the rated input voltage and output current range for the evaluation module. This EVM is designed to demonstrate using the TPS5430 regulator in an inverting buck-boost application and does not reflect the entire design range of input and output voltages that can be used with this part. The switching frequency is internally set at a nominal 500k Hz. The high-side MOSFET is incorporated

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inside the TPS5430 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET helps the TPS5430 to achieve high efficiencies and keep the junction temperature low at high output currents. The compensation components are internal to the integrated circuit (IC), whereas an external divider permits an adjustable output voltage. Additionally, the TPS5430 provides an enable input. The absolute maximum input voltage is 24 V.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS5430EVM-342	VIN = 10.8 V to 19.8 V	0 A to 2.25 A

1.2 Reference Information

- *Using a buck converter in an inverting buck-boost topology* (SLYT283) technical brief.
- *Using the TPS5430 As An Inverting Buck Boost Converter* (SLVA257) application report.
- 3-A, WIDE INPUT RANGE, STEP-DOWN SWIFT™ CONVERTER (SLVS632) data sheet for the TPS5430 and TPS5431.

1.3 Performance Specification Summary

Table 2 provides a summary of the TPS5430EVM-342 performance specifications . Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of –5 V, unless otherwise specified. The TPS5430EVM-342 is designed and tested for V_{IN} = 10.8 = V to 19.8 = V. The ambient temperature is 25°C for all measurements, unless otherwise noted. Maximum input voltage for the TPS5430EVM-342 is 24 = V.

Table 2. TPS5430EVM-342 Performance Specification Summary

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN voltage range			10.8	12 or 15	19.8	V
Output voltage set point				-5.0		V
Output current range		V_{IN} = 15 V	0		2.25	A
Load regulation		V_{IN} = 3.3 V, I_O = 0 A to 3 A		±0.02%		
Load transient response	Voltage change	I_O = 0.75 A to 2.25 A		-50		mV
	Recovery time			120		ms
	Voltage change	I_O = 2.25 A to 0.75 A		+50		mV
	Recovery time			120		ms
Loop bandwidth		V_{IN} = 12 V, I_O = 2 A		11.21		kHz
Phase margin		V_{IN} = 12V, I_O = 2 A		73		°
Output ripple voltage		V_{IN} = 12V, I_O = 2 A		100		mVpp
Output rise time				8		ms
Operating frequency				500		kHz
Max efficiency		V_{IN} = 11 V, V_O = -5 V, I_O = 0.8 A		87%		

1.4 Modifications

The TPS5430EVM-342 is designed to demonstrate the TPS5430 configured as an inverting buck-boost converter. A few changes can be made to this module.

1.4.1 Output Voltage Setpoint

To change the output voltage of the EVM, it is necessary to change the value of resistor R3. Changing the value of R3 can change the output voltage below about –1.25 V. The value of R3 for a specific output voltage can be calculated using Equation 1.

$$R2 = 10\ k\Omega \times \frac{1.221\ V}{V_O - 1.221\ V} \quad (1)$$

Table 3 lists the R3 values for some common output voltages. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

CAUTION

V_{IN} must be in a range so that the minimum on-time is greater than 200 ns, and the maximum duty cycle is less than 87%.

Table 3. Output Voltages Available

Output Voltage (V)	R_3 Value (kΩ)
-1.8	21.5
-2.5	9.53
-3.3	5.90
-5	3.24

1.4.2 Input Voltage Range

The EVM is designed to operate from a nominal 12 V, 15 V, or 18 V ± 10% input voltage. The TPS5430 is specified to operate over an input voltage range of 5.5 V to 36 V. The EVM may not be operated over this range without damage as the input bypass capacitor is rated at 25 V. This capacitor was chosen for its small package size. Additionally, the voltage differential from input to output cannot exceed the maximum operating range of the input voltage, 36 V.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS5430EVM-342 evaluation module. The section also includes test results typical for the TPS5430EVM-342 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

2.1 Input / Output Connections

The TPS5430EVM-342 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 3 A should be connected to J1 through a pair of 20 AWG wires. The load should be connected to J2 through a pair of 20 AWG wires. The maximum load current capability should be 2.25 A. Wire lengths should be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the VIN input voltages with TP2 providing a convenient ground reference. TP5 is used to monitor the output voltage with TP4 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN}, 12 V nominal, 10.8 V to 19.8 V
J2	OUT, -5 V at 2.25A maximum
JP1	2-pin header for enable. Connect EN to the -5 V output to disable, open to enable.
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	PH test point
TP4	GND test point at OUT connector

Table 4. EVM Connectors and Test Points (continued)

Reference Designator	Function
TP5	Output voltage test point at OUT connector
TP6	Test point between voltage divider network and R1. Used for loop response measurements.

2.2 Efficiency

The TPS5430EVM-342 efficiency peaks at load current of about 0.8 A, and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPS5430EVM-342 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs.

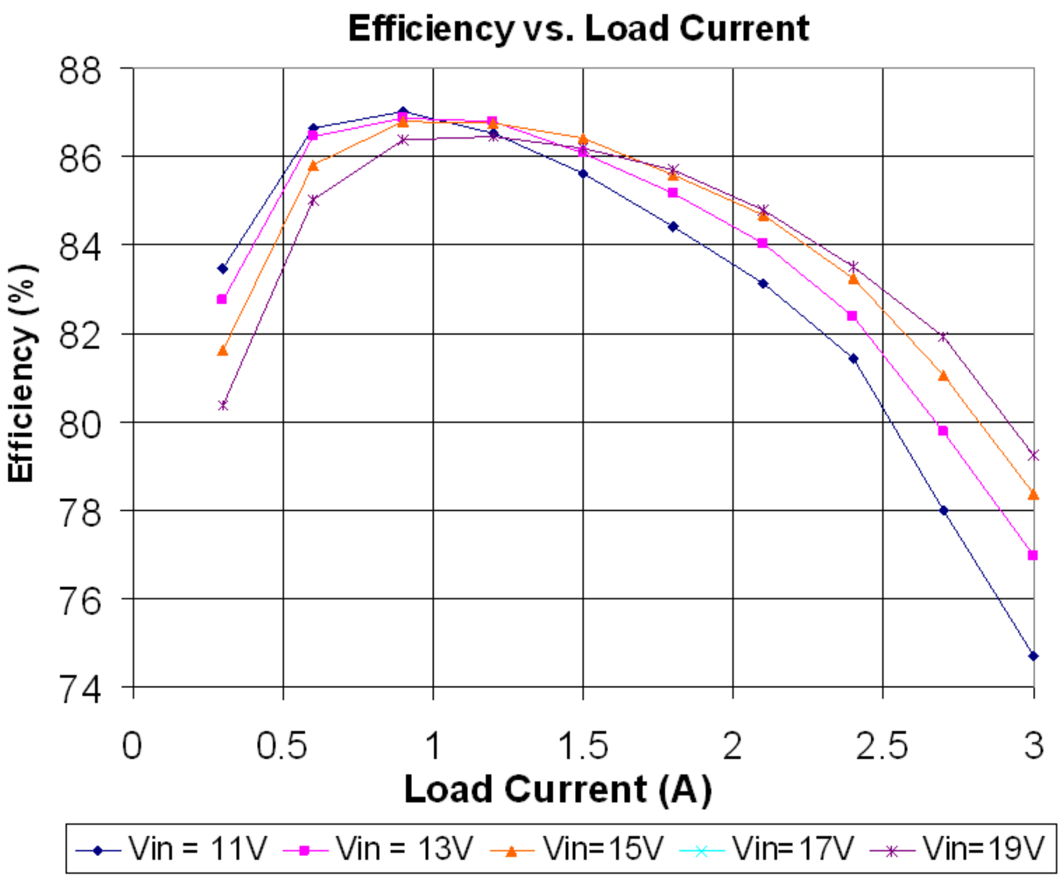

Figure 1. Measured Efficiency, TPS5430

2.3 Output Voltage Regulation

Figure 2 displays the output voltage load regulation of the TPS5430EVM-342. Measurements were taken at 25°C ambient temperature.

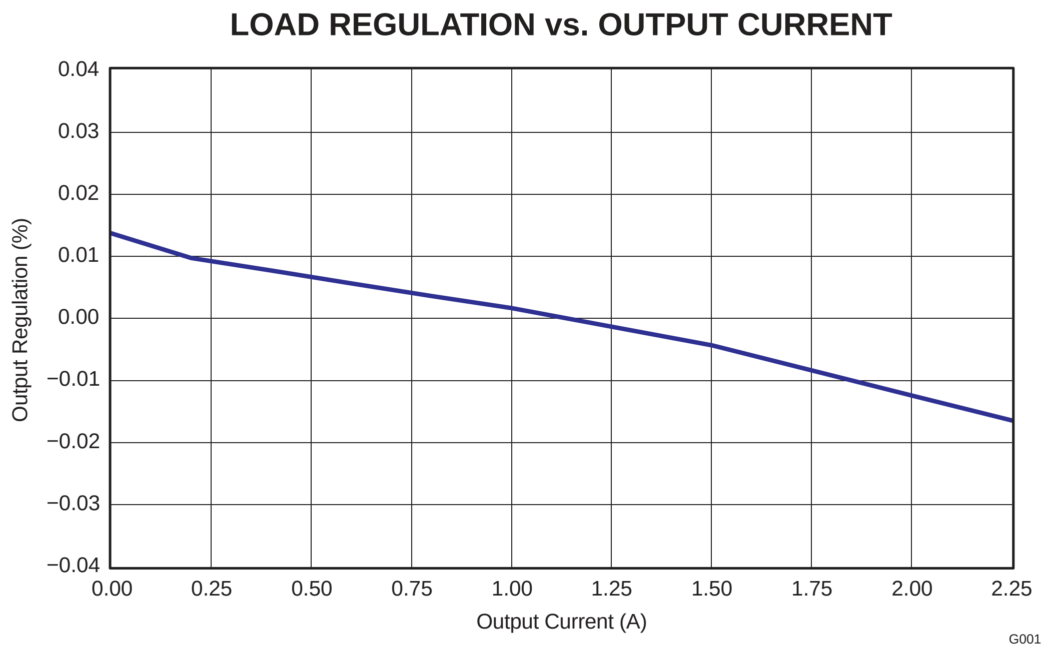

Figure 2. Load Regulation

2.4 Load Transients

Figure 3 shows the TPS5430EVM-342 response to load transients. The current step is from 25% to 100% of maximum-rated load. Total peak-to-peak voltage variation is shown with ripple and noise on the output.

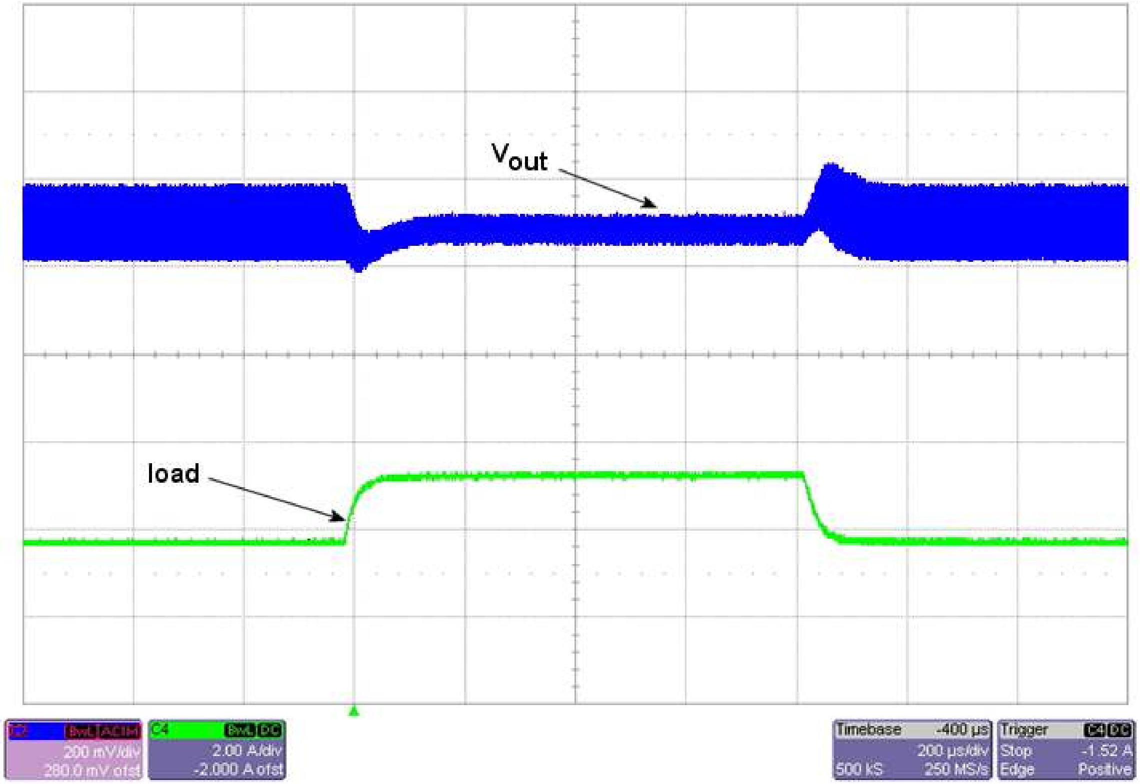

Figure 3. Load Transient Response, TPS5430

2.5 Loop Characteristics

Figure 4 shows the TPS5430EVM-342 loop-response characteristics . Gain and phase plots display the V_{IN} voltage of 10.8 V and 19.8 V.

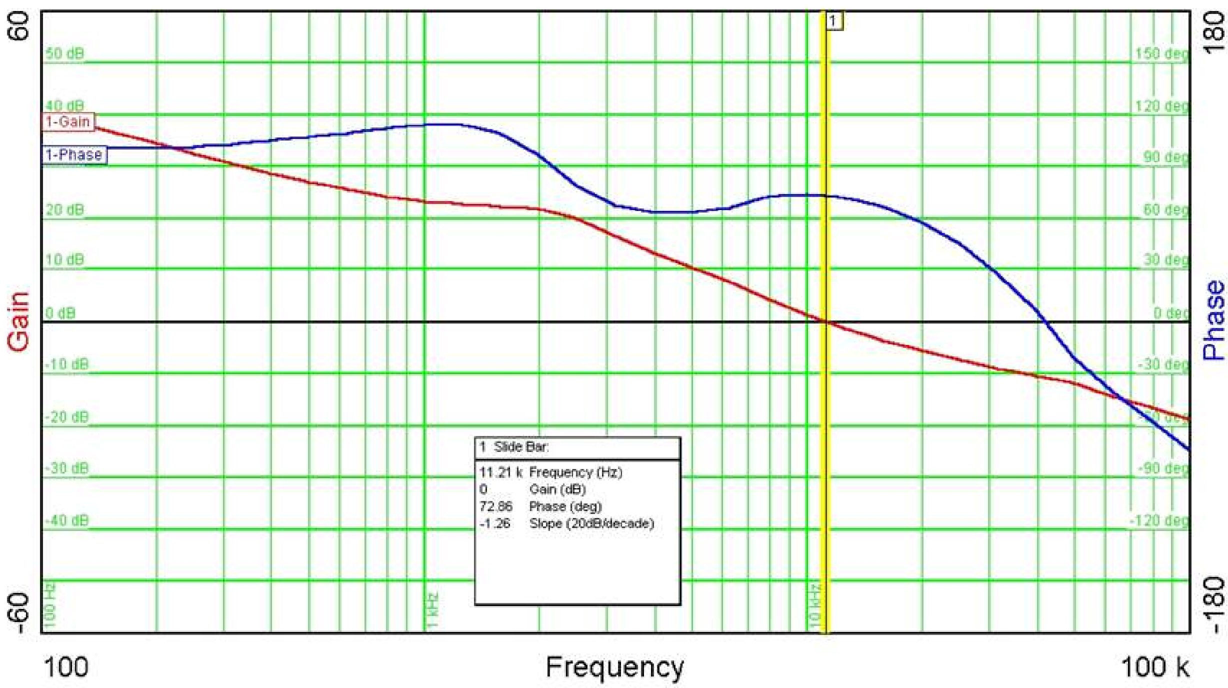

Figure 4. Measured Loop Response, TPS5430, V_{IN} = 12 V

2.6 Output Voltage Ripple

Figure 5displays the TPS5430EVM-342 output voltage ripple. The input voltage is V_{IN} = 12 V for the TPS5430. Output current is the rated full load of 3 A. Voltage is measured directly across output capacitors.

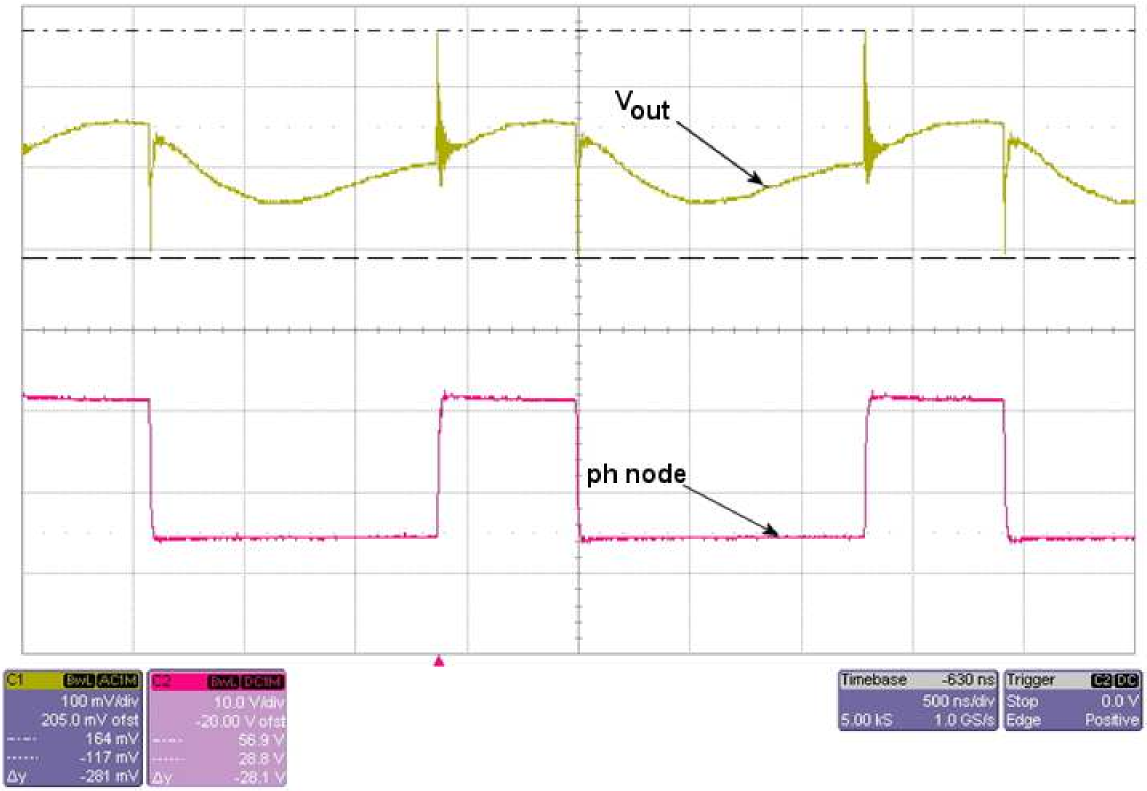

Figure 5. Measured Output Voltage Ripple, TPS5430

2.7 Powering Up

Figure 6 provides the TPS5430EVM-342 start-up waveforms. The top trace shows V_{IN} whereas the bottom trace shows V_{OUT}. V_{IN} charges up from 0 V toward 12 V. When the input voltage reaches the internally set UVLO threshold voltage, the slow-start sequence begins. After a delay, the internal reference begins to ramp up linearly at the internally set slow-start rate towards 1.221 V, and the output ramps up toward the set voltage of 5 V. The output can be inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, EN is released and the slow-start voltage begins to ramp up at the internally set rate. When the EN voltage reaches the enable-threshold voltage of 1.06 V, the start-up sequence begins as described.

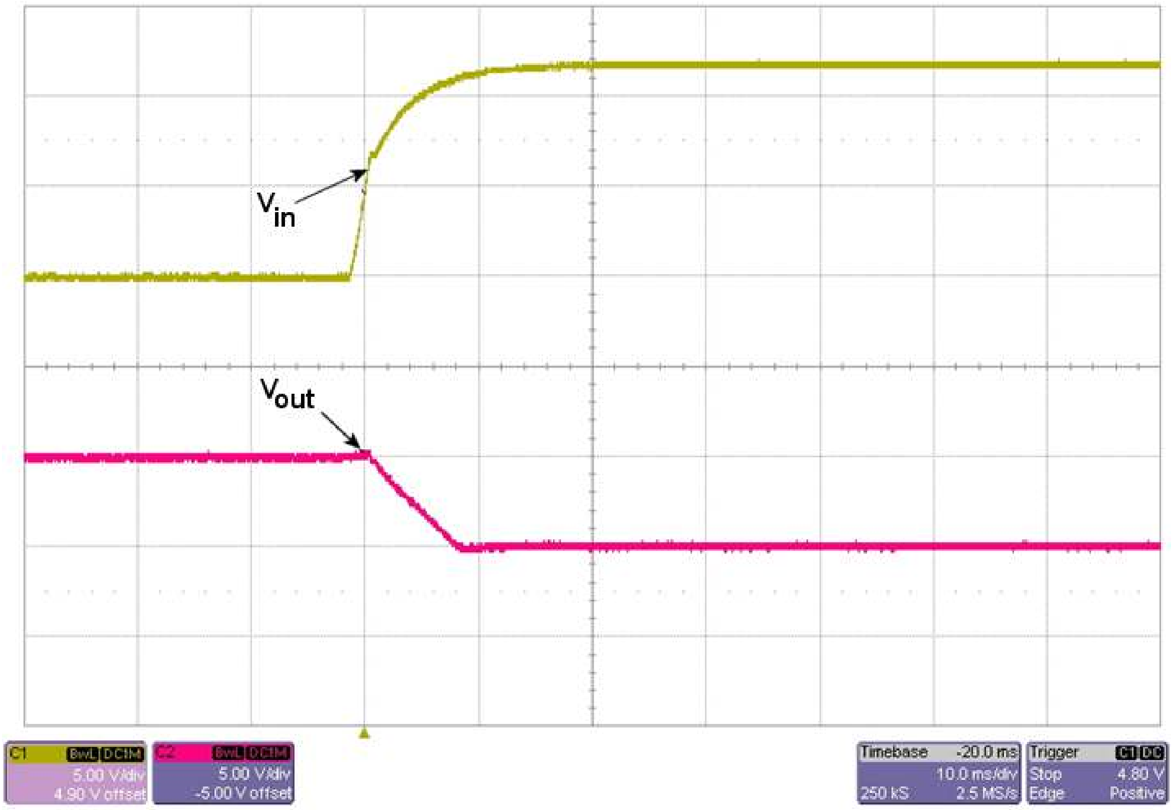

Figure 6. Power Up, V_{OUT} Relative to V_{IN}

3 Board Layout

This section describes the TPS5430EVM-342 board layout and layer illustrations.

3.1 Layout

Figure 7 through Figure 9 display the board layout for the TPS5430EVM-342. The topside layer of the TPS5430EVM-342 is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS5430 and a large area filled with ground. The bottom layer contains ground and some signal routing. The top and bottom and internal ground traces are connected with multiple vias placed around the board including four vias directly under the TPS5430 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitor (C1) and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the voltage set point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, adjacent to the output capacitor C3.

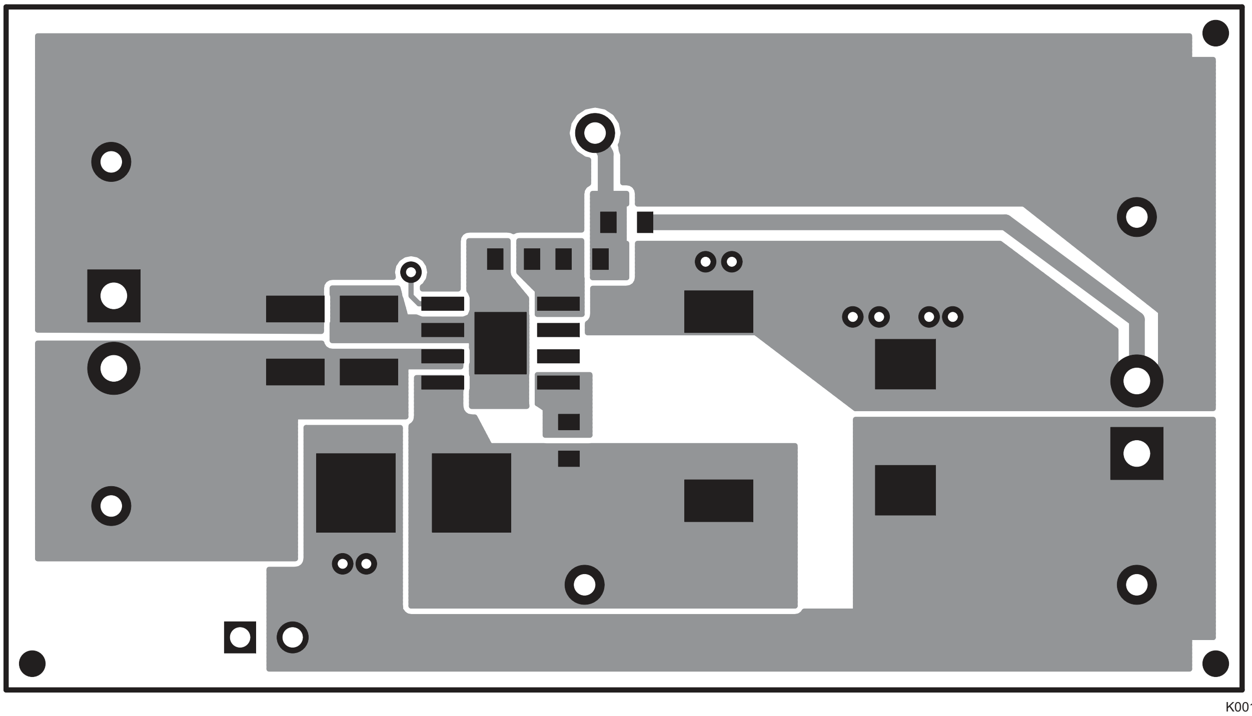

Figure 7. Top-side Layout

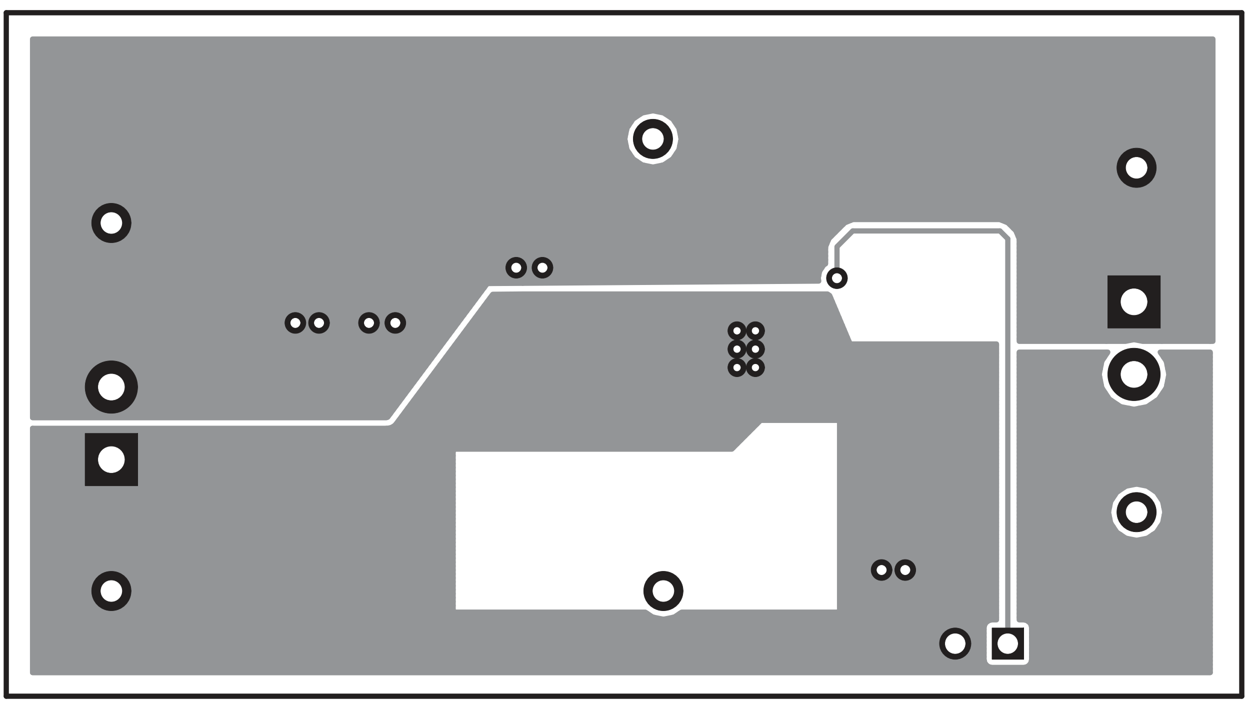

Figure 8. Bottom-side Layout (View from Top Side)

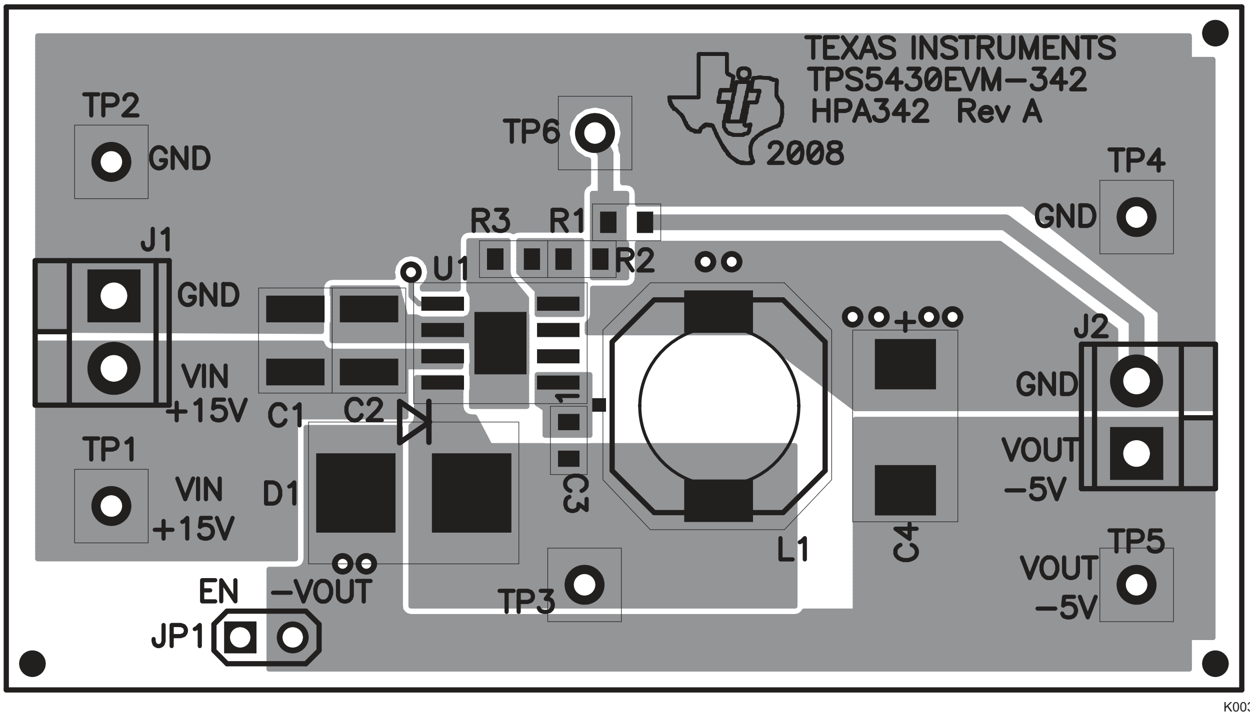

Figure 9. Top-side Assembly

4 Schematic and Bill of Materials

This section describes the TPS5430EVM-342 schematic and itemizes the bill of materials.

4.1 Schematic

Figure 10 displays the TPS5430EVM-342 schematic.

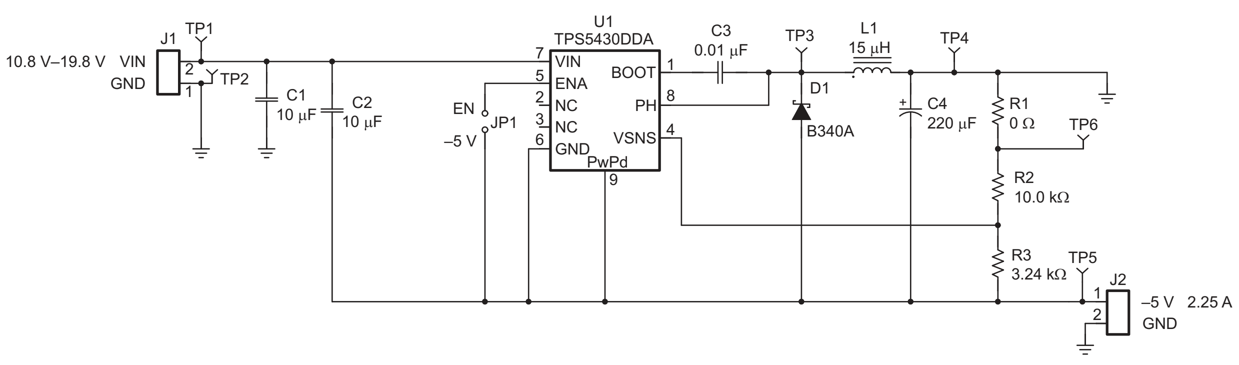

Figure 10. TPS5430EVM-342 Schematic

4.2 Bill of Materials

Table 5 itemizes the TPS5430EVM-342 bill of materials.

Table 5. TPS5430EVM-342 Bill of Materials

Count	REF DES	Value	Description	Size	Part Number	MFR
2	C1, C2	10 µF	Capacitor, Ceramic, 25 V, X7R, 10%	1210	C3225X7R1E106K	TDK
1	C3	0.01 µF	Capacitor, Ceramic, 50 V, X7R, 10%	0603	C1608X7R1H103K	TDK
1	C4	220 µF	Capacitor, POSCAP, 10 V, 40 milliohm, 20%	7343(D)	10TPB220M	Sanyo
1	D1	B340A	Diode, Schottky Barrier Rectifier, 3 A, 40 V	SMA	B340A	Diodes Inc
2	J1, J2	ED1514	Terminal Block, 2 pin, 6 A, 3.5 mm	0.27 x 0.25	ED1514	OST
1	JP1	PTC36SAAN	Header, 2-pin, 100 mil spacing, (36-pin strip)	0.100 inch x 2	PTC36SAAN	Sullins
1	L1	15 µH	Inductor, SMT, 3.4 A, 41 milliohm	0.405 sq inch	CDRH105R-150	Sumida
1	R1	0 Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	10.0 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	3.24 kΩ	Resistor, Chip, 1/16W, 5%	0603	Std	Std
4	TP1, TP3, TP5, TP6	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
2	TP2, TP4	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	TPS5430DDA	IC, Switching Step-Down Regulator, 5.5 V - 36 V, 3 A	SO8[DDA]	TPS5430DDA	TI
1	–		PCB, 1.3 inch x 2.35 inch x 0.062 In		HPA136	Any
1	–		Shunt, 100 mil, Black	0.100	929950-00	3M

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 10.8 V to 19.8 V and the output voltage range of fixed at –5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 90°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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