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FDMS2D4N03S

N-Channel PowerTrench[®] SyncFETTM 30 V, 163 A, 1.8 m Ω

Features

- Max $r_{DS(on)}$ = 1.8 m Ω at V_{GS} = 10 V, I_D = 28 A
- Max $r_{DS(on)}$ = 2.34 m Ω at V_{GS} = 4.5 V, I_D = 26 A
- High Performance Technology for Extremely Low r_{DS(on)}
- SyncFETTM Schottky Body Diode
- 100% UIL Tested
- RoHS Compliant

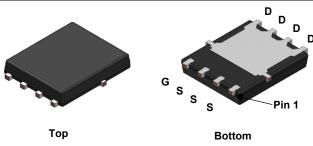
General Description

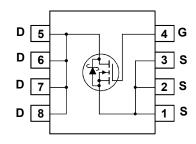
The FDMS2D4N03S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{\text{DS}(\text{on})}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic schottky body diode.

Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/ GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification







Power 56

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter			Ratings	Units	
V_{DS}	Drain to Source Voltage			30	V	
V_{GS}	Gate to Source Voltage			±16	V	
	Drain Current -Continuous	T _C = 25 °C	(Note 5)	163		
	-Continuous	T _C = 100 °C	(Note 5)	103		
'D	-Continuous	T _A = 25 °C	(Note 1a)	28	Α	
	-Pulsed		(Note 4)	694		
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	175	mJ	
В	Power Dissipation	T _C = 25 °C		74	w	
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.5	VV	
T _J , T _{STG}	Operating and Storage Junction Tempera	ture Range		-55 to +150	°C	

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a	50	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS2D4N03S	FDMS2D4N03S	Power 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	acteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, referenced to 25 °C		18		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			500	μΑ
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±16 V, V _{DS} = 0 V			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 1 \text{ mA}$	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 10 mA, referenced to 25 °C		-4		mV/°C
		V _{GS} = 10 V, I _D = 28 A		1.4	1.8	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 26 \text{ A}$		1.7	2.34	mΩ
()		$V_{GS} = 10 \text{ V}, I_D = 28 \text{ A}, T_J = 125 ^{\circ}\text{C}$		2.0	2.8	1
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 28 A		200		S

Dynamic Characteristics

C _{iss}	Input Capacitance	\\ -45\\\\ -0\\		4670	6540	pF
Coss	Output Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		1395	1955	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 WILL		63	120	pF
R _a	Gate Resistance		0.1	0.5	1.5	Ω

Switching Characteristics

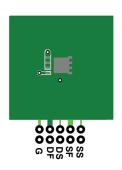
t _{d(on)}	Turn-On Delay Time		15	28	ns
t _r	Rise Time	V _{DD} = 15 V, I _D = 28 A,	4	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	38	61	ns
t _f	Fall Time		3	10	ns
Q_g	Total Gate Charge	V _{GS} = 0 V to 10 V	63	88	nC
Q_{g}	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $V_{DD} = 15 \text{ V}$	28	40	nC
Q _{gs}	Gate to Source Charge	I _D = 28 A	9.8		nC
Q_{gd}	Gate to Drain "Miller" Charge		4.9		nC

Drain-Source Diode Characteristics

V	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.1 A (Note 2)	0.65	1.2	V
V_{SD}	Source to Drain blode 1 of ward voltage	$V_{GS} = 0 \text{ V}, I_S = 28 \text{ A}$ (Note 2)	0.78	1.3	· •
t _{rr}	Reverse Recovery Time	I _E = 28 A, di/dt = 300 A/μs	37	59	ns
Q_{rr}	Reverse Recovery Charge	1 _F - 20 A, αι/αι - 300 Α/μs	51	81	nC

Notes:

^{1.} R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0CA} is determined by the user's board design.



50 °C/W when mounted on a 1 in² pad of 2 oz copper



125 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.
 3. E_{AS} of 175 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 10.8 A, V_{DD} = 30 V, V_{GS} =10 V. 100% test at L = 0.1 mH, I_{AS} = 33 A.
 4. Pulsed Id please refer to Fig 11 SOA graph for more details.
 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted.

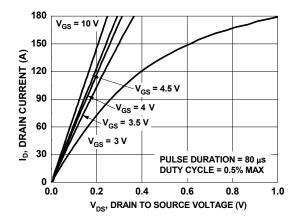


Figure 1. On Region Characteristics

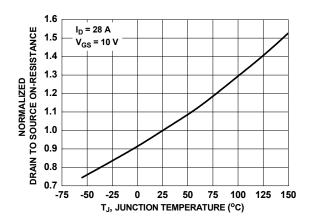


Figure 3. Normalized On Resistance vs. Junction Temperature

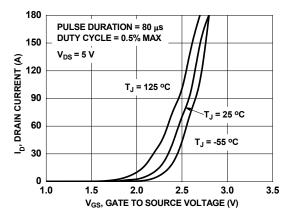


Figure 5. Transfer Characteristics

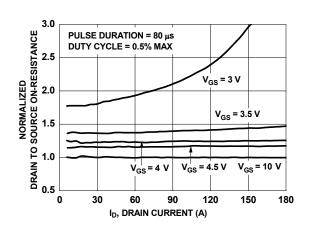


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

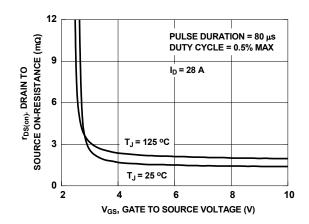


Figure 4. On-Resistance vs. Gate to Source Voltage

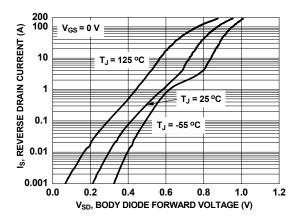


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

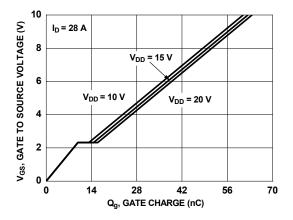


Figure 7. Gate Charge Characteristics

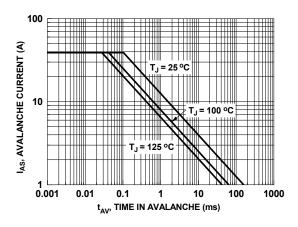


Figure 9. Unclamped Inductive Switching Capability

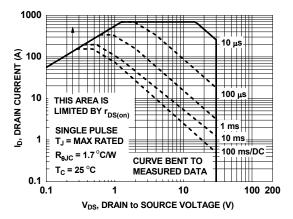


Figure 11. Forward Bias Safe Operating Area

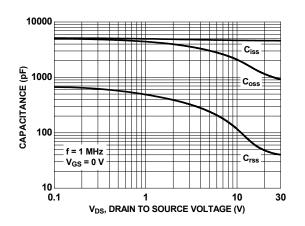


Figure 8. Capacitance vs. Drain to Source Voltage

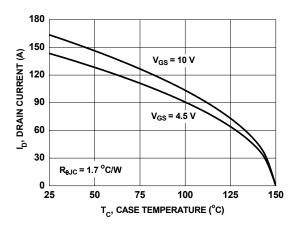


Figure 10. Maximum Continuous Drain Current vs Case Temperature

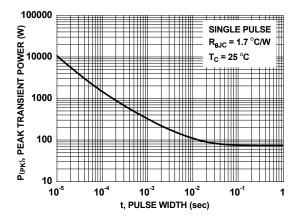


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

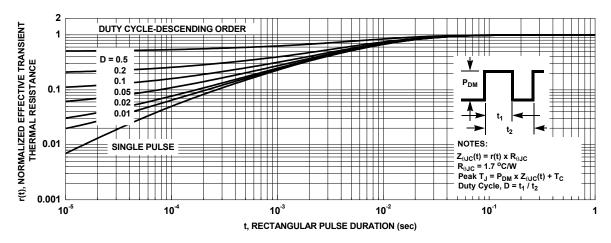


Figure 13. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFETTM Schottky body diode Characteristics

Fairchild's SyncFETTM process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS2D4N03S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

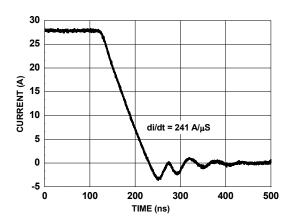


Figure 14. FDMS2D4N03S SyncFETTM Body Diode Reverse Recovery Characteristic

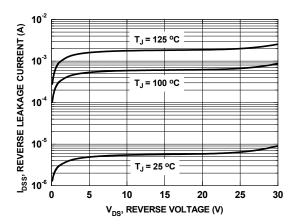
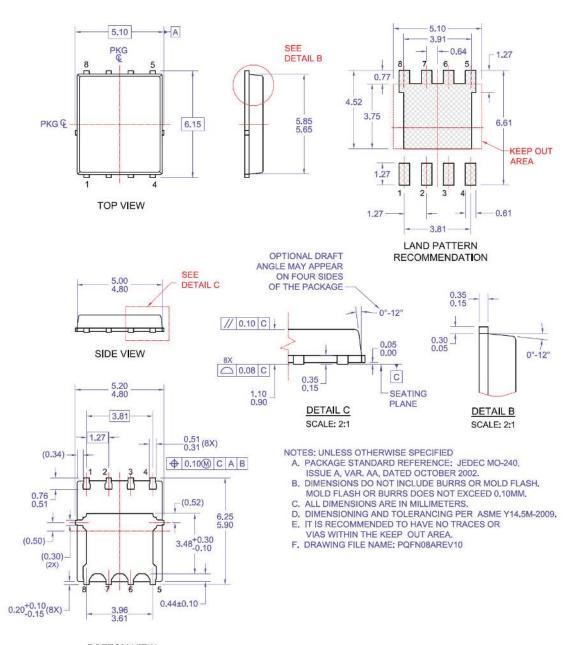


Figure 15. SyncFETTM Body Diode Reverse Leakage vs. Drain-Source Voltage

Dimensional Outline and Pad Layout



BOTTOM VIEW

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