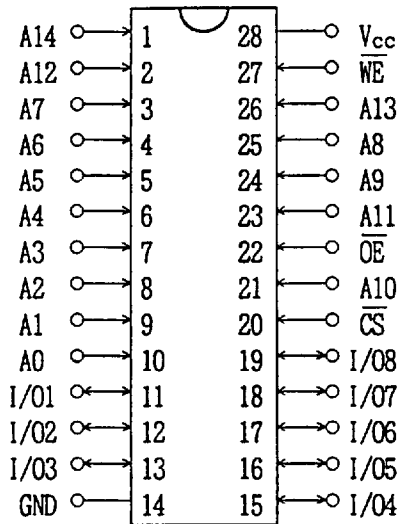


ORDERING INFORMATION

PART NUMBER	PACKAGE	ACCESS TIME (MAX.)	NOTE
μ PD43256BCZ-70X	28-pin Plastic DIP (600mil)	70ns	X-Version Ta=-25 to 85 °C
μ PD43256BCZ-85X	"	85ns	" "
μ PD43256BCZ-10X	"	100ns	" "
μ PD43256BCZ-70Y	"	70ns	Y-Version Ta=-40 to 85 °C
μ PD43256BCZ-85Y	"	85ns	" "
μ PD43256BCZ-10Y	"	100ns	" "
μ PD43256BGU-70X	28-pin Plastic SOP	70ns	X-Version Ta=-25 to 85 °C
μ PD43256BGU-85X	"	85ns	" "
μ PD43256BGU-10X	"	100ns	" "
μ PD43256BGU-70Y	"	70ns	Y-Version Ta=-40 to 85 °C
μ PD43256BGU-85Y	"	85ns	" "
μ PD43256BGU-10Y	"	100ns	" "

PIN CONFIGURATION

28-pin Plastic DIP/SOP
(TOP VIEW)



- A0 to A14 : Address input
- I/O1 to I/O8 : Data input/Output
- \overline{CS} : Chip Select Input
- \overline{WE} : Write Enable Input
- OE : Output Enable Input
- V_{cc} : Power Supply (+5 V)
- GND : Ground
- NC : No Connection

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}		-0.5 ^{Note} to +7.0	V
Input/Output Voltage	V_T		-0.5 ^{Note} to $V_{CC}+0.5$	V
Operating Temperature	V_{opt}	X-Version	-25 to +85	°C
		Y-Version	-40 to +85	°C
Storage Temperature	V_{stg}		-55 to +125	°C

Note: -3.0V MIN. (Pulse Width 50ns)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V_{CC}	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4		$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}	-0.3 ^{Note}		0.6	V
Ambient Temperature	T_a	-X	-25	85	°C
		-Y	-40	85	

Note: -3.0V MIN. (Pulse Width 50ns)

C CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Leakage Current	I_{LI}	$V_{IN}=0$ to V_{CC}	-1.0		1.0	μA
I/O Leakage Current	I_{LO}	$V_{I/O}=0$ to V_{CC} $\overline{CS}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$	-1.0		1.0	μA
Operating Supply Current	I_{CCA1}	$\overline{CS}=V_{IL}$ MIN. Cycle $I_{I/O}=0$ mA	$\mu PD43256B-70$		45	mA
			$\mu PD43256B-85$		45	mA
			$\mu PD43256B-10$		40	mA
	I_{CCA2}	$\overline{CS}=V_{IL}$, $I_{I/O}=0$ mA			15	mA
	I_{CCA3}	$\overline{CS} \leq 0.2V$, Cycle=1MHz, $I_{I/O}=0$ mA $V_{IL} \leq 0.2V$, $V_{IH} \geq V_{CC}-0.2V$			15	mA
Standby Supply Current	I_{SB}	$\overline{CS}=V_{IH}$			3	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$		0.002	0.2 ^{Note}	mA
Output High Voltage	V_{OH1}	$I_{OH}=-1.0$ mA	2.4			V
	V_{OH2}	$I_{OH}=-0.1$ mA			$V_{CC}+0.5$	V
Output Low Voltage	V_{OL}	$I_{OL}=2.1$ mA			0.4	V

Note T_a : 70°C MAX.0.1mA MAX.

CAPACITANCE (Ta=25 °C, f=1 MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	單位
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{ V}$			8	pF
Input Capacitance	C_{IN}	$V_{IN}=0\text{ V}$			5	pF

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

AC TEST CONDITIONS

- Input Pulse Levels : 0.6 ~ 2.4 V
- Input Pulse Rise and Fall Time : 5 ns
- Timing Reference Levels : 1.5 V
- Output Load : See Fig.1,2.

Fig. 1

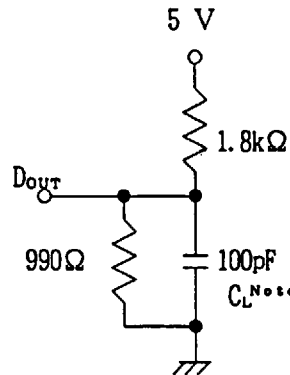
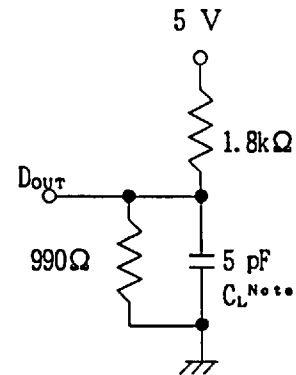


Fig. 2

($t_{CHZ}, t_{OHZ}, t_{CLZ}, t_{OLZ}$
 t_{WHZ}, t_{OW})

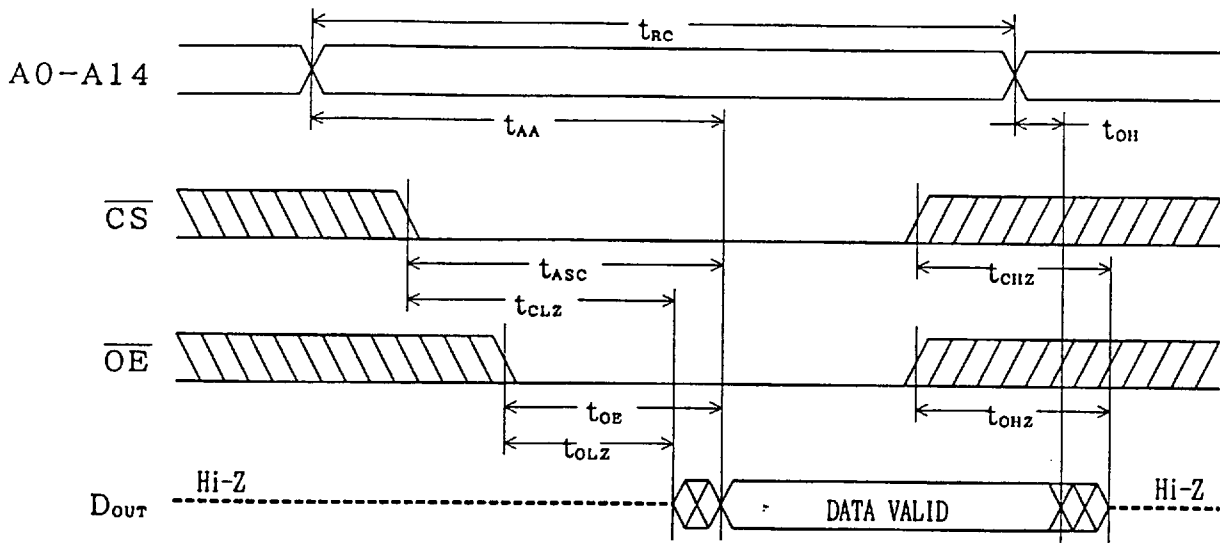


Note: including scope and jig.

READ CYCLE

PARAMETER	SYMBOL	μPD43256B-70		μPD43256B-85		μPD43256B-10		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read cycle Time	t_{RC}	70		85		100		n s
Address Access Time	t_{AA}		70		85		100	n s
Chip Select Access Time	t_{ACS}		70		85		100	n s
Output Enable to Output Valid	t_{OE}		35		40		50	n s
Output Hold from Address Change	t_{OH}	10		10		10		n s
Chip Select to Output in L_{0-z}	t_{CLZ}	10		10		10		n s
Output Enable to Output in L_{0-z}	t_{OLZ}	5		5		5		n s
Chip Select to Output in H_{1-z}	t_{CHZ}		30		30		35	n s
Output Enable to Output in H_{1-z}	t_{OHZ}		30		30		35	n s

READ CYCLE TIMING CHART NOTE1



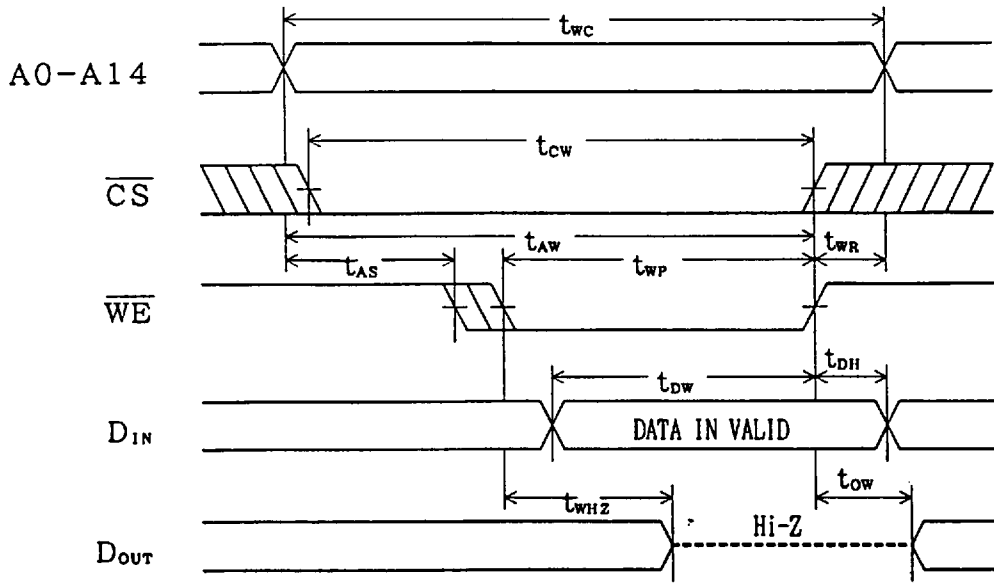
NOTE 1: \overline{WE} is high for read cycle.

WRITE CYCLE

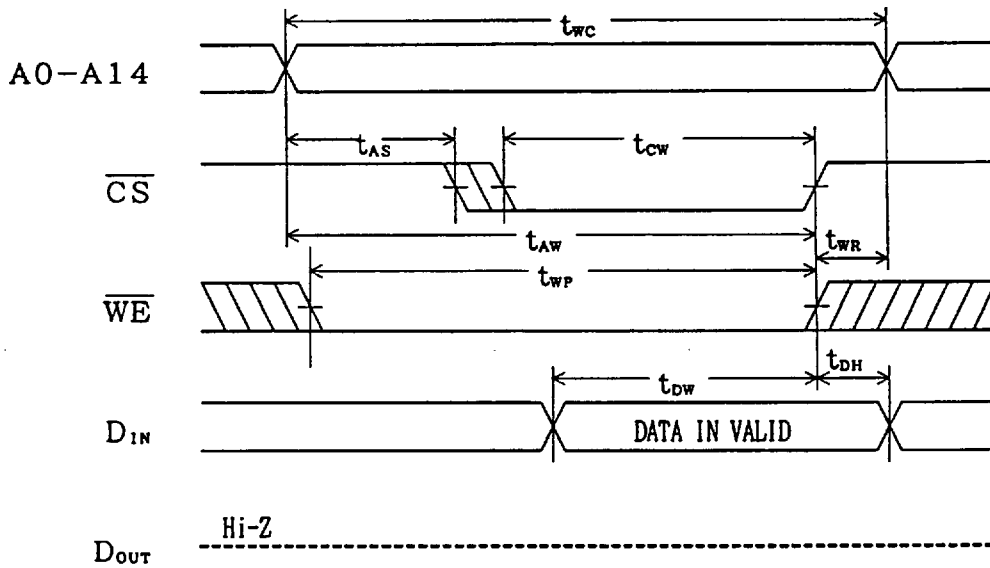
PARAMETER	SYMBOL	$\mu PD43256B-70$		$\mu PD43256B-85$		$\mu PD43256B-10$		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	70		85		100		ns
Chip Select to end of Write	t_{CW}	60		70		80		ns
Address Valid to end of Write	t_{AW}	60		70		80		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	55		65		70		ns
Write Recovery Time	t_{WR}	10		10		10		ns
Data Valid to end of Write	t_{DW}	30		35		40		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Output in H_{I-Z}	t_{WHZ}		30		30		35	ns
Output Active from end of Write	t_{OW}	10		10		10		ns

WRITE CYCLE TIMING CHART

WRITE CYCLE (\overline{WE} CONTROLLED) NOTE 1.2.3



WRITE CYCLE (\overline{CS} CONTROLLED) NOTE 1,2



NOTE1: A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} .

2: \overline{CS} or \overline{WE} must be high during address transition.

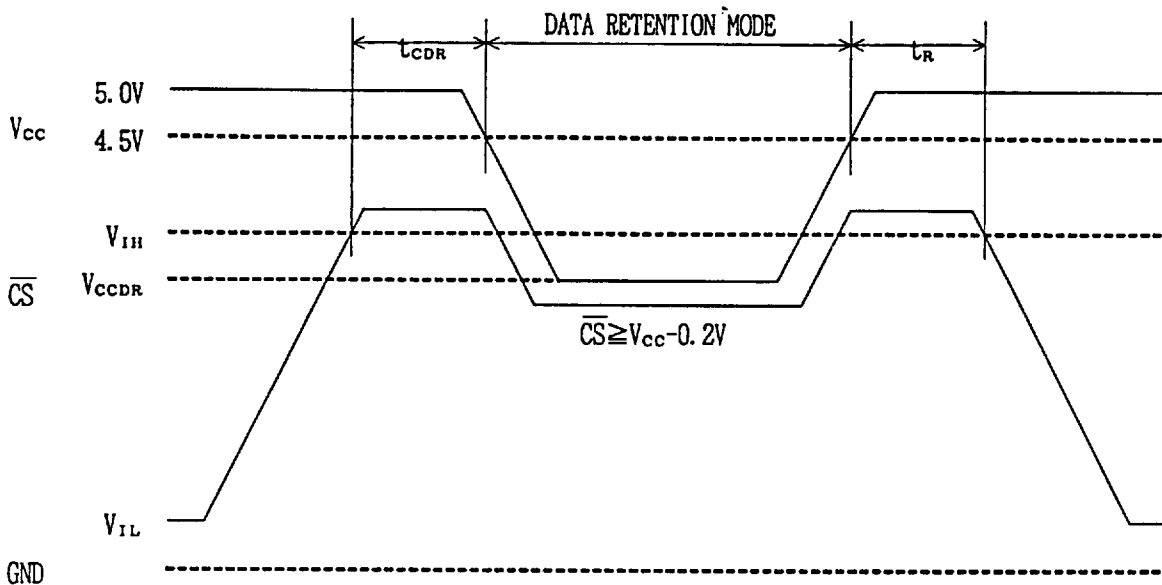
3: If \overline{OE} is high, I/O pins remain in a high impedance state.

LOW V_{CC} DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V _{CCDR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Supply Current	I _{CCDR}	V _{CC} =3.0V, $\overline{CS} \geq V_{CC} - 0.2V$		1	100 ^{Note}	μA
Chip Deselection to Data Retention Mode	t _{CDR}		0			ns
Operation Recovery Time	t _R		5			ms

Note Ta:40°C MAX.15μA MAX.
 Ta:70°C MAX.50μA MAX.

DATA RETENTION TIMING CHART Note



Note: The other inputs (Addresses, \overline{OE} , \overline{WE} , I/Os) can be in a high impedance state.

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