SCOPE: **+5V/Programmable Low-Dropout Voltage Regulator**

Device Type	Generic Number
01	MAX667M(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter		Mil-Std-1835	Case Outline	Package Code
MAXIM	SMD			
JA	P	GDIP1-T8 or CDIP2-T8	8 LEAD CERDIP	J8

Absolute Maximum Ratings

Input Supply Voltage .....+18V
Output Short Circuit to GND ..... 1 sec
LBO Output Sink Current 50mA
LBO Output Voltage ..... GND to V_{OUT}
SHDN Input Voltage ..... -0.3V to (V_{IN}+0.3)V
Input Voltages LBI, SET ..... -0.3V to (V_{IN}-1.0)V

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation .....T_A=+70°C
8 lead CERDIP(derate 8.0mW/°C above +70°C) 640mW

Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC: ..... 55°C/W
Thermal Resistance, Junction to Ambient, ΘJA: ..... 125°C/W

Recommended Operating Conditions.
Ambient Operating Range (T_A) ..... -55°C to +125°C

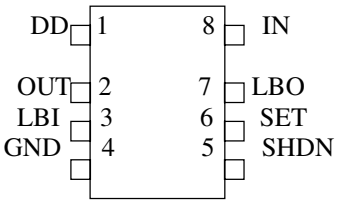
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1 ELECTRICAL TESTS

PARAMETER	Symbol	CONDITIONS -55 °C <=T_A<= +125°C GND=0V, V_{IN}=+9V, V_{OUT}=+5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Input Voltage	V_{IN}		1,2,3	01	3.5	16.5	V
Output Voltage	V_{OUT}	V_{SET}=0V, V_{IN}=6V, I_{OUT}=10mA	1,2,3	01	4.8	5.2	V
Maximum Output Current	I_{OUT}	V_{IN}=6V, 4.5V<V_{OUT}<5.5V	1,2,3	01	250		mA
Quiescent Current	I_Q	V_{SHDN}=2V	1 2,3	01		1 2	µA
		V_{SHDN}=0V, V_{SET}=0V, I_{OUT}=0µA	1 2,3	01		25 35	µA
		V_{SHDN}=0V, V_{SET}=0V, I_{OUT}=100µA	1 2,3	01		30 50	µA
		V_{SHDN}=0V, V_{SET}=0V, I_{OUT}=200µA	1 2,3	01		15 20	mA
Dropout Voltage NOTE 1		I_{OUT}=100µA	1 2,3	01		60 75	mV
		I_{OUT}=200µA	1 2,3	01		250 350	mV
Load Regulation		10mA≤I_{OUT}≤200mA	1 2,3	01		100 250	mV
Line Regulation NOTE 2		6.0V≤V_{IN}≤10V, I_{OUT}=10mA	1 2,3	01		10 15	mV
Set Reference Voltage	V_{SET}		1,2,3	01	1.20	1.28	V
Set Input Leakage Current	I_{SET}	V_{SET}=1.5V	1 2,3	01		±10 ±1000	nA
Output Leakage Current	I_{OUT}	V_{SHDN}=2V	1,2,3	01		1	µA
Short-Circuit Current	I_{OUT}	NOTE 3	1 2,3	01		400 450	mA
Low-Battery Detector Reference Voltage	V_{LBI}		1,2,3	01	1.185	1. 295	V
Low-Battery Detector Input Leakage Current	I_{LBI}	V_{LBI}=1.5V	1 2,3	01		±10 ±1000	nA
Low-Battery Detector Ouput Voltage	V_{LBO}	V_{IN}=9V, V_{LBI}=2V, I_{LBO}=10mA	1 2,3	01		0.25 0.40	V
Shutdown Threshold	V_{SHDN}		1,2,3	01	1.5		V
Shutdown Input Leakage Current	I_{SHDN}	V_{SHDN}= 0 to V_{IN}	1 2,3	01		±10 ±1000	nA
Dropout Detector Output Voltage	V_{DD}	V_{SET}=0V, V_{SHDN}=0V, R_{DD}=100kΩ, V_{IN}=7V, I_{OUT}=10mA	1,2,3	01		0.25	V
		V_{SET}=0V, V_{SHDN}=0V, R_{DD}=100kΩ, V_{IN}=4.5V, I_{OUT}=10mA			4		V

NOTE 1: Dropout voltage is V_{IN}-V_{OUT} when V_{OUT} falls to 0.1V below its value at V_{IN}=V_{OUT}+2V.
NOTE 2: Line Regulation Limit = .05%/V for Subgroup 1 and .075 %/V for Subgroup 2,3.
NOTE 3: Short-Circuit Current is pulsed tested to maintain junction temperature. Short-circuit duration is limited by package dissipation.

	ORDERING INFORMATION.	SMD	PKG.Code
01	MAX667MJA/883B	5962-9212604MPA	J08



TERMINAL NUMBER	FUNCTION	MAX 667 MJA
1	Dropout Detector Output - the collector of a PNP pass transistor. Normally an open circuit, it sources current as dropout is reached.	DD
2	Regulated Output Voltage. OUT falls to 0V when SHDN is above 1.5V. SET determines output voltage when SET is above 50mV; otherwise it is 5V. OUT must be connected to an output filter capacitor.	OUT
3	Low-Battery Detector. A CMOS input to an internal 1.255V comparator whose output is the LBO pin.	LBI
4	Ground.	GND
5	Shutdown Input. Connected to GND for normal operation (output active). Pull above 1.5V to disable OUT, LBO, and DD and to reduce quiescent current to <1µA.	SHDN
6	(Output) Voltage Set, CMOS Input. Connect to GND for 5V output. For other voltages, connect external resistive divider from OUT.	SET
7	Low-Battery Output. An open-drain N-channel transistor that sinks current to GND when LBI is less than 1.22V.	LBO
8	Positive Input Voltage (unregulated)	IN

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3
Group A Test Requirements Method 5005	1, 2, 3
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.