TPS650241EVM

This user's guide describes the characteristics, operation, and use of the TPS650241EVM-234 evaluation module (EVM). This EVM is designed to help the user evaluate and test the various operating modes of the TPS650241. This User's Guide includes setup instructions for the hardware, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

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1 Introduction

The Texas Instruments TPS650241EVM is an integrated Power Management IC for applications that are powered with one Li-Ion or Li-Polymer cell and require multiple power rails. The TPS650241 contains three highly efficient switching step-down converters, three LDOs, and additional status and I/O pins.

1.1 Requirements

No additional components other than the external power supply are needed. See Section 2 – *Setup*.

1.2 Printed Circuit Board Assembly

The TPS650241EVM-234 PCB contains the TPS650241 IC and its required external components. This board contains several jumpers and connectors that allow the user to customize the board for specific operating conditions.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the TPS650241EVM-234.

2.1 Input/Output Connector Descriptions

2.1.1 J2 — VIN

Input voltage from the external power supply, recommended maximum is 5.5V. The input current is dependent on the load, but is typically below 2A.

2.1.2 J5 — GND

This is the return connection for VIN

2.1.3 J1 — VDCDC1

Output from the DCDC1 switching regulator, maximum output current is 1.6A. The default voltage setting is 3.3V.

2.1.4 J3 — GND

Return for VDCDC1.

2.1.5 J4 — VDCDC2

Output from the DCDC2 switching regulator, maximum output current is 1A. The default voltage setting is 2.5V

2.1.6 J6 — GND

Return for VDCDC2.

2.1.7 J7 — VDCDC3

Output from the switching regulator DCDC3, maximum output current is 800mA. The default value is 1.375V.

2.1.8 J8 — GND

Return for VDCDC3.

2.1.9 J9 — VLD01

Output from the low drop out regulator VLDO1, maximum output current is 200mA. The default value is 1.5V.

2.1.10 J10 — GND

Return for VLDO1.

2.1.11 J11 — VLD02

Output from the low drop out regulator VLDO2, maximum output current is 200mA. The default value is 1.5V.

2.1.12 J12 — GND

Return for VLDO2.

2.1.13 J13 — VINLDO/GND

Input voltage from the external power supply, recommended maximum 5.5V. The input current is dependent on the load but is typically below 2A.

The EVM has this input connected to the VDCDC1 output via R11.

2.1.14 J14 — VDD_ALIVE/GND

Output from the low drop out regulator VLDO3, maximum output current is 30mA. The default value is 1.2V.

2.1.15 J5 — $\overline{\text{PWRFAIL}}$

$\overline{\text{PWRFAIL}}$ – Fault occurs when the input voltage is below 3V. It is pulled up to VIN when safe, low for fail.

2.1.16 JP1 — DEF1

Sets the default voltage for DCDC1, 2.8V or 3.3V.

2.1.17 JP2 — DEF2

Sets the default voltage for DCDC2, 1.8V or 2.5V.

2.1.18 JP5 — DEF3

Sets the default voltage for DCDC3, 0.9V or 1.375V.

2.1.19 JP3 — DCDC1 ON/OFF

EN for the DCDC1 converter. The default setting is ON.

2.1.20 JP4 — DCDC2 ON/OFF

EN for the DCDC2 converter. The default setting is ON.

2.1.21 JP6 — DCDC3 ON/OFF

EN for the DCDC3 converter. The default setting is ON.

2.1.22 JP7 — PWM/PFM MODE

PWM or PFM Mode jumper. The default setting is PWM.

2.1.23 JP8 — LDO ON/OFF

EN for both the LDO1 and LDO2 regulators. The default setting is ON.

2.1.24 JP9 — VDD_ALIVE/GND

EN for the VDD_ALIVE low dropout regulator. The default setting is ON.

2.2 Factory Setup

The EVM comes from the factory with the following default settings on the jumpers.

Table 1. Jumper Settings

Jumper	Shunt Location
JP1	Between V-Hi and DEF1
JP2	Between V-Hi and DEF2
JP3	Between ON and DCDC1
JP4	Between ON and DCDC2
JP5	Between V-Hi and DEF3
JP6	Between ON and DCDC3
JP7	Between PWM and MODE
JP8	Between ON and LDO
JP9	Between ON and VDD_ALIVE

3 Board Layout

This section provides the TPS650241EVM-234 board layout and illustrations.

3.1 Layout

Board layout is critical for all switch mode power supplies. Figure 1 through Figure 5 shows the board layout for the TPS650241EVM-234 PWB. The nodes with high switching frequencies and currents are short and are isolated from the noise sensitive feedback circuitry. Careful attention has been given to the routing of high frequency current loops. See the data sheet (SLVS774) for specific layout guidelines.

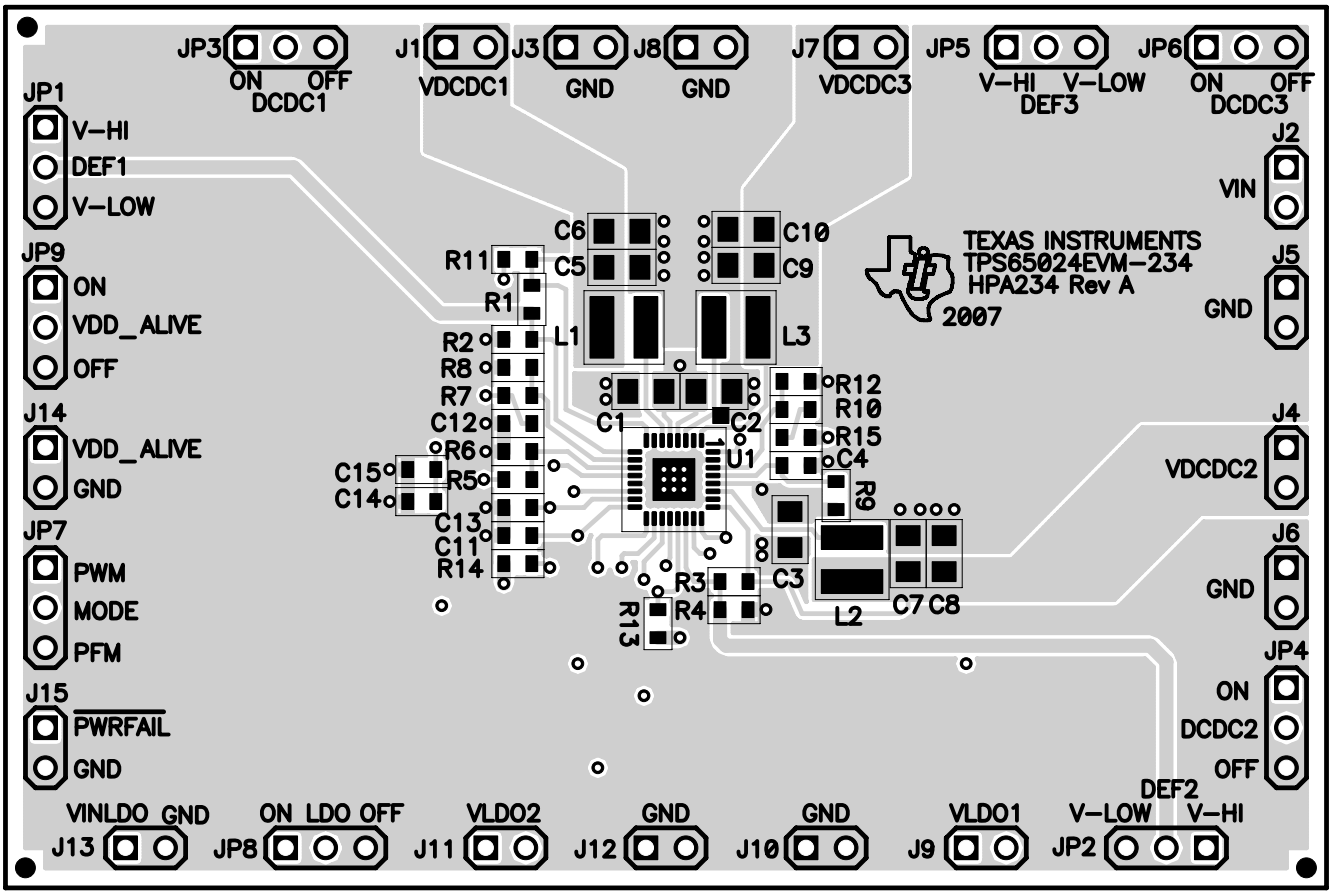

Figure 1. Assembly Layer

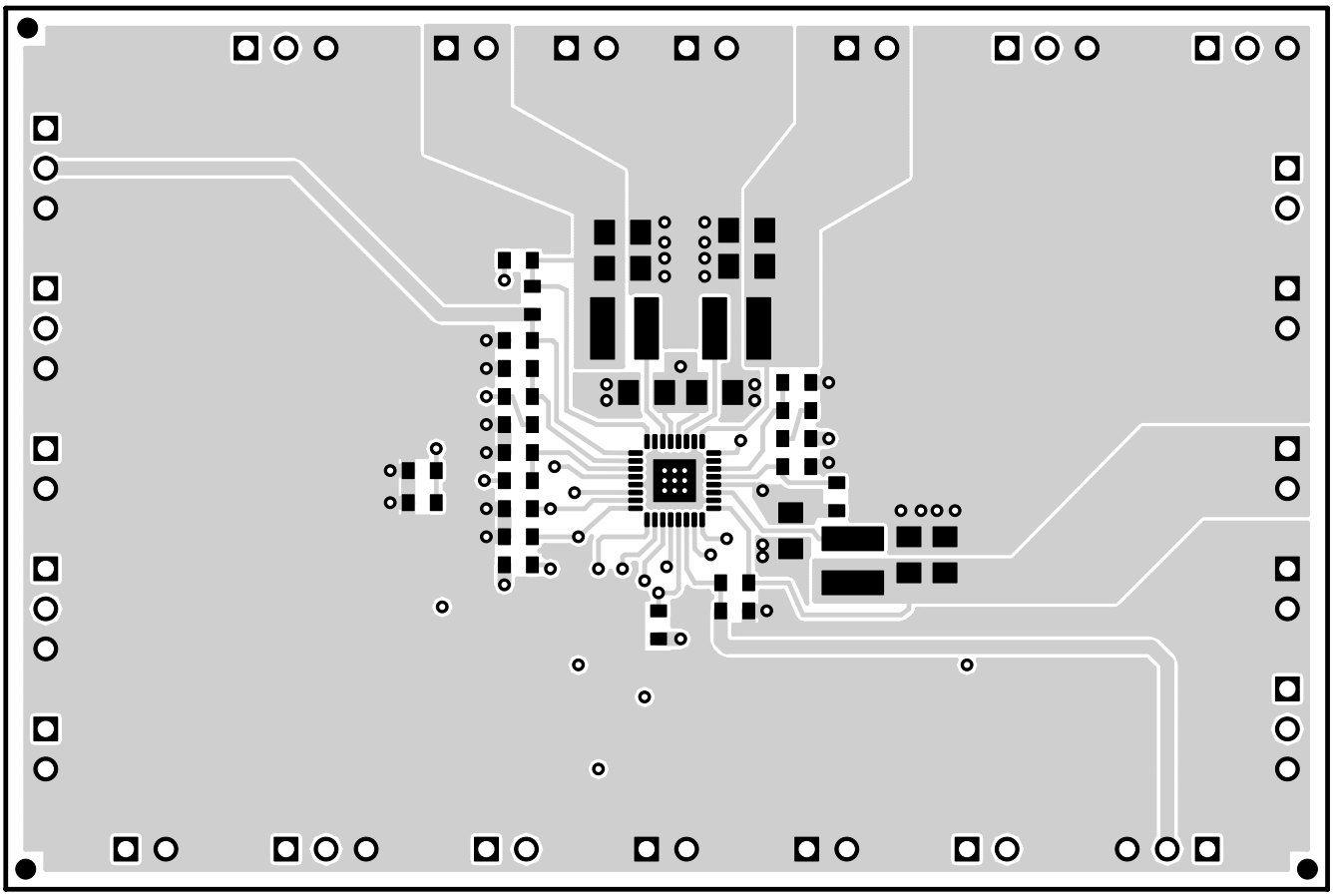

Figure 2. Top Layer Routing

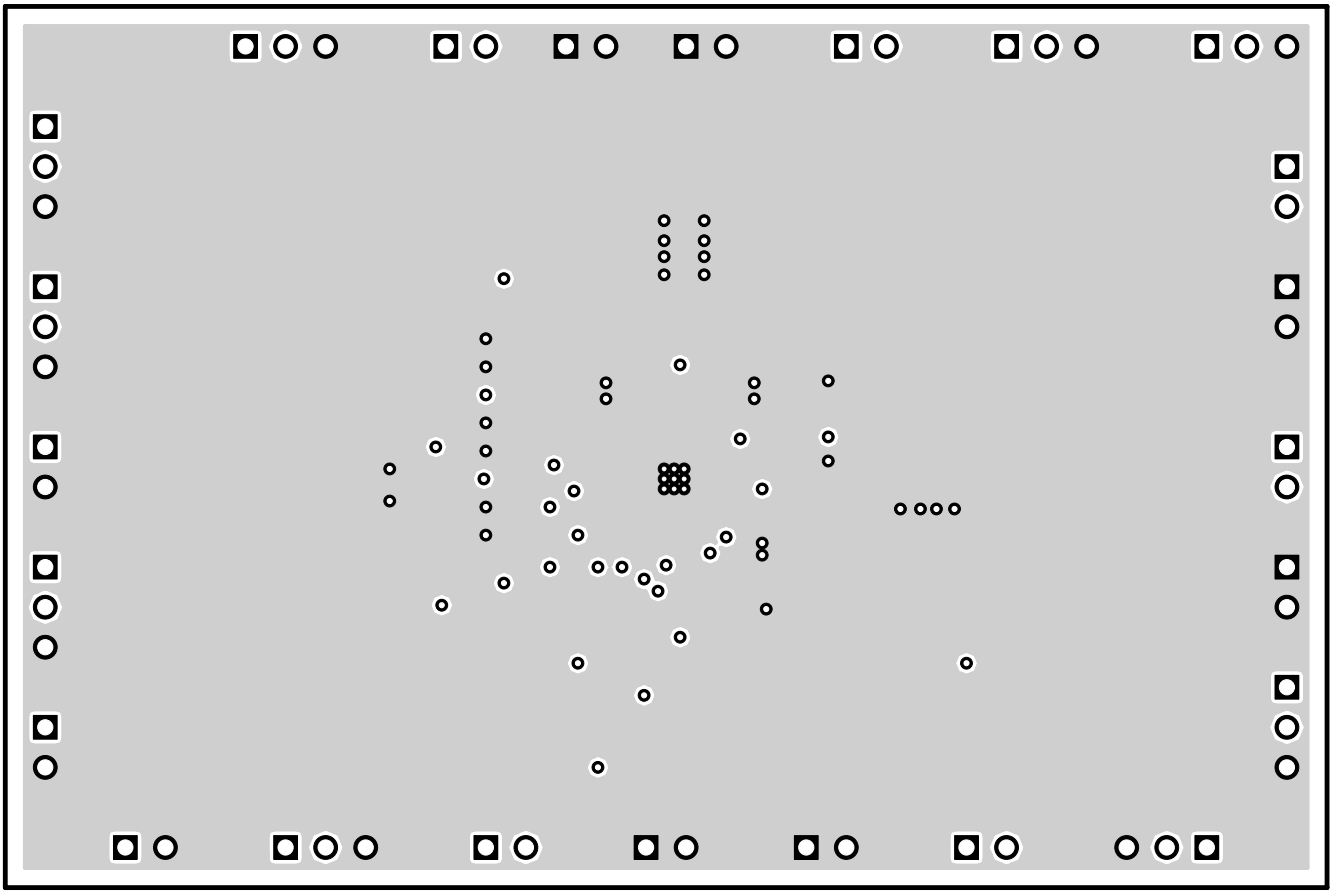

Figure 3. Layer 2, GND Plane

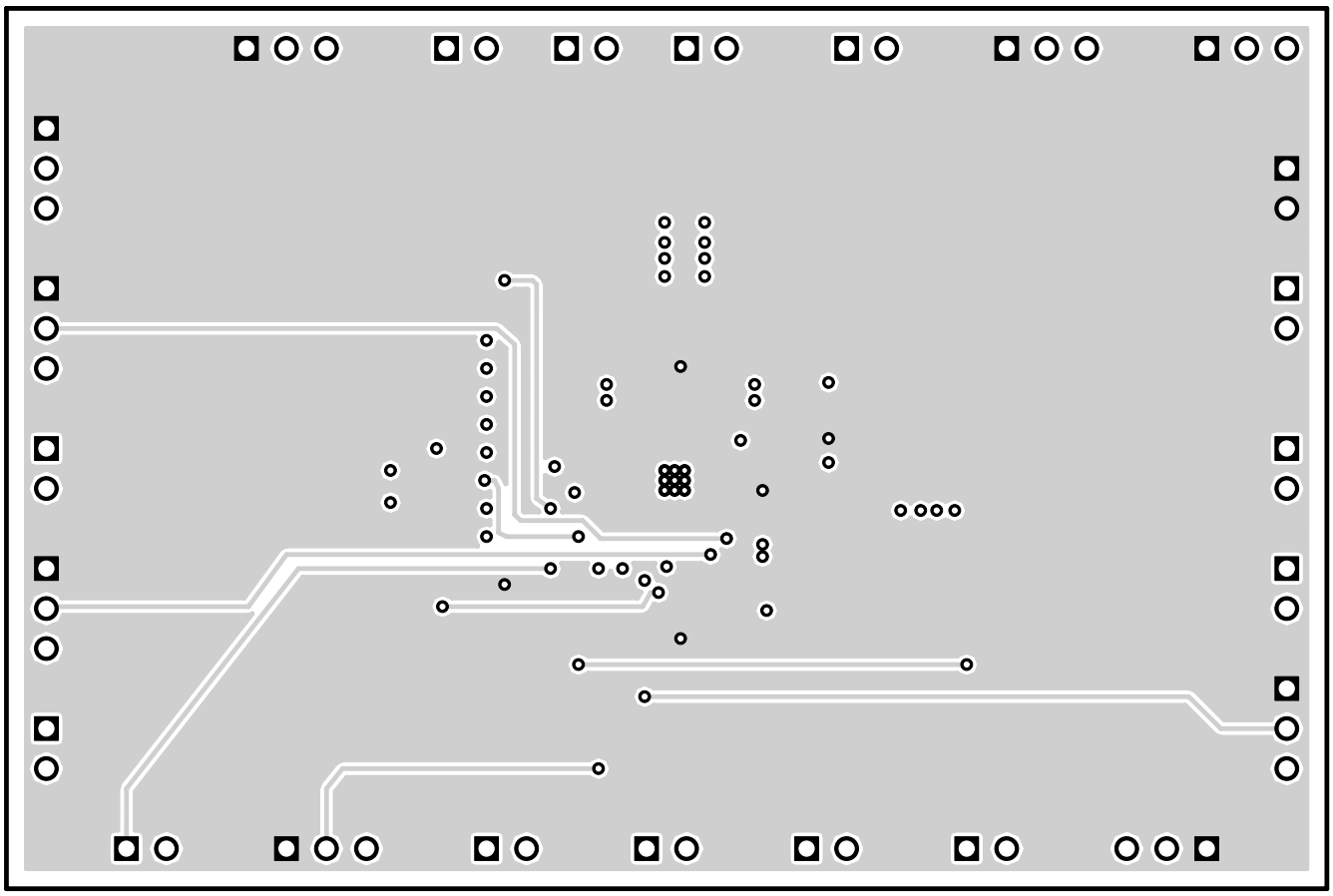

Figure 4. Layer 3 Routing

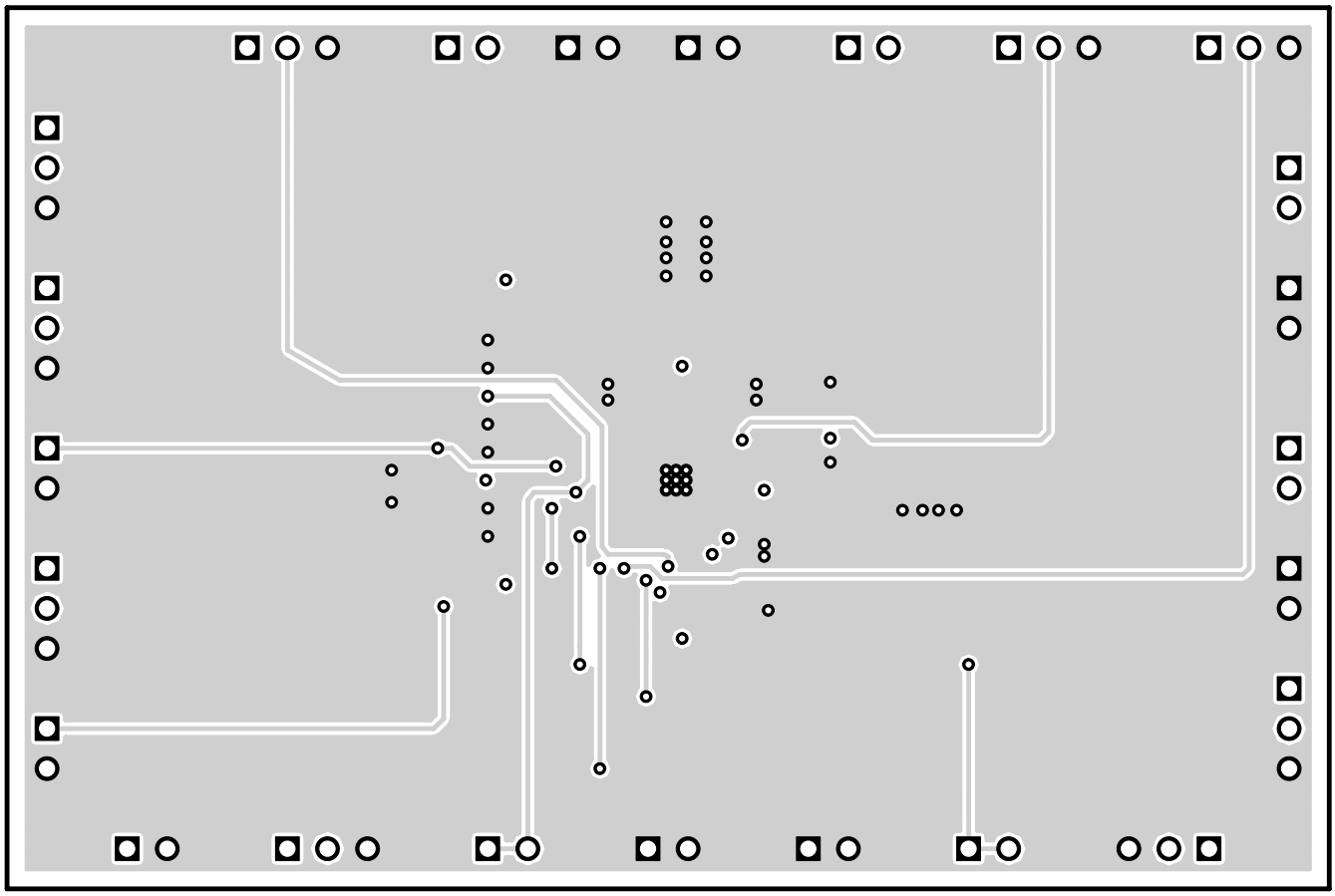

Figure 5. Bottom Layer Routing

4 Schematic and Bill of Materials

This section provides the TPS6650241EVM-234 schematic and bill of materials.

4.1 Schematic

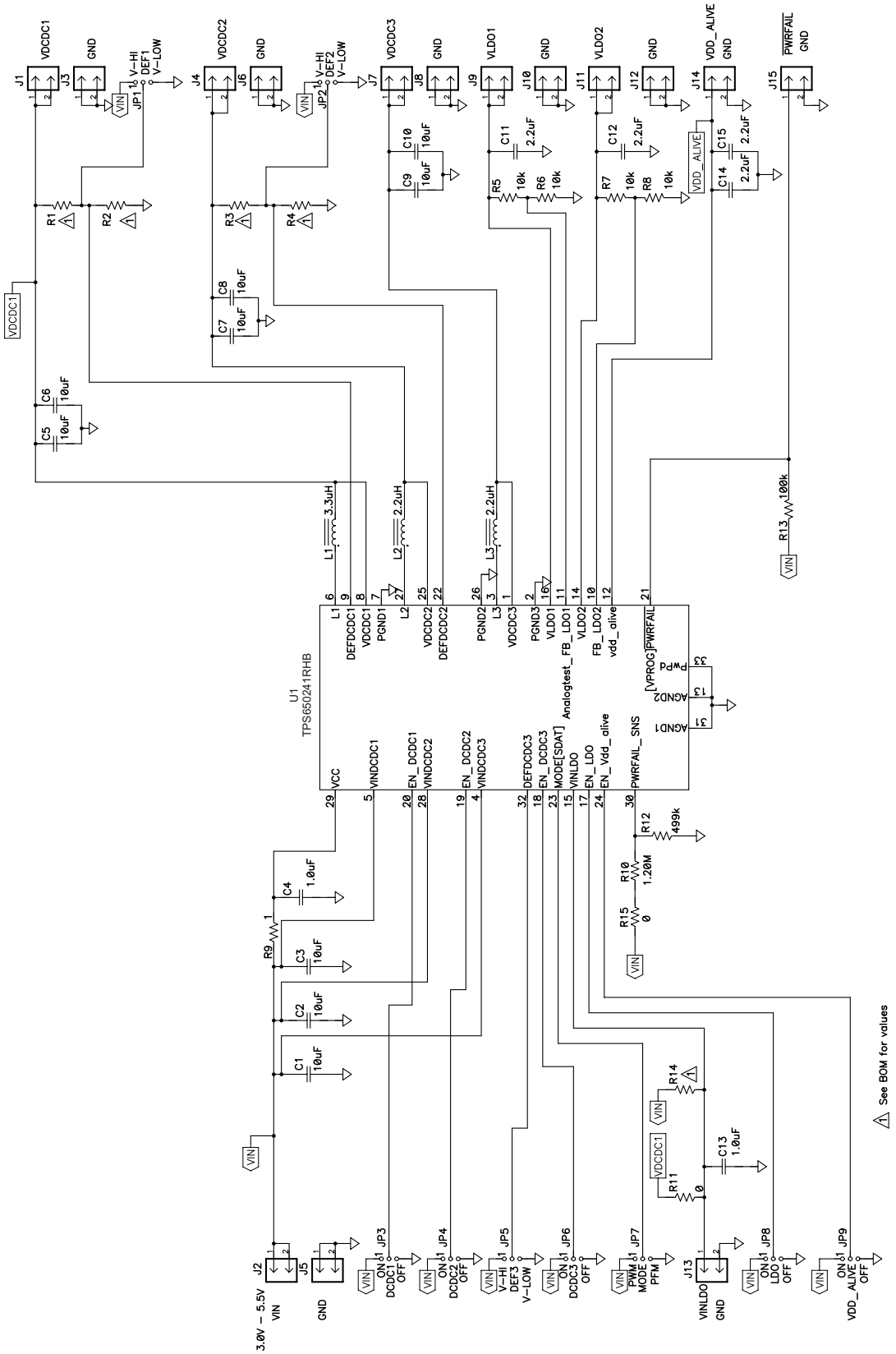

Figure 6. TPS650241EVM-234 Schematic

4.2 Bill of Materials

Table 2. TPS650241EVM-234 Bill of Materials

COUNT	RefDes	Value	Description	Size	Part Number	MFR
9	C1, C2, C3, C5 - C10	10uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0805	C2012X5R0J106K	TDK
2	C11, C12, C14, C15	2.2uF	Capacitor, Ceramic, 6.3V, X5R,10%	0603	C1608X5R0J225K	TDK
2	C4, C13	1.0uF	Capacitor, Ceramic, 6.3V, X5R,10%	0603	C1608X5R0J105K	TDK
15	J1 - J15		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
9	JP1 - JP9		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 x 3	PTC36SAAN	Sullins
1	L1	3.3uH	Inductor, SMT, 1.52A, 78milliohm	0.157 x 0.157	VLCF4020T-3R5N1R5	TDK
2	L2, L3	2.2uH	Inductor, SMT, 1.72A, 59milliohm	0.157 x 0.157	VLCF4020T-2R2N1R7	TDK
0	R1, R2, R3, R4, R14	Open	Resistor, Chip, 1/16W, 1%	0603		
1	R10	1.20M	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R11, R15	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R12	499k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R13	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	R5, R6, R7, R8	10k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	1	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	U1		IC, 3 DC-DC Converters	QFN-32[RTV]	TPS650241RHB	TI
1	--		PCB, 3.3 In x 2.2 In x 0.062 In		HPA234	Any
9	--		Shunt, 100 mil, Black	0.100	929950-00	3M

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1 V to 5.5 V and the output voltage range of 1 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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