# FOUR-PORT USB HUB POWER CONTROLLERS

## FEATURES

- **Complete USB Hub Power Solution**
- **Meets USB Specifications 1.1 and 2.0**
- **Independent Thermal and Short-Circuit Protection**
- **3.3-V Regulator for USB Hub Controller**
- **Overcurrent Logic Outputs**
- **4.5-V to 5.5-V Operating Range**
- **CMOS- and TTL-Compatible Enable Inputs**
- **185 µA Bus-Power Supply Current**
- **Available in 32-Pin HTSSOP PowerPAD™ Package**
- **–40°C to 85°C Ambient Temperature Range**

## DESCRIPTION

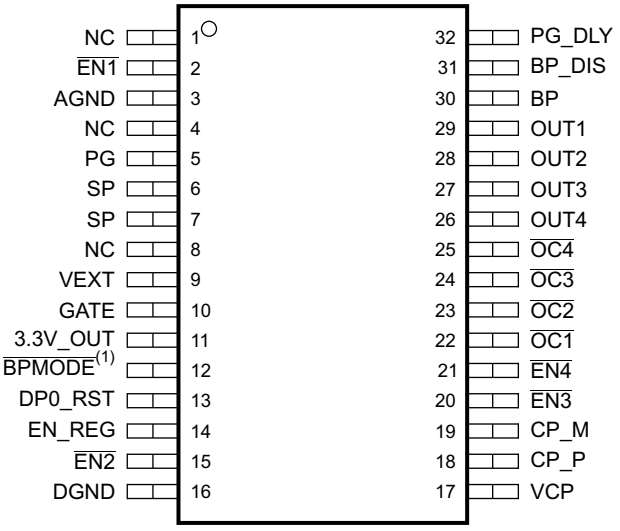
The TPS2070 and TPS2071 provide a complete USB hub power solution by incorporating four major functions: current-limited power switches for four ports, a 3.3-V 100-mA regulator, a 5-V regulator controller for self-power, and a DP0 line control to signal attach/detach of the hub.

These devices are designed to meet bus-powered and self-powered hub requirements. These devices are also designed for hybrid hub implementations and allow for automatic switching from self-powered mode to bus-powered mode if loss of self-power is experienced (can be disabled by applying a logic high to BP_DIS).

Each port has a current-limited 107-mΩ N-channel MOSFET high-side power switch for 500-mA self-powered operation. Each port also has a current-limited 560-mΩ N-channel MOSFET high-side power switch for 100-mA bus-powered operation. All the N-channel MOSFETs are designed without parasitic diodes, preventing current backflow into the inputs.

For applications not requiring a 5-V regulator controller, use the TPS2074 or TPS2075 device.

**DAP Package**
**(Top View)**




NC - No internal connection

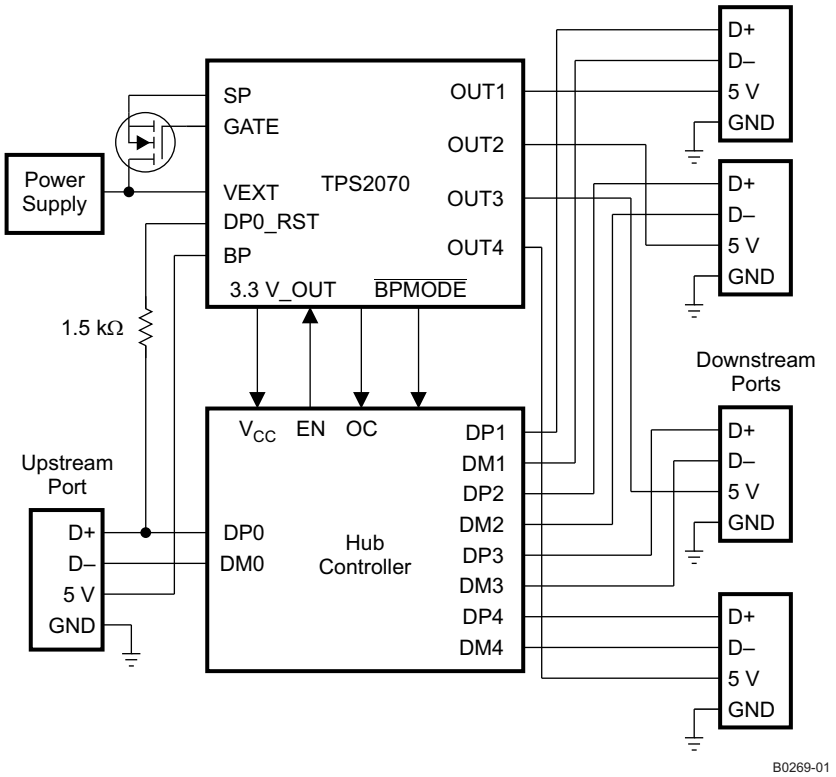
P0073-01

(1) Pin 12 is active-low (BPMODE) for TSS2070 and active-high (BPMODE) for TPS2071.(1)

**GENERAL SWITCH CATALOG**

| 33 mΩ, Single | 80 mΩ, Single | 80 mΩ, Dual | 80 mΩ, Dual | 80 mΩ, Triple | 80 mΩ, Quad | 80 mΩ, Quad |
|---|---|---|---|---|---|---|
| TPS201xA 0.2 A to 2 A | TPS2014 600 mA | TPS2042B 500 mA | TPS2080 500 mA | TPS2043B 500 mA | TPS2044B 500 mA | TPS2085 500 mA |
| TPS202x 0.2 A to 2 A | TPS2015 1 A | TPS2052B 500 mA | TPS2081 500 mA | TPS2053B 500 mA | TPS2054B 500 mA | TPS2086 500 mA |
| TPS203x 0.2 A to 2 A | TPS2041B 500 mA | TPS2046B 250 mA | TPS2082 500 mA | TPS2047B 250 mA | TPS2048A 250 mA | TPS2087 500 mA |
| | TPS2051B 500 mA | TPS2056 250 mA | TPS2090 250 mA | TPS2057A 250 mA | TPS2058 250 mA | TPS2095 250 mA |
| | TPS2045A 250 mA | TPS2062 1 A | TPS2091 250 mA | TPS2063 1 A | | TPS2096 250 mA |
| | TPS2049 100 mA | TPS2066 1 A | TPS2092 250 mA | TPS2067 1 A | | TPS2097 250 mA |
| | TPS2055A 250 mA | TPS2060 1.5 A | | | | |
| | TPS2061 1 A | TPS2064 1.5 A | | | | |
| | TPS2065 1 A | | | | | |
| | TPS2068 1.5 A | | | | | |
| | TPS2069 1.5 A | | | | | |

### Simplified Hybrid-Hub Diagram(1)



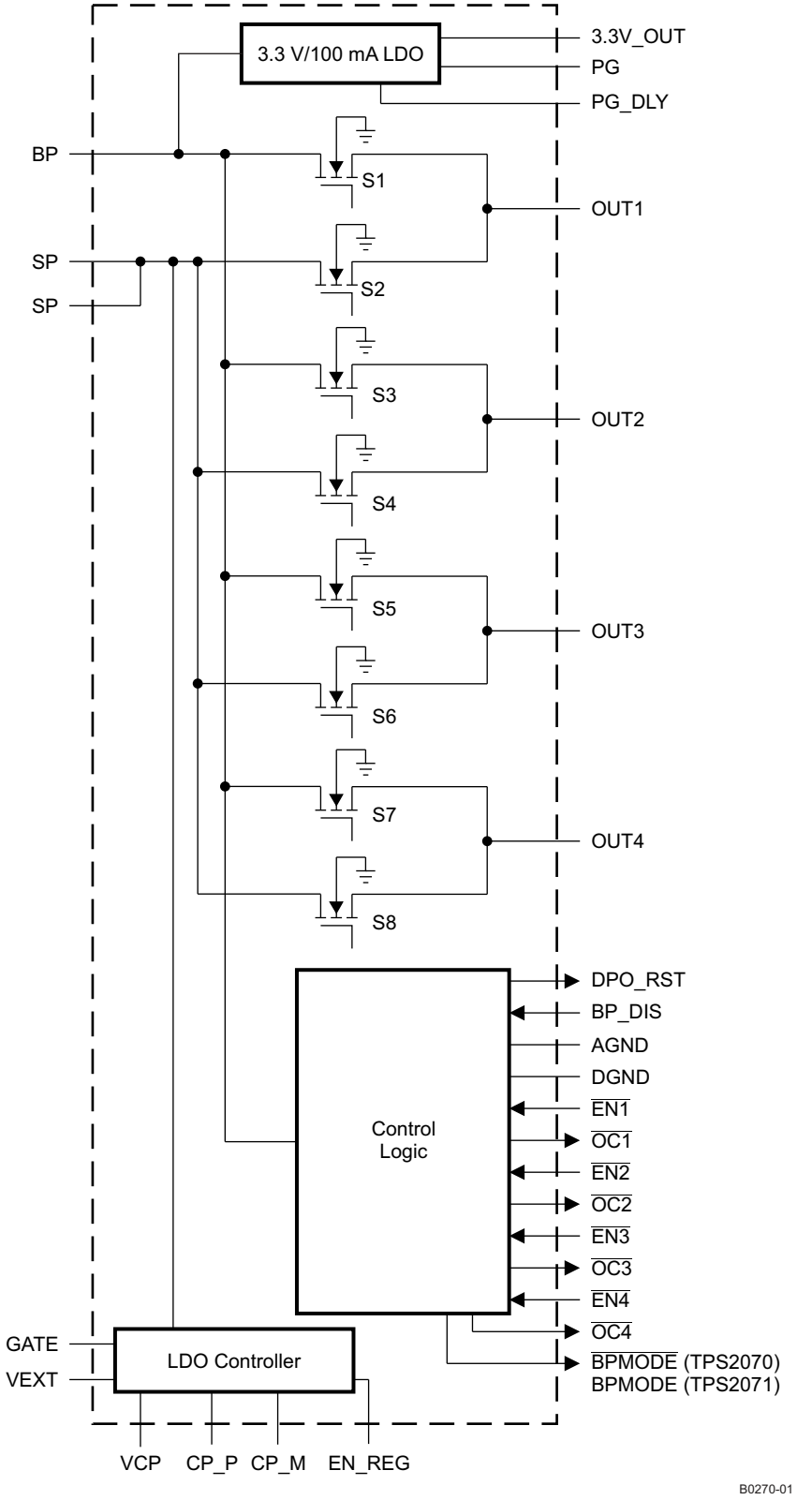

(1) See Figure 38 for complete implementation.

## SELECTION GUIDE

| $T_A$ | USB HUB POWER CONTROLLERS | PACKAGED DEVICES | | | |
|---|---|---|---|---|---|
| | | PIN COUNT | BP MODE | HTSSOP (DAP)(1) | SSOP (DB) |
| –40°C to 85°C | Four-port with internal LDO controller | 32 | Active low | TPS2070DAP | — |
| | | | Active high | TPS2071DAP | — |
| | Four-port without internal LDO controller | 24 | Active low | — | TPS2074DB |
| | | | Active high | — | TPS2075DB |

(1) The DAP package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2070DAPR).

## FUNCTIONAL BLOCK DIAGRAM



## TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 3.3V_OUT | 11 | O | 3.3-V internal voltage regulator output |
| AGND | 3 | | Analog ground |
| BP | 30 | I | Bus power voltage input, connect to $V_{BUS}$ |
| BP_DIS | 31 | I | Active-high logic input, disables autoswitch to bus power when self-power is disconnected. Connect to BP or GND |
| $\overline{\text{BPMODE}}$ (1) | 12 | O | A logic signal that indicates if the outputs source from the bus-powered supply. $\overline{\text{BPMODE}}$ (TPS2070) or BPMODE (TPS2071) can be used to signal hub controller. |
| CP_M | 19 | | Charge-pump-capacitor connection from CP_P. Recommend 0.01-µF between CP_P and CP_M. |
| CP_P | 18 | | Charge-pump-capacitor connection from CP_M. Recommend 0.01-µF between CP_P and CP_M. |
| DGND | 16 | | Digital ground |
| DP0_RST | 13 | O | Connects to DP signal from upstream hub/host through an external 1.5-kΩ resistor |
| $\overline{\text{EN1}}$ | 2 | I | Active-low enable for OUT1 |
| $\overline{\text{EN2}}$ | 15 | I | Active-low enable for OUT2 |
| $\overline{\text{EN3}}$ | 20 | I | Active-low enable for OUT3 |
| $\overline{\text{EN4}}$ | 21 | I | Active-low enable for OUT4 |
| EN_REG | 14 | I | Active-high enable, enables external voltage regulator. Connect to BP or GND |
| GATE | 10 | O | Output gate drive for an external N-channel MOSFET |
| NC | 1, 4, 8 | | No internal connection |
| $\overline{\text{OC1}}$ | 22 | O | Logic output, overcurrent response for OUT1 |
| $\overline{\text{OC2}}$ | 23 | O | Logic output, overcurrent response for OUT2 |
| $\overline{\text{OC3}}$ | 24 | O | Logic output, overcurrent response for OUT3 |
| $\overline{\text{OC4}}$ | 25 | O | Logic output, overcurrent response for OUT4 |
| OUT1 | 29 | O | Power switch output for downstream ports |
| OUT2 | 28 | O | Power switch output for downstream ports |
| OUT3 | 27 | O | Power switch output for downstream ports |
| OUT4 | 26 | O | Power switch output for downstream ports |
| PG | 5 | O | Logic output, power good |
| PG_DLY (2) | 32 | | Adjusts the PG time delay with a capacitor to ground. Adjust the pulse duration to fit the application. |
| SP | 6, 7 | I | Self-power voltage input, connects to local power supply |
| VCP | 17 | | Charge-pump output, source for an external voltage-regulator driver. Recommend 0.1-µF capacitor to DGND. |
| VEXT | 9 | I | Input voltage for the external voltage regulator |

(1) Pin 12 is active-low for TPS2070 and active-high for TPS2071.
(2) Use the following formula to calculate the capacitance needed: C = (desired pulse duration $\times$ 3 $\times$ $10^{-6}$)/1.22

## DETAILED DESCRIPTION

### BP

The bus-powered supply input (BP) serves as the source for the internal 3.3-V LDO and for all logic functions in the device. In bus-powered mode, BP also serves as the source for all the outputs (OUTx). If BP is below the undervoltage threshold, all power switches turn off and the LDO is disabled. BP must be connected to a voltage source for the device to operate.

### SP

The self-powered supply input (SP) serves as the source for all the outputs (OUTx) in self-powered mode. The enable logic for the SP switches requires that BP be connected to a voltage source.

### OUT1, OUT2, OUT2, OUT4

OUTx are the outputs of the integrated power switches.

### 3.3V_OUT

The internal 3.3-V LDO output can be used to supply up to 100 mA of current to low-power functions, such as hub controllers.

### VEXT

VEXT is used to generate a 5-V source for the SP input by using the internal LDO controller and an external N-channel MOSFET. This pin connects to a 6-V to 9-V power supply and to the drain of the MOSFET if the external LDO is needed.

### GATE

GATE is the output of the 5-V LDO controller and connects to the gate of the external MOSFET.

### EN_REG

The active-high input, EN_REG, is used to enable the 5-V regulator controller. EN_REG is compatible with TTL and CMOS logic levels.

### DP0_RST

DP0_RST functions as a hub reset when a 1.5-kΩ resistor is connected between DP0_RST and the upstream DP0 data line in a hub system. To provide a clean attach signal on the DP0 data line, the DP0_RST output goes low momentarily (because of the upstream pulldown resistor) to discharge any parasitic charge on the cable, then goes to the high-impedance state and finally outputs a high signal. The low and Hi-Z pulse durations are adjustable using a capacitor between PG_DLY and ground, and are approximately 50% of the power-good time delay. Detachment is signaled by a Hi-Z on DP0_RST. Both DP0_RST and PG transition high at the same time.

### Power Good (PG)

The power-good (PG) function serves as a reset for a USB hub controller. PG is asserted low when the output voltage on the internal voltage regulator is below a fixed threshold. A time delay to ensure a stable output voltage before PG goes high is adjustable using a small-value ceramic capacitor from PG_DLY to ground.

### PG_DLY

PG_DLY connects to an external capacitor to adjust the time delay for PG and DP0_RST. For USB applications, a 0.1-µF capacitor is recommended; however, see the USB hub controller data sheet to determine the required pulse-duration criteria.

### BP_DIS

BP_DIS is used to enable or disable the autoswitching function between bus-powered mode and self-powered mode. When BP_DIS is connected low and the voltage on SP is greater than the undervoltage-lockout (UVLO) threshold, the device switches to self-powered operation automatically; if the SP voltage falls lower than the UVLO threshold, the device switches to bus-powered operation. When BP_DIS is connected high, the autoswitching function is disabled and the device does not autoswitch to bus-powered operation if the SP voltage is below the UVLO threshold.

### $\overline{\text{BPMODE}}$ or BPMODE

$\overline{\text{BPMODE}}$ (TPS2070) or $\overline{\text{BPMODE}}$ (TPS2071) is an output that signals when the device is in bus-powered mode. The logic state is set according to the voltages on BP, SP, and BP_DIS. For the TPS2070, BPMODE outputs a low signal to indicate bus-powered mode or a high signal to indicate self-powered mode. For the TPS2071, BPMODE outputs a high signal to indicate bus-powered mode or a low signal to indicate self-powered mode. This output can be used to inform a USB hub controller to configure for bus-powered mode or self-powered mode.

### $\overline{OC1}$, $\overline{OC2}$, $\overline{OC3}$, $\overline{OC4}$

$\overline{OCx}$ is an output signal that is asserted (active low) when an overcurrent or overtemperature condition is encountered for the corresponding channel. $\overline{OCx}$ remains asserted until the overcurrent or overtemperature condition is removed.

### $\overline{EN1}$, $\overline{EN2}$, $\overline{EN3}$, $\overline{EN4}$

The active-low logic input $\overline{ENx}$ enables or disables the power switches in the device. The enable input is compatible with both TTL and CMOS logic levels. The switches do not turn on until 3.3V_OUT is above the PG threshold.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | VALUE | UNIT |
|---|---|---|---|
| Input voltage range | $V_{I(BP)}$, $V_{I(SP)}$, $V_{I(\overline{ENx})}$, $V_{I(EN\_REG)}$, $V_{I(BP\_DIS)}$ | –0.3 to 6 | V |
| | $V_{I(VEXT)}$ | –0.3 to 10 | V |
| Output voltage range | $V_{O(OUTx)}$, $V_{O(3.3V\_OUT)}$, $V_{O(PG\_DLY)}$, $V_{O(\overline{OCx})}$, $V_{O(\overline{BPMODE})}$, $V_{O(DP0\_RST)}$, $V_{O(PG)}$ | –0.3 to 6 | V |
| | $V_{O(GATE)}$, $V_{O(CP\_M)}$, $V_{O(CP\_P)}$, $V_{O(VCP)}$ | –0.3 to 15 | V |
| Continuous output current | $I_{O(OUTx)}$ | Internally limited | |
| | $I_{O(3.3V\_OUT)}$ | Internally limited | |
| Maximum output current | $I_{O(VCP)}$ | ±30 | mA |
| | $I_{O(\overline{BPMODE})}$ or $I_{O(BPMODE)}$, $I_{O(DP0\_RST)}$, $I_{O(PG)}$, $I_{O(OCx)}$ | ±10 | mA |
| | $I_{O(GATE)}$, sourcing | 700 | µA |
| | $I_{O(GATE)}$, sinking | –2.2 | mA |
| Continuous total power dissipation | | See Dissipation Rating Table | |
| Operating virtual junction temperature range, $T_J$ | | –40 to 125 | °C |
| Storage temperature range, $T_{stg}$ | | –65 to 150 | °C |
| Lead temperature (soldering), 1,6 mm (1/16 inch) from case for 10 seconds | | 260 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

## DISSIPATION RATINGS

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| 32-DAP | 1162.8 mW | 11.6 mW/°C | 639.5 mW | 465.1 mW |
| 32-DAP(1) | 4255.3 mW | 42.5 mW/°C | 2340.4 mW | 1702.1 mW |

(1) Using thermal pad as heatsink.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{I(BP)}$ | Input voltage | | 4.5 | 5.5 | V |
| $V_{I(SP)}$ | | | 0 | 5.5 | |
| $V_{I(VEXT)}$ | | | 0 | 9 | |
| $V_{I(BP\_DIS)}$ | | | 0 | 5.5 | |
| $V_{I(\overline{ENx})}$ | | | 0 | 5.5 | |
| $V_{I(EN\_REG)}$ | | | 0 | 5.5 | |
| $I_O$ | Continuous output current | BP to OUTx (per switch) | | 100 | mA |
| | | SP to OUTx (per switch) | | 500 | |
| | | BP to 3.3V_OUT | | 100 | |
| $T_J$ | Operating virtual junction temperature | | –40 | 125 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, 4.5 V ≤ $V_{I(BP)}$ ≤ 5.5 V, 4.85 V ≤ $V_{I(SP)}$ ≤ 5.5 V, 6 V ≤ $V_{I(VEXT)}$ ≤ 9 V, $\overline{ENx}$ = 0 V, EN_REG = 0 V, BP_DIS = 0 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS[1] | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **INPUT CURRENT** | | | | | | | | |
| $I_{I(BP)}$ | Input current at BP, switches disabled | | No load on OUTx and 3.3V_OUT, $\overline{ENx}$ = $V_{I(BP)}$ | $V_{I(SP)}$ = Hi-Z | | 185 | 240 | µA |
| | | | | $V_{I(SP)}$ = 0 V | | 185 | 240 | |
| | | | | $V_{I(SP)}$ = 5 V | | 175 | 210 | |
| | Input current at BP, switches enabled | | No load on OUTx and 3.3V_OUT, $\overline{ENx}$ = 0 V | $V_{I(SP)}$ = Hi-Z | | 185 | 240 | µA |
| | | | | $V_{I(SP)}$ = 0 V | | 185 | 240 | |
| | | | | $V_{I(SP)}$ = 5 V | | 175 | 210 | |
| $I_{I(SP)}$ | Input current at SP, switches disabled | | No load on OUTx and 3.3V_OUT, $\overline{ENx}$ = $V_{I(SP)}$ | $V_{I(SP)}$ = Hi-Z | | 90 | 115 | µA |
| | | | | $V_{I(SP)}$ = 0 V | | 90 | 115 | |
| | | | | $V_{I(SP)}$ = 5 V | | 115 | 140 | |
| | Input current at SP, switches enabled | | No load on OUTx and 3.3V_OUT, $\overline{ENx}$ = 0 V | $V_{I(SP)}$ = Hi-Z | | 90 | 115 | µA |
| | | | | $V_{I(SP)}$ = 0 V | | 90 | 115 | |
| | | | | $V_{I(SP)}$ = 5 V | | 115 | 140 | |
| $I_{I(VEXT)}$ | Input current at VEXT, LDO controller disabled | | $V_{I(EN\_REG)}$ = 0 V or Hi-Z, $V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = Hi-Z | | | 200 | 360 | µA |
| | Input current, at VEXT, LDO controller enabled | | $V_{I(EN\_REG)}$ = 5 V, $V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = Hi-Z | | | | 10 | mA |
| **POWER SWITCHES** | | | | | | | | |
| $r_{DS(on)}$ | Static drain-source on-state resistance | SP to OUTx | $V_{I(SP)}$ = $V_{I(BP)}$ = 5 V, $I_{Ox}$ = 0.5 A | $T_A$ = 25°C | | 107 | | mΩ |
| | | | | $T_A$ = 70°C | | 125 | 160 | |
| | | BP to OUTx | $V_{I(BP)}$ = 4.5 V, $V_{I(SP)}$ = open, $I_{Ox}$ = 0.1 A | $T_A$ = 25°C | | 560 | | |
| | | | | $T_A$ = 70°C | | 630 | 900 | |
| $I_{lkg(OUTx)}$ | Leakage current at OUTx | | $\overline{ENx}$ = $V_{I(BP)}$ = 5.5 V, $V_{I(SP)}$ = Hi-Z, OUTx connected to ground, $V_{I(VIN)}$ = Hi-Z, no load on 3.3V_OUT | $T_J$ = 25°C | | 0.5 | 10 | µA |
| | | | $\overline{ENx}$ = $V_{I(BP)}$ = $V_{I(SP)}$ = 5.5 V, OUTx connected to ground, $V_{I(EXT)}$ = Hi-Z, no load on 3.3V_OUT | $T_J$ = 25°C | | 0.5 | 10 | |
| | | | $\overline{ENx}$ = $V_{I(BP)}$ = Hi-Z or 0 V, $V_{I(VEXT)}$ = $V_{I(SP)}$ = $V_{I(OUTx)}$ = 5.5 V, no load on 3.3V_OUT | $T_J$ = 25°C | | 0.5 | 10 | |
| | | | $\overline{ENx}$ = $V_{I(BP)}$ = $V_{I(SP)}$ = Hi-Z or 0 V, $V_{I(VEXT)}$ = $V_{I(OUTx)}$ = 5.5 V, no load on 3.3V_OUT | $T_J$ = 25°C | | 0.5 | 10 | |
| | | | $\overline{ENx}$ = $V_{I(BP)}$ = $V_{I(SP)}$ = $V_{I(VEXT)}$ = Hi-Z or 0 V, $V_{I(OUTx)}$ = 5.5 V, no load on 3.3V_OUT | $T_J$ = 25°C | | 0.5 | 10 | |
| $I_{OS}$ | Short-circui outputt current[1] | | $V_{I(BP)}$ = $V_{I(SP)}$ = 5 V, OUTx connected to GND, device enabled into short circuit | | 0.6 | 0.9 | 1.2 | A |
| | | | $V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = open, OUTx connected to GND, device enabled into short circuit | | 0.12 | 0.2 | 0.3 | |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, 4.5 V ≤ $V_{I(BP)}$ ≤ 5.5 V, 4.85 V ≤ $V_{I(SP)}$ ≤ 5.5 V, 6 V ≤ $V_{I(VEXT)}$ ≤ 9 V, $\overline{ENx}$ = 0 V, EN_REG = 0 V, BP_DIS = 0 V (unless otherwise noted)

| PARAMETER | | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **INPUT SIGNALS ($\overline{ENx}$, EN_REG, BP_DIS)** | | | | | | | | |
| $V_{IH}$ | High-level input voltage | | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.8 | V |
| $I_I$ | Input current | Pullup | $\overline{ENx}$ (active-low) | $V_{I(\overline{ENx})}$ = 0 V | | | 5 | µA |
| | | Pulldown | EN_REG (active-high) | $V_{I(EN\_REG)}$ = 5 V | | | 5 | µA |
| | | | BP_DIS (active-high) | $V_{I(BP\_DIS)}$ = 5 V | | | 5 | µA |

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, 4.5 V ≤ $V_{I(BP)}$ ≤ 5.5 V, 4.85 V ≤ $V_{I(SP)}$ ≤ 5.5 V, 6 V ≤ $V_{I(VEXT)}$ ≤ 9 V, $\overline{ENx}$ = 0 V, EN_REG = 0 V, BP_DIS = 0 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **OUTPUT SIGNALS (BPMODE or $\overline{BPMODE}$, $\overline{OCx}$, DPO_RST)** | | | | | | | | |
| $V_{OH}$ | High-level output voltage | $\overline{BPMODE}$ | 4.25 V ≤ $V_{I(BP)}$ ≤ 5.5 V, 4.5 V ≤ $V_{I(SP)}$ ≤ 5.5 V | $I_O$ = 2 mA | 2.4 | | | V |
| | | BPMODE | 4.25 V ≤ $V_{I(BP)}$ ≤ 5.5 V, $V_{I(SP)}$ < 4 V | | 2.4 | | | V |
| | | $\overline{OCx}$ | 4.25 V ≤ $V_{I(BP)}$ ≤ 5.5 V, $V_{I(\overline{ENx})}$ = 3.3 V or Hi-Z | | 2.4 | | | V |
| | | DPO_RST | 4.25 V ≤ $V_{I(BP)}$ ≤ 5.5 V, $V_{I(PG\_DLY)}$ = 3.3 V | | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $\overline{BPMODE}$ | 4.25 V ≤ $V_{I(BP)}$ ≤ 5.5 V, $V_{I(SP)}$ < 4 V | $I_O$ = 3.2 mA | | | 0.4 | V |
| | | BPMODE | 4.25 V ≤ $V_{I(BP)}$ ≤ 5.5 V, 4.5 V ≤ $V_{I(SP)}$ ≤ 5.5 V | | | | 0.4 | V |
| | | $\overline{OCx}$ | 4.25 V ≤ $V_{I(BP)}$ ≤ 5.5 V, OUTx = 0 V | $I_{O(\overline{OC})}$ = 3.2 mA | | | 0.4 | V |
| $V_{I(BP)}$ | Minimum input voltage at BP for low-level output | | $I_O$ = 300 µA, $V_{O(\overline{BPMODE})}$ ≤ 0.4 V | | | | 1.5 | µA |
| | | | $I_O$ = 300 µA, $V_{O(BPMODE)}$ ≤ 0.4 V, $V_{I(SP)}$ = 5 V | | | | 1.5 | µA |
| $I_{lkg}$ | Hi-Z leakage current at DP0_RST | | 0 V ≤ $V_{I(DP0\_RST)}$ ≤ 3.3 V, $V_{I(SP)}$ = 0 V, $V_{I(BP)}$ = 5.5 V, $V_{I(PG\_DLY)}$ = 0.9 V | | –5 | | 5 | |
| $t_d$ | Overcurrent response delay time (1) | | | | 1 | | 10 | ms |
| **UNDERVOLTAGE LOCKOUT (SP, BP, VEXT)** | | | | | | | | |
| | Start threshold | | SP | | | | 4.5 | V |
| | | | BP | $V_{I(SP)}$ = Hi-Z | | | 4.25 | V |
| | | | VEXT | | | | 3 | V |
| | Stop threshold | | SP | | 4 | | | V |
| | | | BP | | 3.75 | | | V |
| | | | VEXT | | 2.5 | | | V |
| $V_{hys}$ | Hysteresis voltage (1) | | SP | | 300 | | | mV |
| | | | BP | | 300 | | | mV |
| | | | VEXT | | 150 | | | mV |

(1) Specified by design, not tested in production.

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, 4.5 V ≤ $V_{I(BP)}$ ≤ 5.5 V, 4.85 V ≤ $V_{I(SP)}$ ≤ 5.5 V, 6 V ≤ $V_{I(VEXT)}$ ≤ 9 V, $\overline{ENx}$ = 0 V, EN_REG = 0 V, BP_DIS = 0 V, $C_{L(3.3V\_OUT)}$ = 10 µF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INTERNAL VOLTAGE REGULATOR** | | | | | | |
| $V_O$ | Output voltage, dc | $V_{I(BP)}$ = 4.25 V to 5.5 V, $I_O$ = 5 mA to 100 mA | 3.2 | 3.3 | 3.4 | V |
| | Dropout voltage | $I_O$ = 100 mA | | 0.6 | | V |
| | Line regulation | $V_{I(BP)}$ = 4.25 V to 5.25 V, $I_O$ = 5 mA | | | 0.1 | %/V |
| | Load regulation | $V_{I(BP)}$ = 4.25 V, $I_O$ = 5 mA to 100 mA | | | 0.6% | |
| $I_{OS}$ | Short-circuit current limit (1) | $V_{I(BP)}$ = 4.25 V, 3.3V_OUT connected to GND | 0.12 | 0.2 | 0.3 | A |
| | Pulldown current through transistor at 3.3V_OUTPUT (2) | $V_{I(3.3V\_OUT)}$ = 3.3 V | 10 | | | mA |
| | | $V_{I(3.3V\_OUT)}$ = 1 V | 5 | | | |
| PSRR | Power-supply ripple rejection (2) | f = 1 kHz, $C_{L(3.3V\_OUT)}$ = 4.7 µF, ESR = 0.25 Ω, $I_O$ = 5 mA, $V_{I(BP)PP}$ = 100 mV | 40 | | | dB |
| | Low-level trip threshold voltage at PG | | 2.88 | 2.94 | 3 | V |
| $V_{hys}$ | Hysteresis voltage at PG (2) | | 50 | | 100 | mV |
| $V_{OH}$ | High-level output voltage at PG | 4.25 V ≤ $V_{I(BP)}$ ≤ 5.25 V, $I_O$ = 2 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage at PG | 4.25 V ≤ $V_{I(BP)}$ ≤ 5.25 V, $I_O$ = 3.2 mA | | | 0.4 | V |
| $V_{ref}$ | Reference voltage at PG_DLY | | | 1.22 | | V |
| | Charge current at PG_DLY | | | 3 | | µA |
| $t_d$ | Delay time at PG (2) (3) | $C_{L(PG\_DLY)}$ = 0.47 µF | | 190 | | ms |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Specified by design, not tested in production.
(3) The PG delay time ($t_d$) is calculated using the PG_DLY reference voltage and charge current:

$$t_d = \frac{C_{L(PG\_DLY)} \times V_{ref}}{\text{Charge Current}}$$

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, 4.5 V ≤ $V_{I(BP)}$ ≤ 5.5 V, 4.85 V ≤ $V_{I(SP)}$ ≤ 5.5 V, 6 V ≤ $V_{I(VEXT)}$ ≤ 9 V, $\overline{ENx}$ = 0 V, EN_REG = 3.3 V, BP_DIS = 0 V, $C_{L(SP)}$ = 220 µF (unless otherwise noted))

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **VOLTAGE REGULATOR CONTROLLER** | | | | | | | |
| $V_{O(CP)}$ | Output voltage, charge pump | | $V_{I(VEXT)}$ = 6 V, $I_{O(VCP)}$ = 5 mA, $C_{(CP\_P)}$ = 10 nF, $C_{(VCP)}$ = 100 nF | 10 | | | V |
| $f_{osc}$ | Oscillator frequency (1) | | 6 V ≤ $V_{I(VEXT)}$ ≤ 9 V, $I_{O(VCP)}$ = 5 mA, $V_{O(VCP)}$ = 10 V | | 850 | | kHz |
| | Gate drive current | Sourcing | $V_{I(VCP)}$ = 9 V, $V_{O(GATE)}$ = 7.5 V, $V_{I(SP)}$ = 4.5 V | 500 | | | µA |
| | | Sinking | $V_{I(VCP)}$ = 9 V, $V_{O(GATE)}$ = 5.5 V, $V_{I(SP)}$ = 5.5 V | 1.5 | | | mA |
| | Open-loop gain (1) | | $V_{I(VEXT)}$ = 6 V, 0.5 V ≤ $V_{O(GATE)}$ ≤ 9 V | | 80 | | dB |
| | Reference voltage at $V_{I(SP)}$, using external regulator | | $V_{I(VEXT)}$ = 6 V to 9 V, IRLZ24N FET | 4.9 | 5.1 | 5.25 | V |
| | Gate clamp voltage | | Gate to SP | | 10 | | V |

(1) Specified by design, not tested in production.

## POWER SWITCH TIMING REQUIREMENTS

| PARAMETER | | | TEST CONDITIONS(1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{on}$ | Turnon time(2) | BP to OUTx switch | $V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = open, $T_A$ = 25°C, $C_L$ = 100 µF, $R_L$ = 50 Ω | | 4.5 | | ms |
| | | SP to OUTx switch | $V_{I(SP)}$ = $V_{I(BP)}$ = 5 V, $T_A$ = 25°C, $C_L$ = 100 µF, $R_L$ = 10 Ω | | 4.5 | | |
| $t_{off}$ | Turnoff time(2) | BP to OUTx switch | $V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = open, $T_A$ = 25°C, $C_L$ = 100 µF, $R_L$ = 50 Ω | | 15 | | ms |
| | | SP to OUTx switch | $V_{I(SP)}$ = $V_{I(BP)}$ = 5 V, $T_A$ = 25°C, $C_L$ = 100 µF, $R_L$ = 10 Ω | | 10 | | |
| $t_r$ | Rise time, output(2) | BP to OUTx switch | $V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = open, $T_A$ = 25°C, $C_L$ = 100 µF, $R_L$ = 50 Ω | | 4 | | ms |
| | | SP to OUTx switch | $V_{I(SP)}$ = $V_{I(BP)}$ = 5 V, $T_A$ = 25°C, $C_L$ = 100 µF, $R_L$ = 10 Ω | | 3 | | |
| $t_f$ | Fall time, output(2) | BP to OUTx switch | $V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = open, $T_A$ = 25°C, $C_L$ = 100 µF, $R_L$ = 50 Ω | | 10 | | ms |
| | | SP to OUTx switch | $V_{I(SP)}$ = $V_{I(BP)}$ = 5 V, $T_A$ = 25°C, $C_L$ = 100 µF, $R_L$ = 10 Ω | | 3 | | |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Specified by design, not tested in production.

## THERMAL SHUTDOWN

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_J$ | Thermal shutdown | First | | 140 | | °C |
| | | Second | | 150 | | |
| | Hysteresis | First | | 15 | | °C |
| | | Second | | 25 | | |

## PARAMETER MEASUREMENT INFORMATION

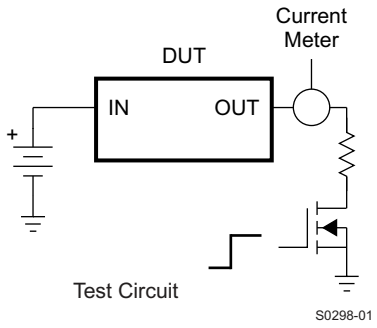



**Figure 1. Current Limit Response**

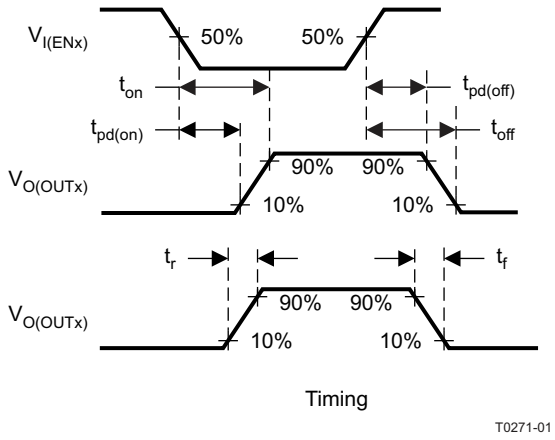



**Figure 2. Timing and Internal Voltage Regulator Transition Waveforms**

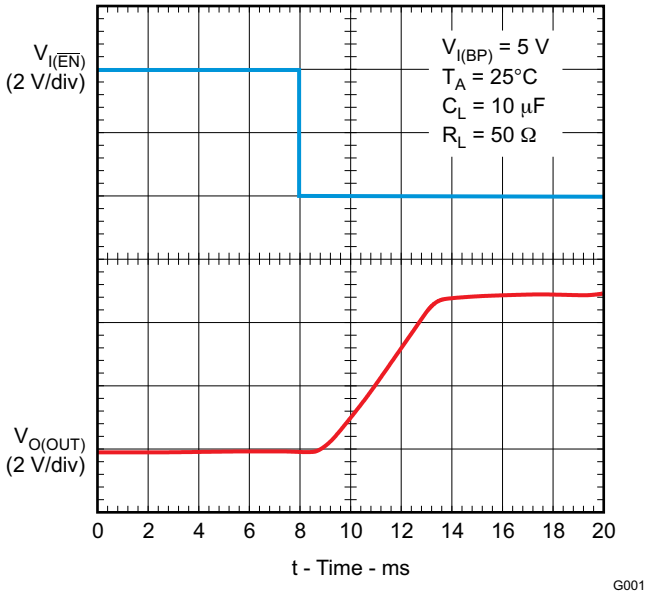



**Figure 3. Turnon Delay and Rise Time (BP Switch)**

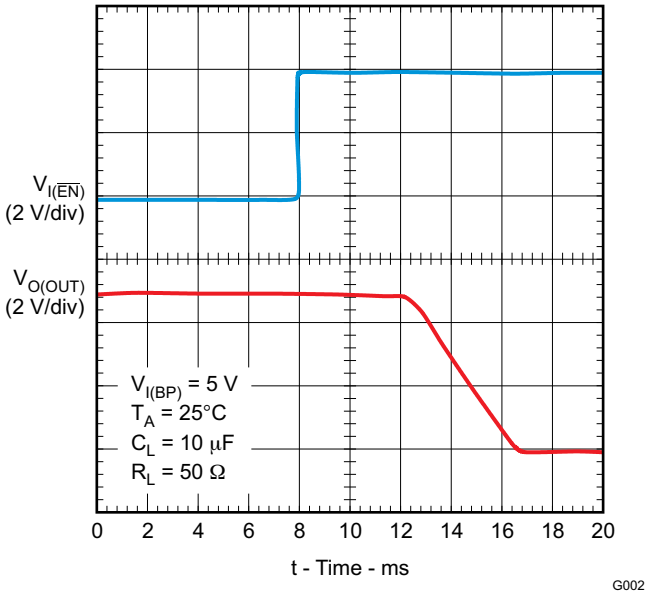



**Figure 4. Turnoff Delay and Fall Time (BP Switch)**

## PARAMETER MEASUREMENT INFORMATION (continued)

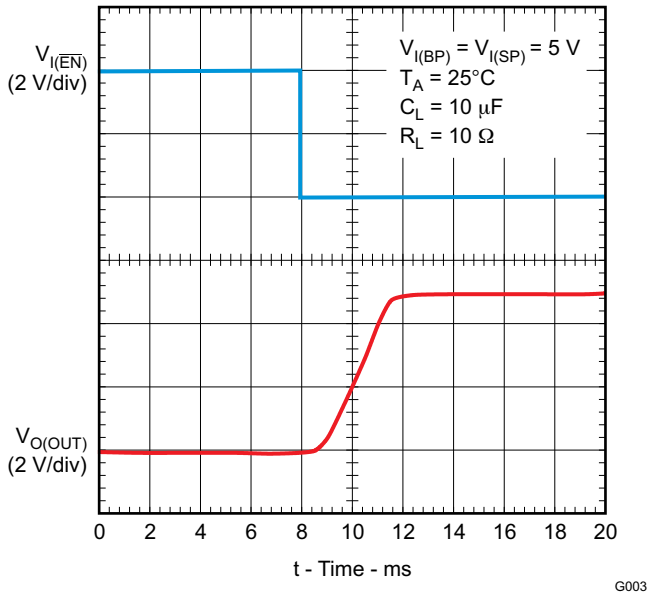



**Figure 5. Turnon Delay and Rise Time (SP Switch)**

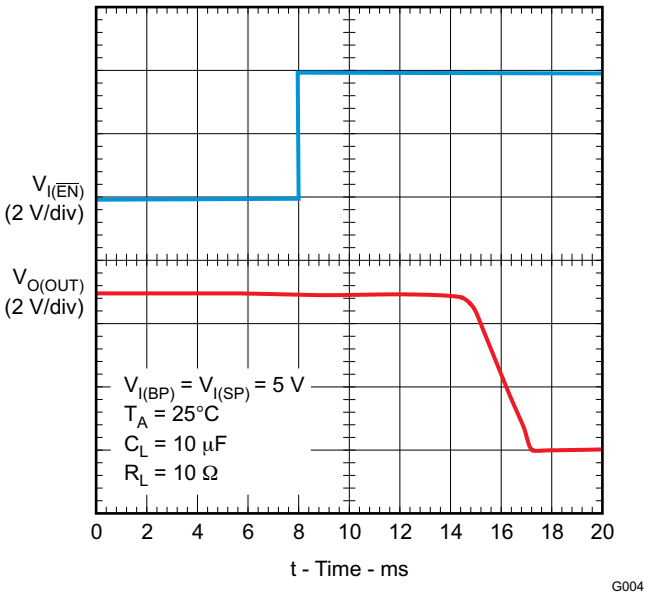



**Figure 6. Turnoff Delay and Fall Time (SP Switch)**

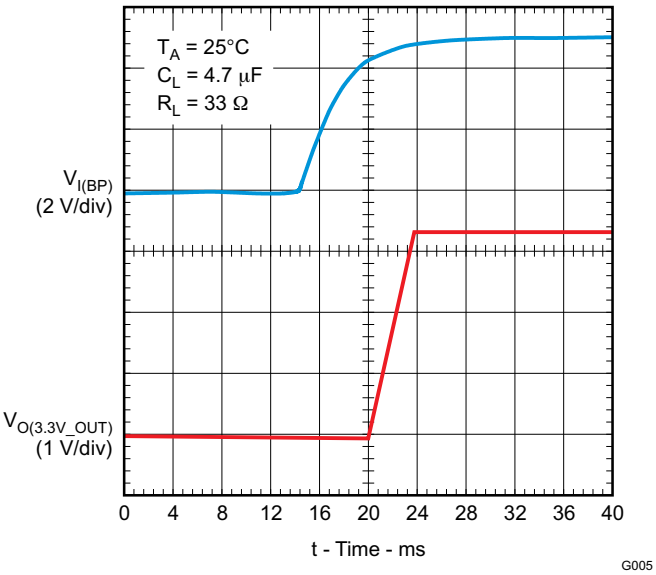



**Figure 7. Turnon Delay and Rise Time (3.3V_OUT)**

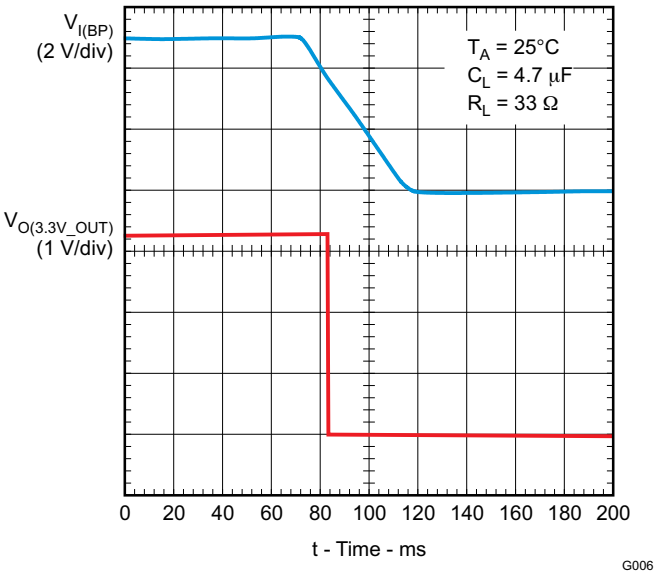



**Figure 8. Turnoff Delay and Fall Time (3.3V_OUT)**

## PARAMETER MEASUREMENT INFORMATION (continued)

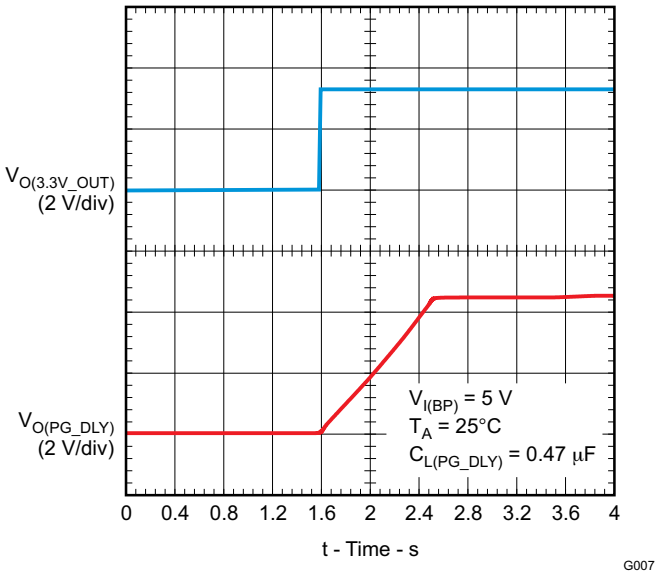



**Figure 9. PG_DLY Rise Time With a 0.47-µF Capacitor**

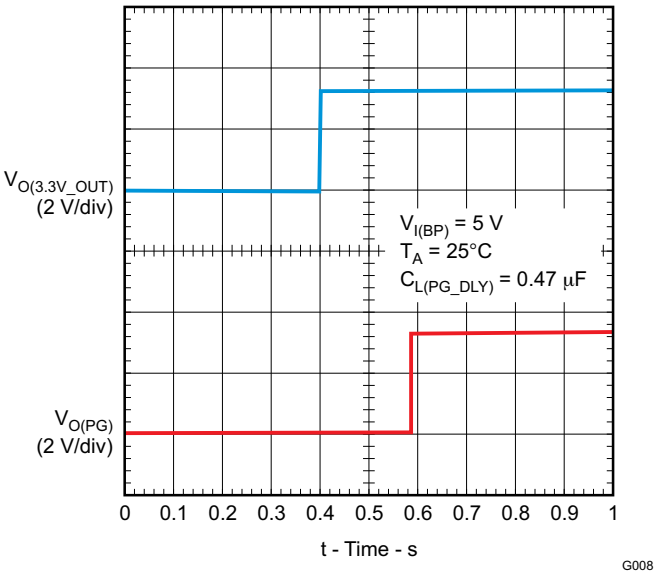



**Figure 10. Turnon Delay (3.3V_OUT to PG)**

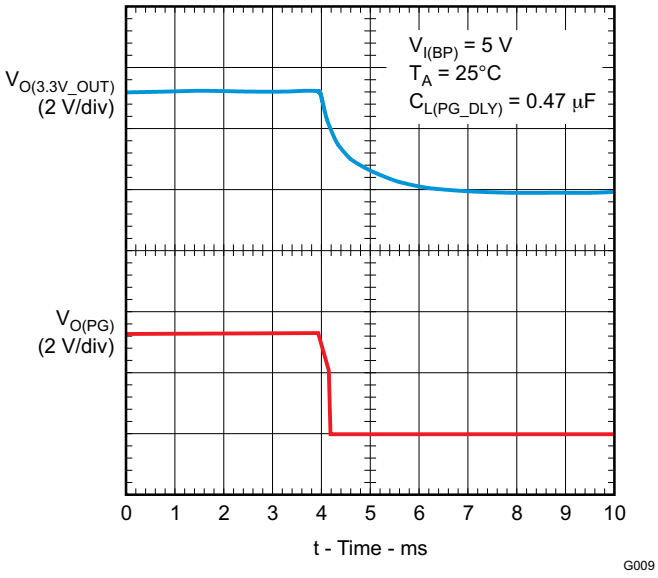



**Figure 11. Turnoff Time (3.3V_OUT to PG)**

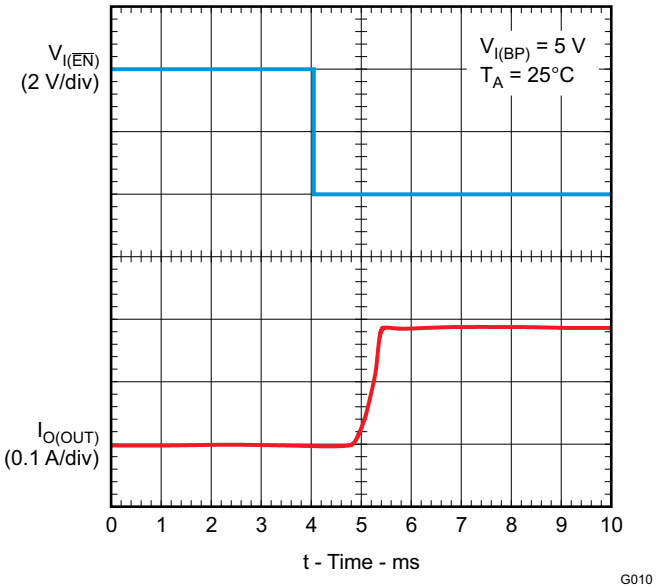



**Figure 12. Short-Circuit Current (BP Switch), Device Enabled Into Short**

## PARAMETER MEASUREMENT INFORMATION (continued)

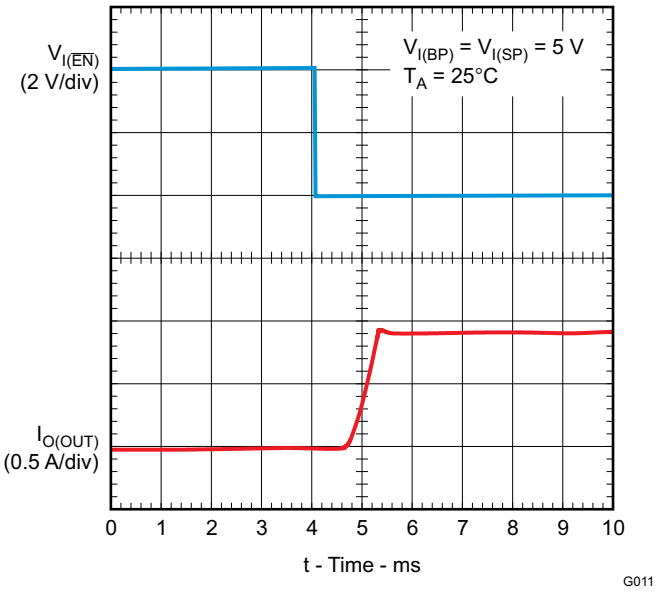



**Figure 13. Short-Circuit Current (SP Switch), Device Enabled Into Short**

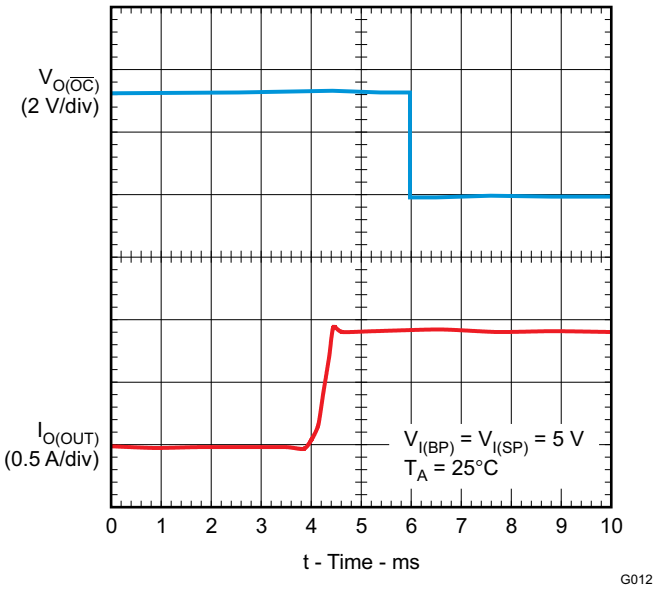



**Figure 14. $\overline{OC}$ Response (SP Switch), Device Enabled Into Short,**

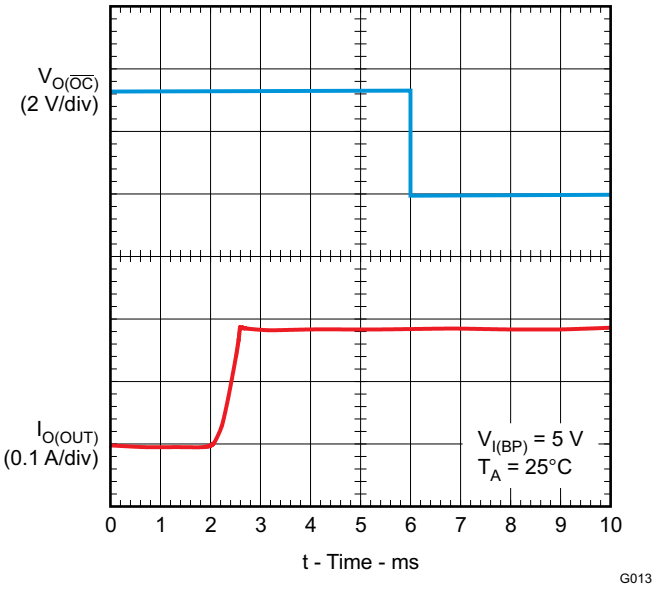



**Figure 15. $\overline{OC}$ Response (BP Switch), Device Enabled Into Short**

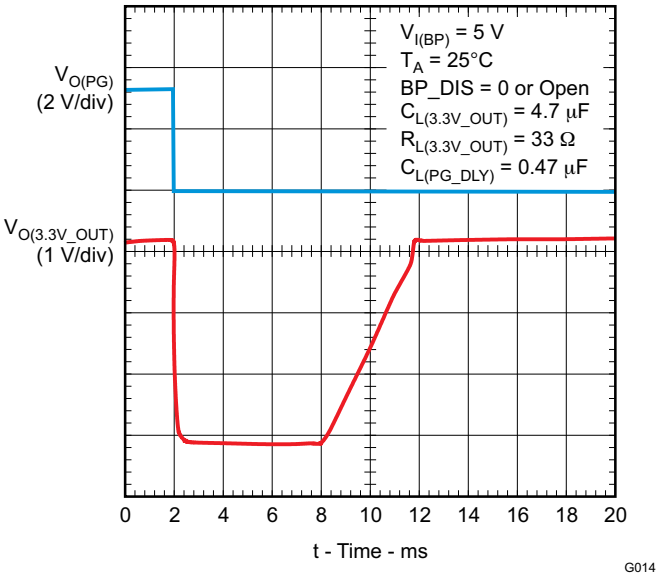



**Figure 16. SP to BP Automatic Switchover Enabled**

## PARAMETER MEASUREMENT INFORMATION (continued)

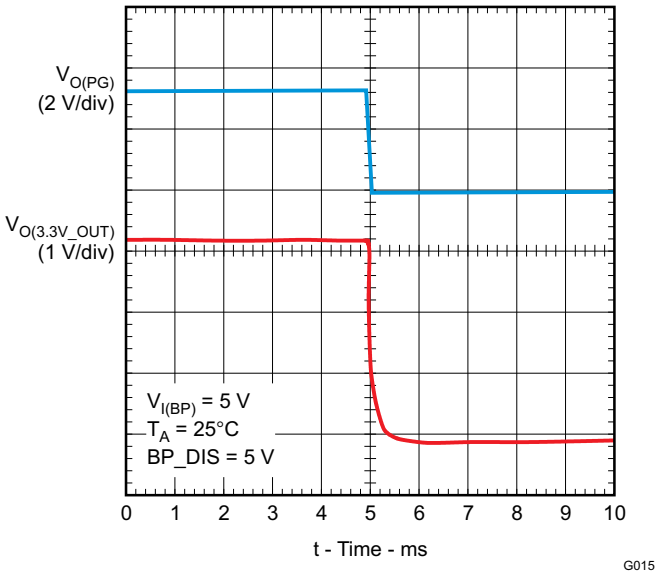



**Figure 17. SP to BP Automatic Switchover Disabled**

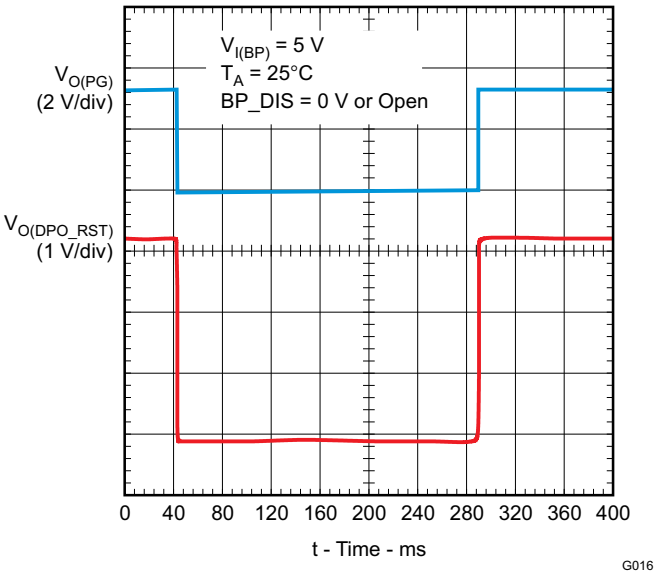



**Figure 18. SP to BP Automatic Switchover Enabled**

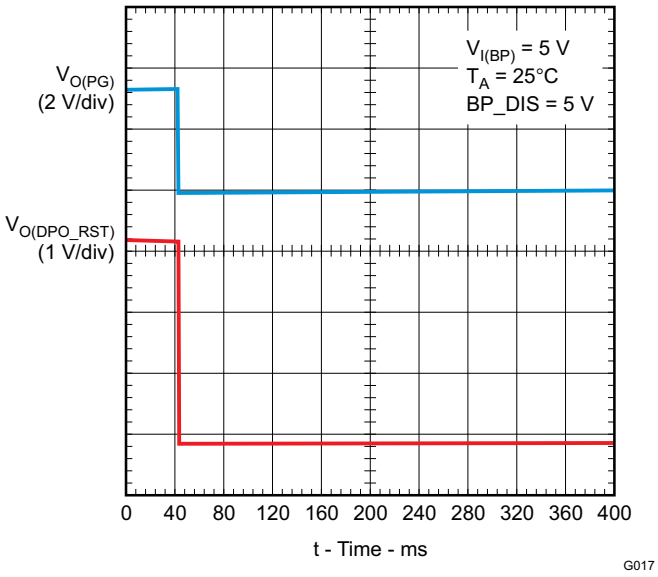



**Figure 19. SP to BP Automatic Switchover Disabled**

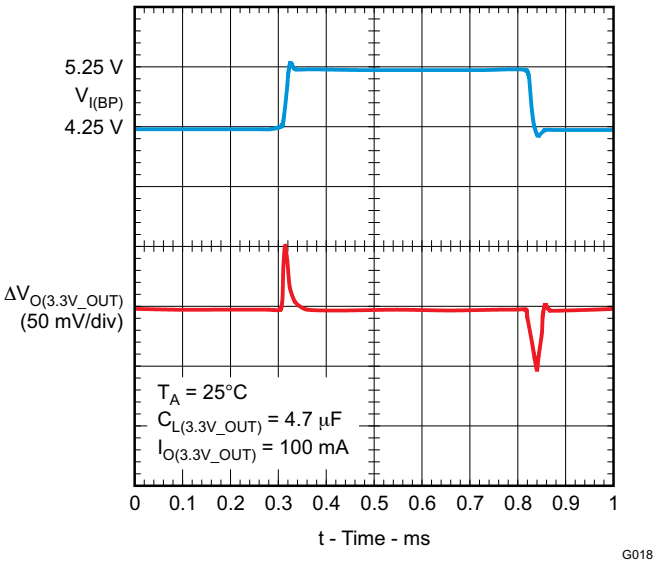



**Figure 20. Line Transient Response**

## PARAMETER MEASUREMENT INFORMATION (continued)

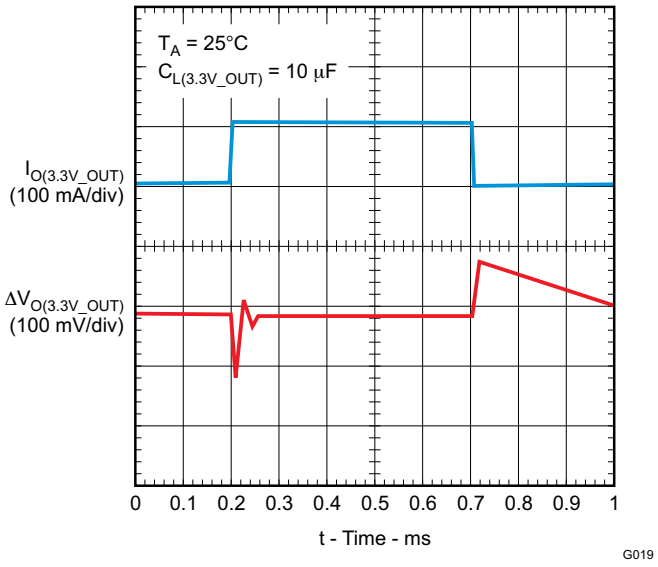



**Figure 21. Load Transient Response**

## TYPICAL CHARACTERISTICS

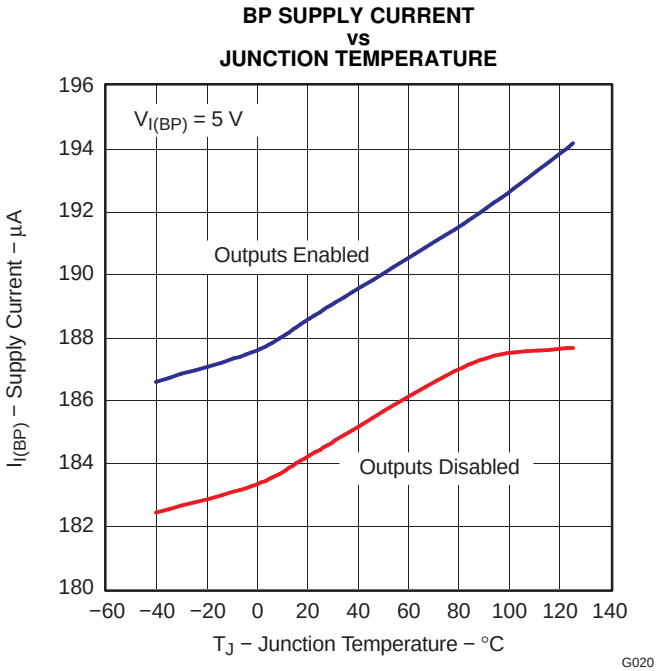



**Figure 22.**

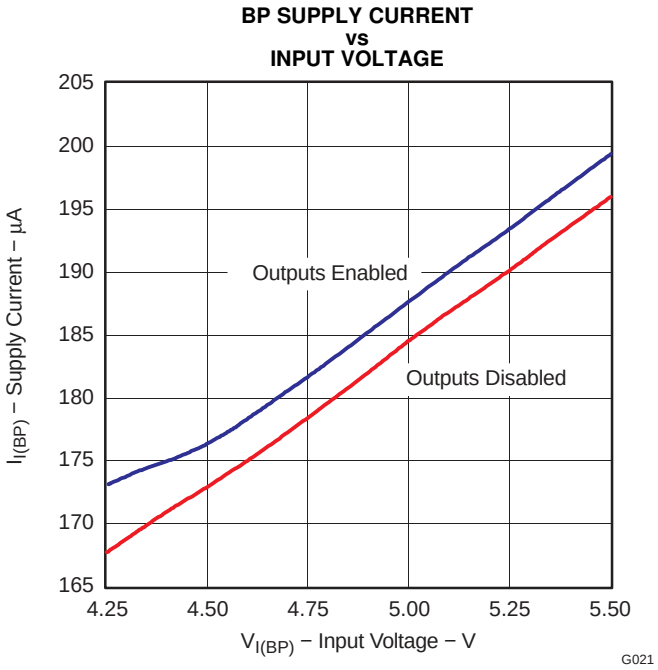



**Figure 23.**

## TYPICAL CHARACTERISTICS (continued)

**SP SUPPLY CURRENT vs JUNCTION TEMPERATURE**

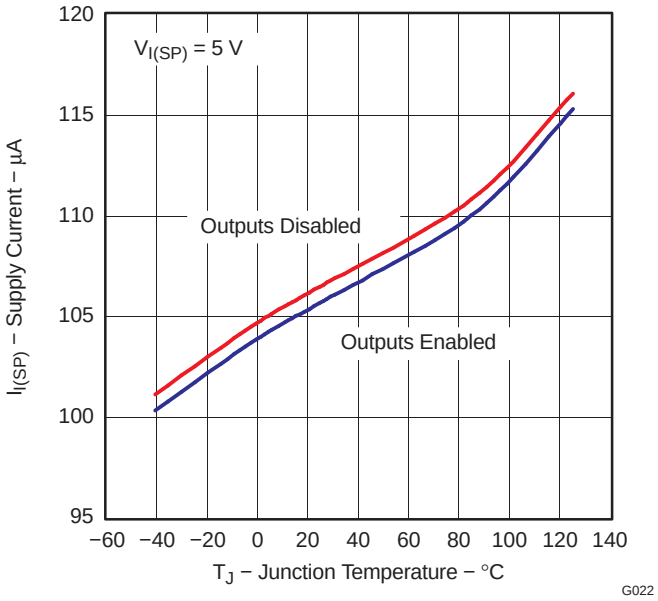



**Figure 24.**

**SP SUPPLY CURRENT vs INPUT VOLTAGE**

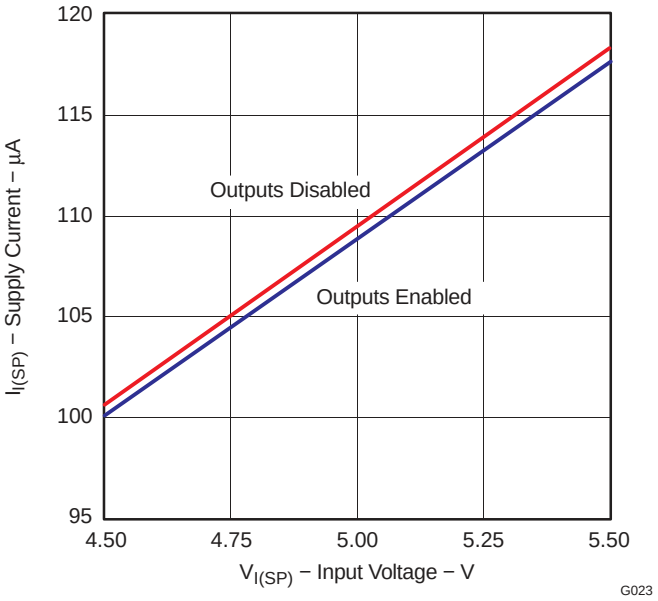



**Figure 25.**

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE (BUS-POWER SWITCHES)**

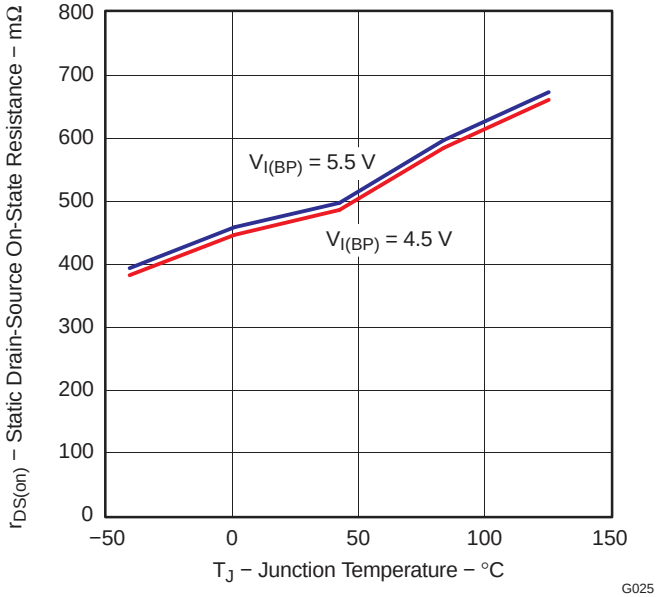



**Figure 26.**

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE (SELF-POWER SWITCHES)**

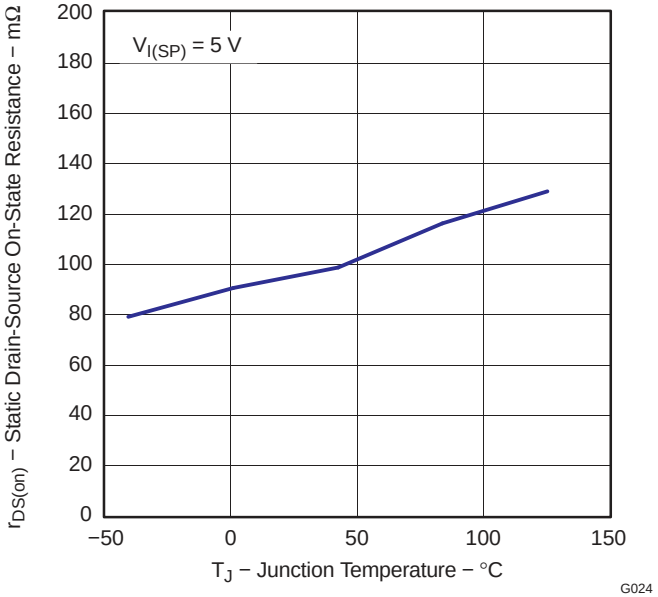



**Figure 27.**

## TYPICAL CHARACTERISTICS (continued)

**SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE (BUS-POWER SWITCHES)**

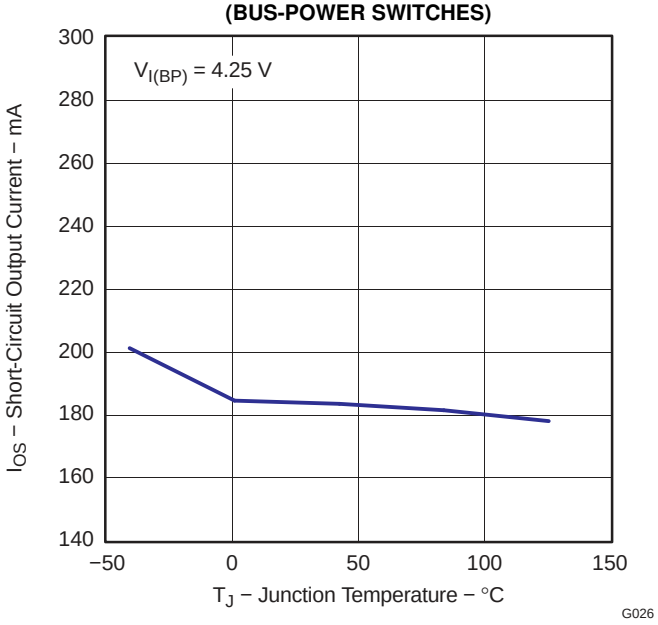



**Figure 28.**

**SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE (BUS-POWER SWITCHES)**

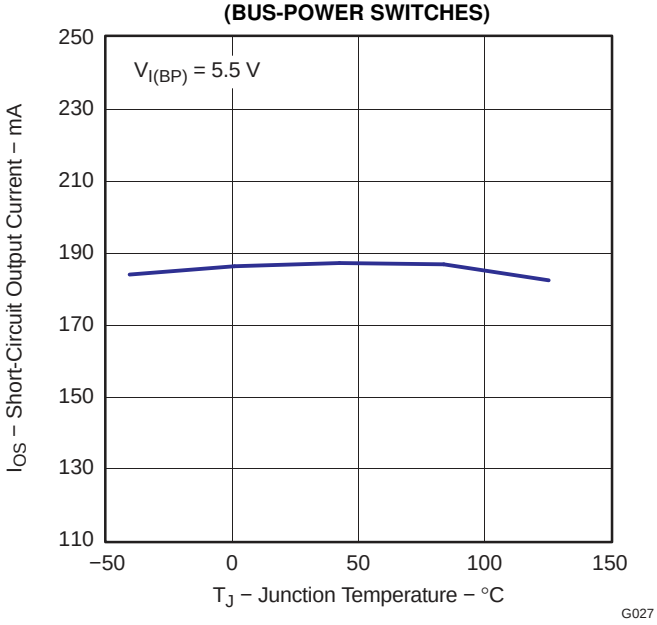



**Figure 29.**

**SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE (SELF-POWER SWITCHES)**

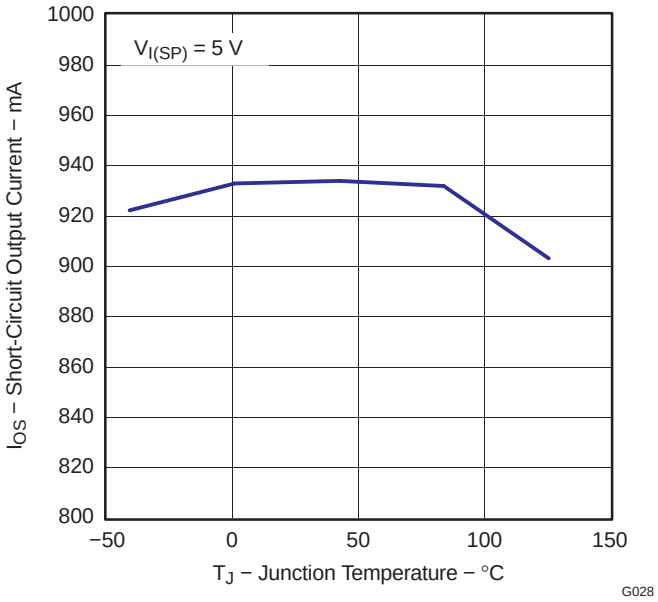



**Figure 30.**

**INPUT VOLTAGE (BP UNDERVOLTAGE LOCKOUT) vs JUNCTION TEMPERATURE**

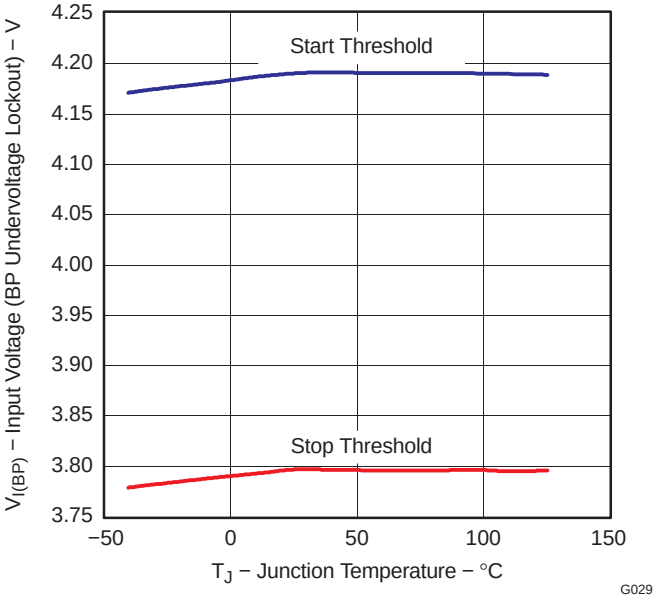



**Figure 31.**

## TYPICAL CHARACTERISTICS (continued)

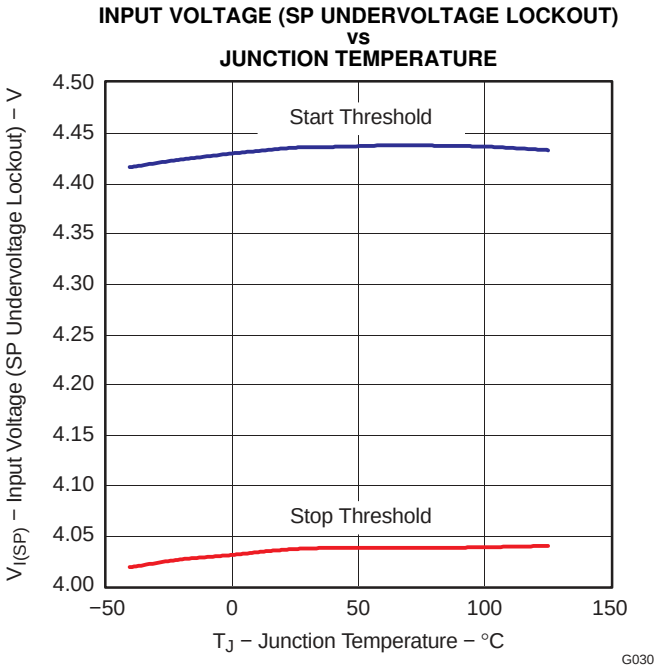



**Figure 32.**

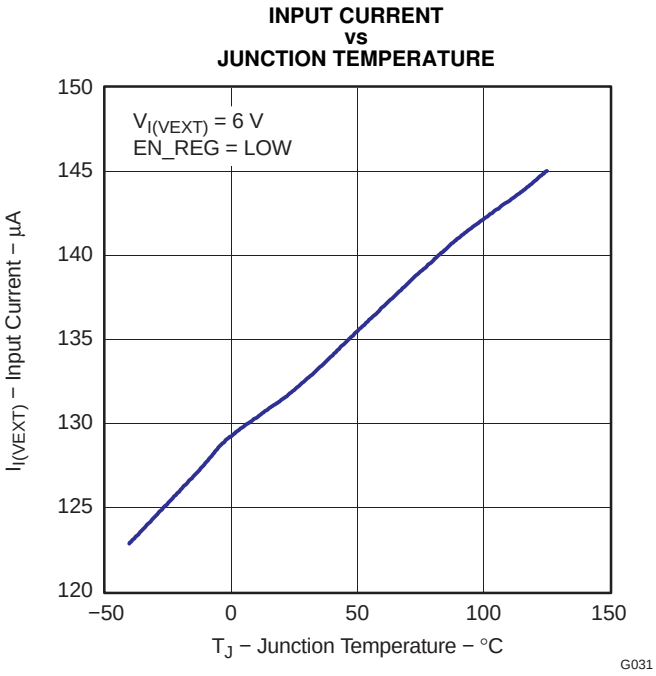



**Figure 33.**

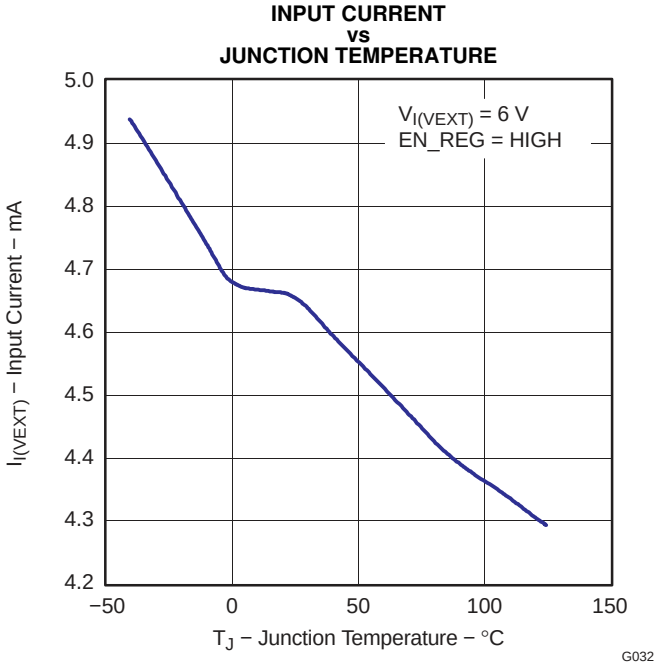



**Figure 34.**

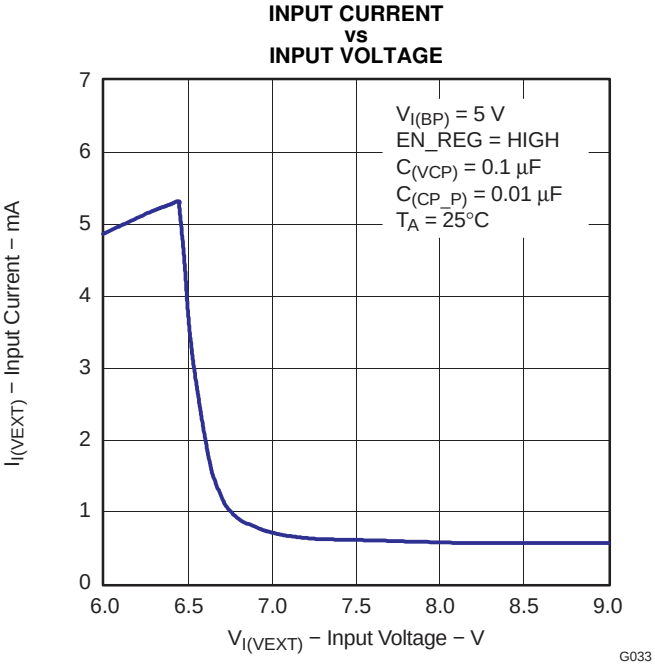



**Figure 35.**

## TYPICAL CHARACTERISTICS (continued)

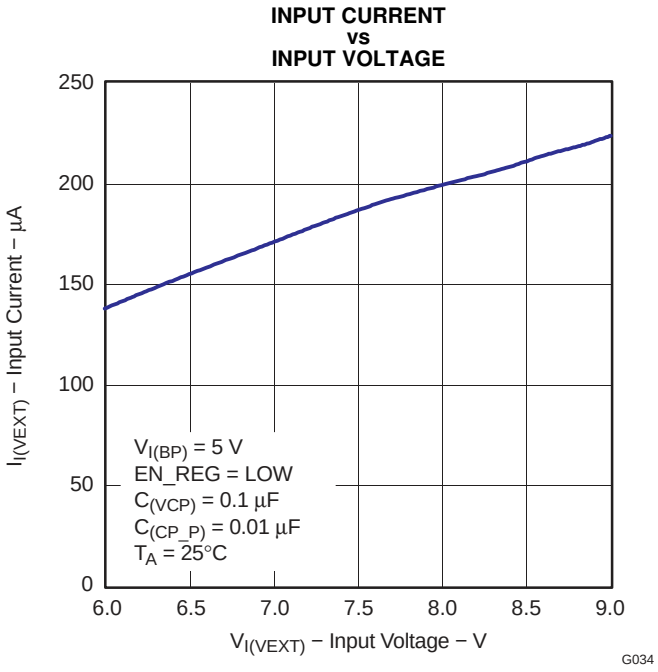



**Figure 36.**

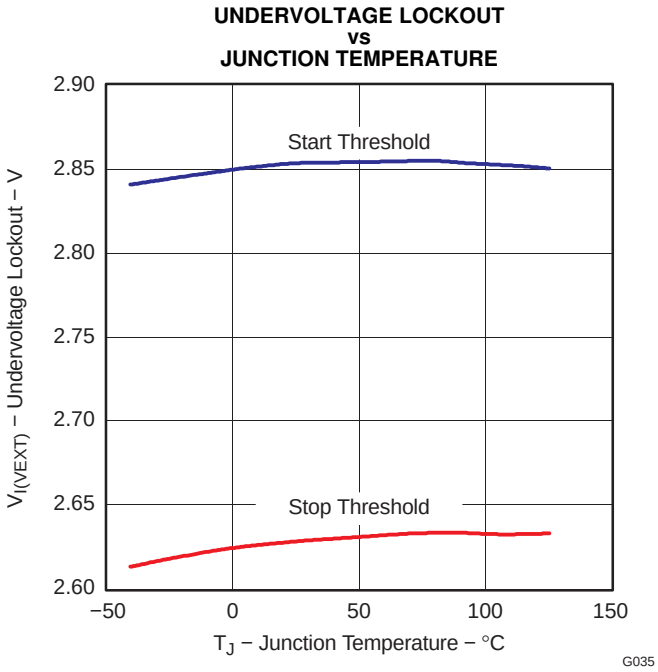



**Figure 37.**

# APPLICATION INFORMATION

## EXTERNAL CAPACITOR REQUIREMENTS

A 0.1-µF ceramic bypass capacitor and a 10-µF bulk capacitor between BP and AGND, close to the device, are recommended. Similarly, a 0.1-µF ceramic and a 68-µF bulk capacitor, from SP to AGND, and from VEXT to AGND if an external 5-V LDO is required, are recommended because of much higher current in the self-powered mode.

From each of the outputs (OUTx) to ground, a 33-µF or higher-valued bulk capacitor is recommended when the output load is heavy. This precaution reduces power-supply transients. Additionally, bypassing the outputs with a 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

An output capacitor connected between 3.3V_OUT and GND is required to stabilize the internal control loop. The internal LDO is designed for a capacitor range of 4.7 µF to 33 µF with an ESR of 0.2 Ω to 10 Ω. Solid tantalum-electrolytic, aluminum-electrolytic and multilayer ceramic capacitors are all suitable.

Ceramic capacitors have different types of dielectric material, each exhibiting different temperature and voltage variations. The most common types are X5R, X7R, Y5U, Z5U, and NPO. The NPO-type ceramic capacitors are generally the most stable over temperature. However, the X5R and X7R are also relatively stable over temperature (with the X7R being the more stable of the two) and are therefore acceptable for use. The Y5U and Z5U types provide high capacitance in a small geometry, but exhibit large variations over temperature. For this reason, the Y5U and Z5U are not generally recommended.

A transient condition occurs because of a sudden increase in output current. The output capacitor reduces the transient effect by providing the additional current needed by the load. Depending on the current demand at the output, a voltage drop occurs across the internal resistance, ESR, of the capacitor. Using a low-ESR capacitor helps minimize this voltage drop. A larger capacitor also reduces the voltage drop by supplying the current demand for a longer time, versus that provided by a smaller capacitor.

## OVERCURRENT

An internal sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before BP and SP have been applied. The TPS2070 and TPS2071 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a very short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS2070 and TPS2071 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

## $\overline{\text{OC}}$ RESPONSE

The $\overline{\text{OCx}}$ output is asserted (active-low) when an overcurrent or overtemperature condition is encountered and remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device and charging the downstream capacitor. The TPS2070 and TPS2071 are designed to reduce false overcurrent reporting by implementing an internal deglitch circuit. This circuit eliminates the need for an external filter, which requires extra components. Also, using low-ESR electrolytic capacitors on the outputs can reduce erroneous overcurrent reporting by providing a low-impedance energy source to lower the inrush current flow through the device during hot-plug events. The $\overline{\text{OCx}}$ outputs are logic outputs, thereby requiring no pullup or pulldown resistors.

## POWER DISSIPATION AND JUNCTION TEMPERATURE

The major source of power dissipation for the TPS2070 and TPS2071 comes from the internal voltage regulator and the N-channel MOSFETs. Checking the power dissipation and junction temperature is always a good design practice. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET according to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the graphs shown under the typical characteristics section of this data sheet. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by four to get the total power dissipation coming from the N-channel MOSFETs.

The power dissipation for the internal voltage regulator is calculated using:

$$P_D = (V_{I(BP)} - V_{O(min)}) \times I_{O(OUT)}$$

The total power dissipation for the device becomes:

$$P_{D(total)} = P_{D(voltage\ regulator)} + (4 \times P_{D(switch)})$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

where:

$T_A$ = ambient temperature in °C

$R_{\theta JA}$ = Thermal resistance in °C/W, equal to inverting of derating factor found on the power dissipation table in this data sheet

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

## THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods. The faults force the TPS2070 and TPS2071 into constant-current mode at first, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels.

The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2070 and TPS2071 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition, the junction temperature rises. Once the die temperature rises to approximately 140°C, the internal thermal-sense circuitry determines which power switch is in an overcurrent condition and turns only that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. If the die temperature exceeds the first thermal trip point of 140°C and reaches 150°C, the device turns off. The $\overline{OC}$ output is asserted (active-low) when overtemperature or overcurrent occurs.

## UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the device (LDO and switches) is in the off state at power up. The UVLO also keeps the device from being turned on until the power supply has reached the start threshold (see undervoltage lockout table), even if the switches are enabled. The UVLO activates whenever the input voltage falls below the stop threshold as defined in the undervoltage lockout table. This facilitates the design of hot-insertion systems, where it is not possible to turn off the power switches before input power is removed. Upon reinsertion, the power switches are turned on with a controlled rise time to reduce EMI and voltage overshoots.

## SELF-POWER TO BUS-POWER OR BUS-POWER TO SELF-POWER TRANSITION

An autoswitching function between bus-powered mode and self-powered mode is a feature of the TPS2070 and TPS2071. When this feature is enabled (BP_DIS is inactive) and SP is removed or applied, a transition is initiated. The transition sequence begins with the internal LDO being turned off and its external capacitance discharged. Any enabled switches are also turned off and the external capacitors discharged. Once the LDO and switch outputs are low, the internal logic turns the LDO back on. This entire sequence occurs whenever power to the SP input is removed or applied, regardless of the source of power, i.e., an external power supply or the use of the external regulator.

## UNIVERSAL SERIAL BUS (USB) APPLICATIONS

The universal serial bus interface is a 1.5/12-Mb/s (for USB), or 480 Mb/s (for Hi-Speed USB), multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V-level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub or across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2070 and TPS2071 can provide power-distribution solutions for hybrid hubs that need switching between BPH and SPH according to power availability and application requirements.

## USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

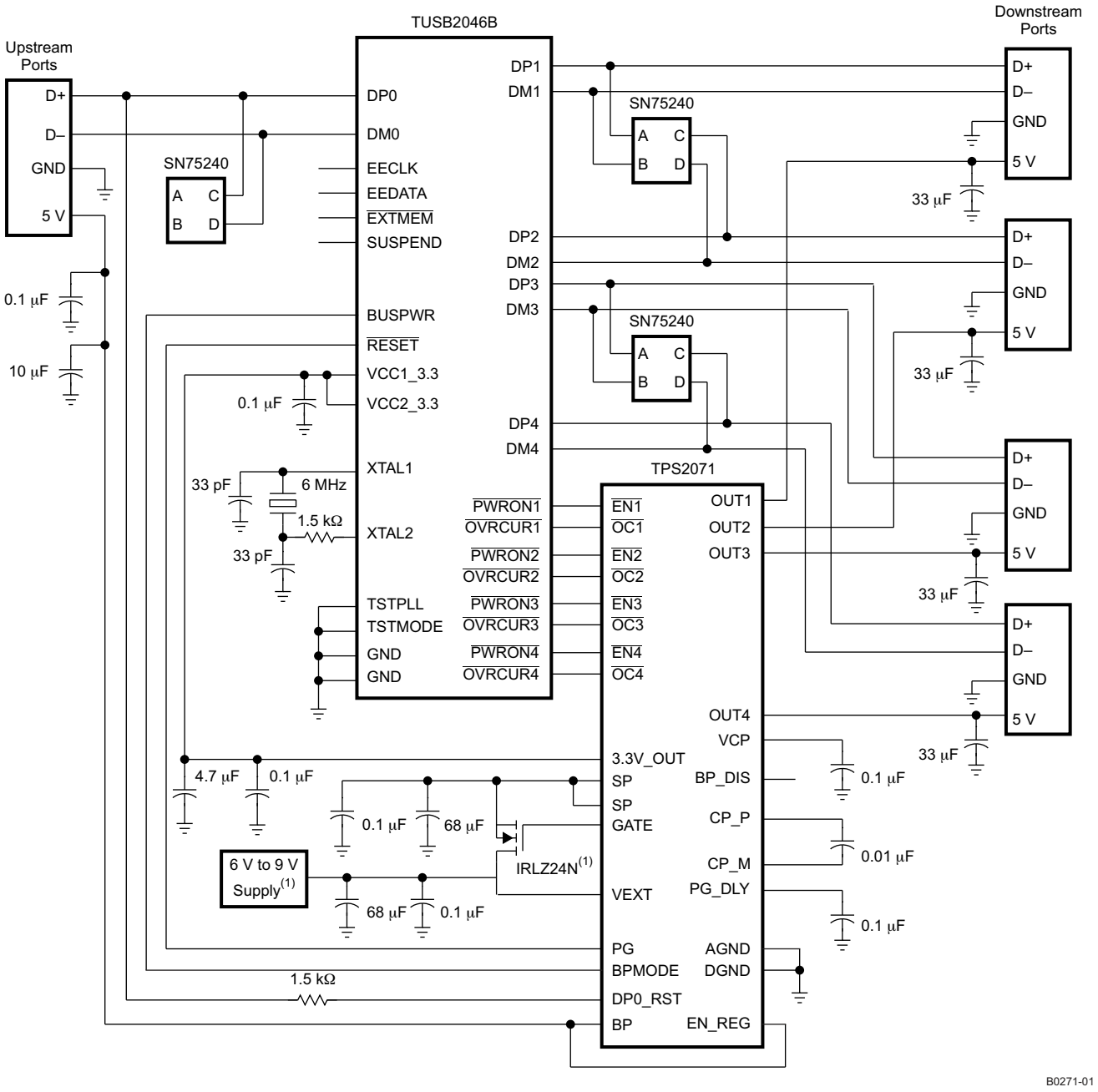
- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB $V_{BUS}$
  - Output 5.25 V to 4.75 V at 500 mA
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
  - Output 5.25 V to 4.4 V at 100 mA
  - Not send power back upstream
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA
  - Not send power back upstream (SP functions)

The feature set of the TPS2070 and TPS2071 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the needs of both input and output ports on hubs, as well as the input ports for bus-powered functions.

## USB HYBRID HUB

A USB hybrid hub can be simply implemented using the TPS2071 USB power controller and a TUSB2046 USB hub controller as shown in Figure 38. The TPS2071 USB power controller provides all the power needs to the four downstream ports and meets all the USB power specifications for both self-powered hubs and bus-powered hubs. The integrated 3.3-V LDO of the power controller is used to provide power for the hub controller and any other local functions (e.g., transient suppressor SN75240 ), which saves board space and cost. The TPS2071 also provides the hub controller with a power-good (PG) signal that connects to the $\overline{\text{RESET}}$ input of the hub controller to reinitialize the hub automatically when switching between self-powered mode and bus-powered mode whenever the self-power supply is connected or disconnected. The amount of time in which the hub controller is kept in a reset state is controlled by a capacitor connected between the PG_DLY pin of the power controller and ground.

By using an external N-channel MOSFET and the TPS2071 internal voltage-regulator controller, a regulated 5-V self-powered source can be generated from an input voltage range of 6 V to 9 V (see Figure 38). In this configuration, the internal voltage regulator controller is enabled by connecting the EN_REG input to the BP input. Using the internal voltage regulator controller also requires connecting a 0.01-µF capacitor between CP_P and CP_M of the TPS2071 power controller. Also, a 0.1-µF capacitor is needed between VCP of the power controller and ground.




(1) This hybrid hub can also be implemented by connecting a 5-V power supply to the SP input of the TPS2071 and eliminating the external FET. However, this type of implementation is best suited for the TPS2074/75 (see the *TPS2074, TPS2075 Four-Port USB Hub Power Controllers* data sheet, SLVS288, for details).

**Figure 38. USB Hybrid Hub Using TPS2071 Power Controller and TUSB2046 Hub Controller**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2070DAP | ACTIVE | HTSSOP | DAP | 32 | 46 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TPS2070 | Samples |
| TPS2071DAP | ACTIVE | HTSSOP | DAP | 32 | 46 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TPS2071 | Samples |
| TPS2071DAPG4 | ACTIVE | HTSSOP | DAP | 32 | 46 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TPS2071 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

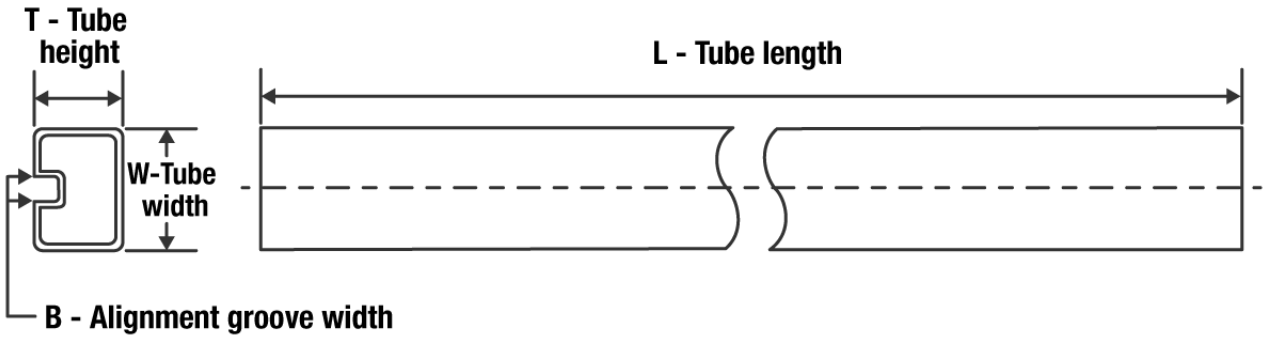
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS2070DAP | DAP | HTSSOP | 32 | 46 | 530 | 11.89 | 3600 | 4.9 |
| TPS2071DAP | DAP | HTSSOP | 32 | 46 | 530 | 11.89 | 3600 | 4.9 |
| TPS2071DAPG4 | DAP | HTSSOP | 32 | 46 | 530 | 11.89 | 3600 | 4.9 |

# GENERIC PACKAGE VIEW

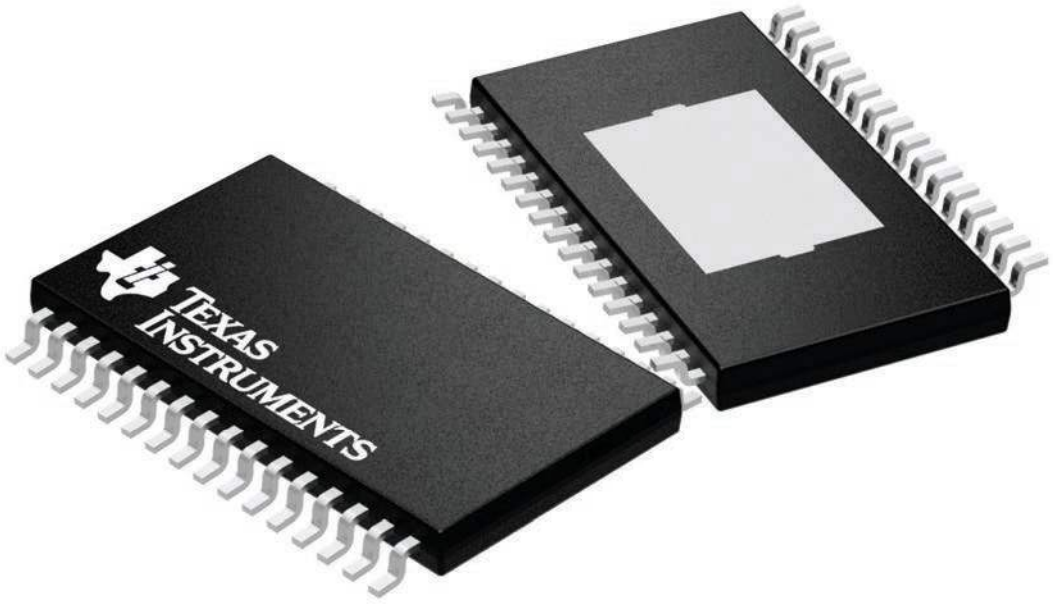
## DAP 32

## PowerPAD™ TSSOP - 1.2 mm max height

**8.1 x 11, 0.65 mm pitch**

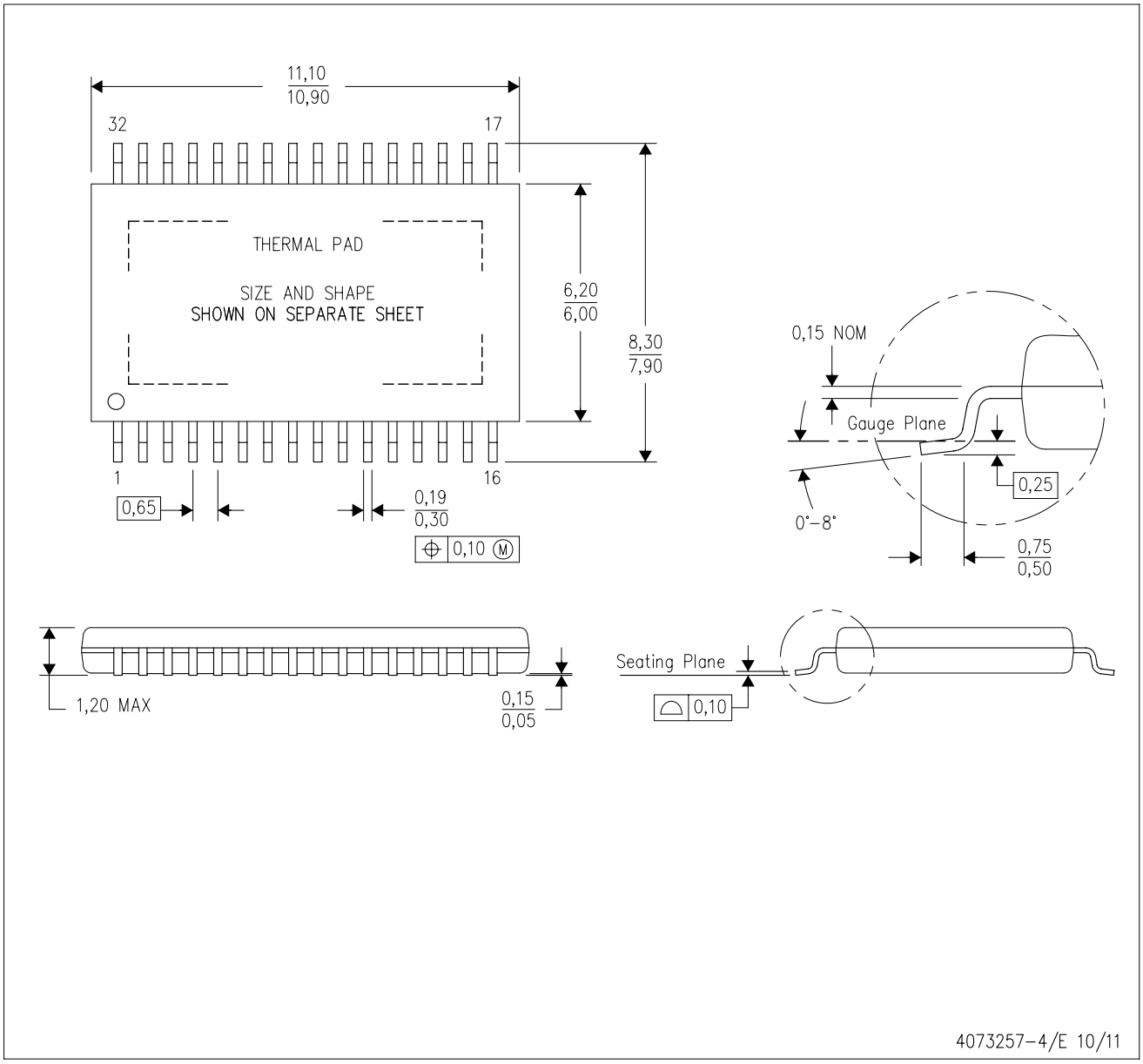
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4225303/A

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

**PowerPAD is a trademark of Texas Instruments.**

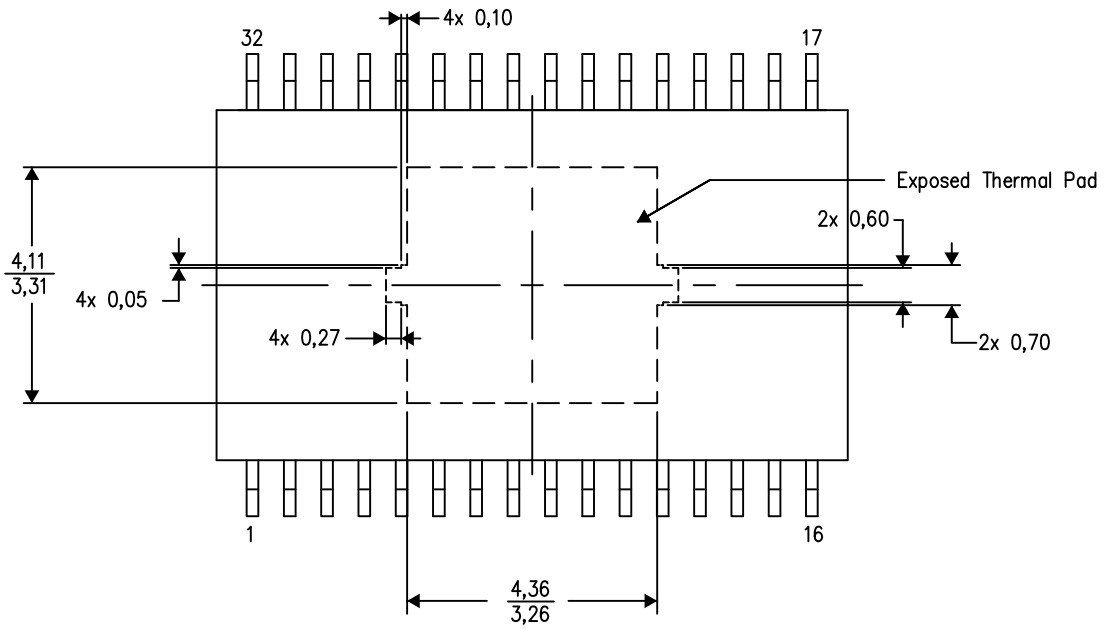
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

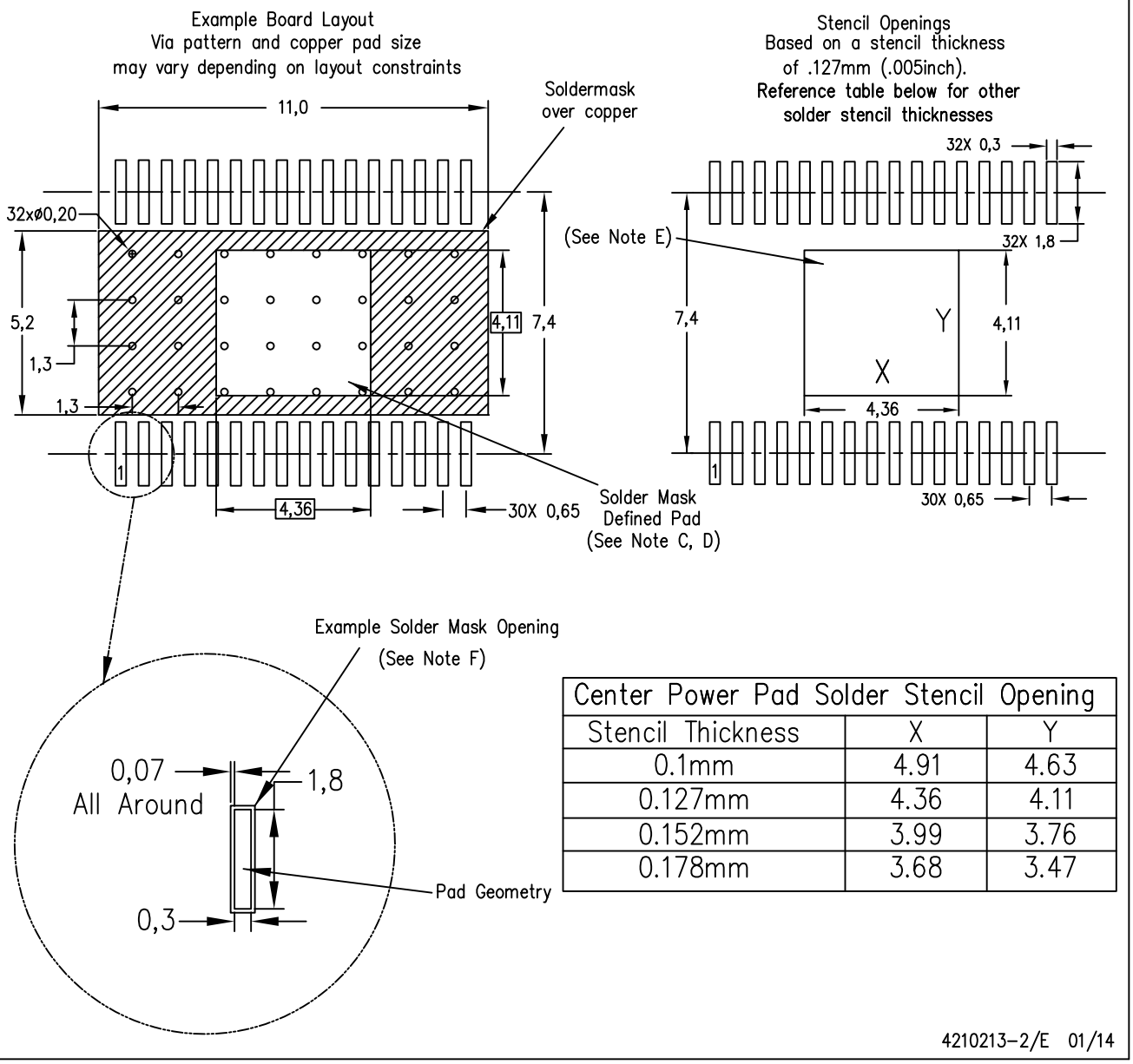
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

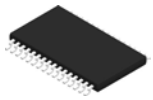
PowerPAD is a trademark of Texas Instruments.

# DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 4.91 | 4.63 |
| 0.127mm | 4.36 | 4.11 |
| 0.152mm | 3.99 | 3.76 |
| 0.178mm | 3.68 | 3.47 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

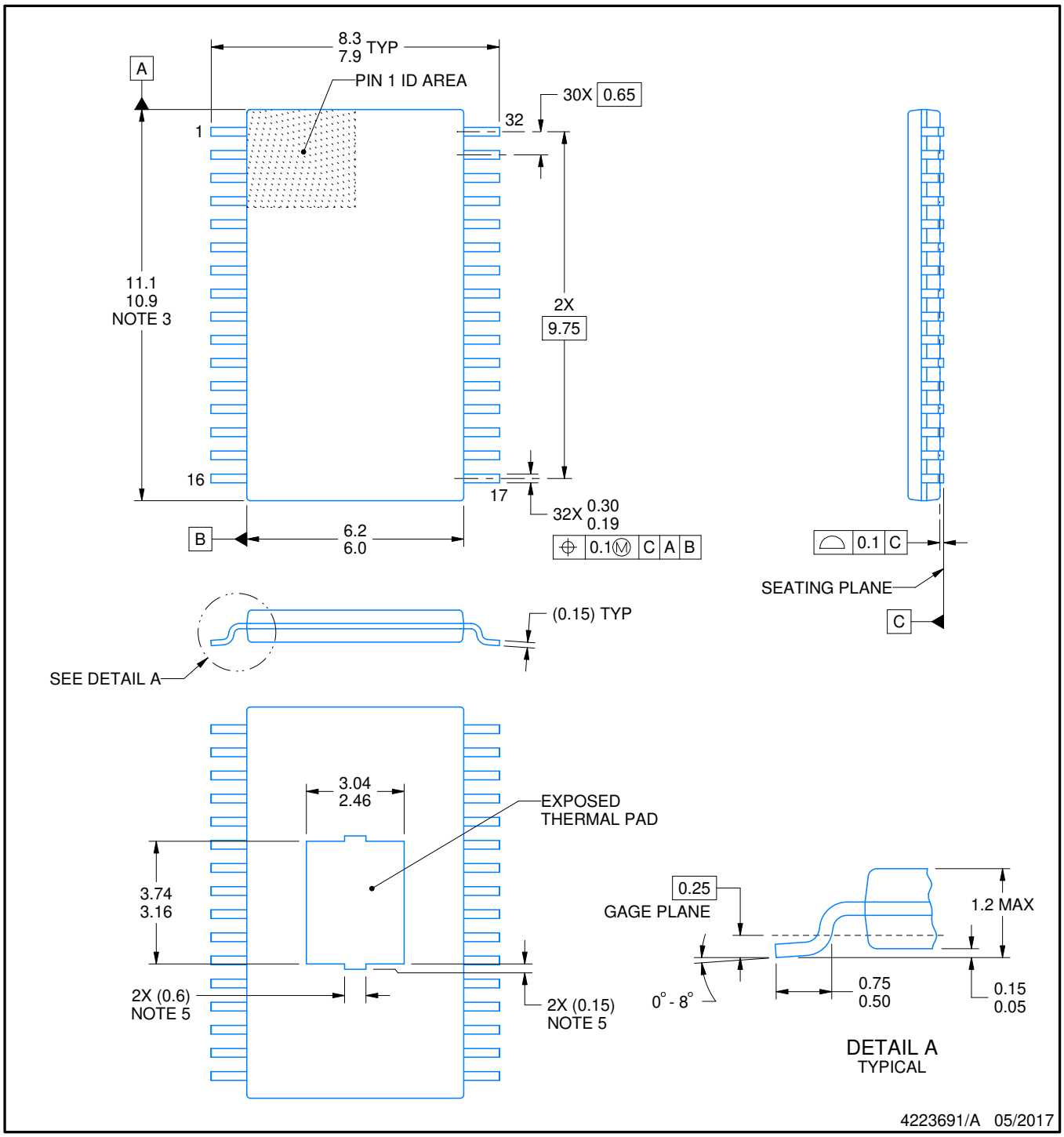


# PACKAGE OUTLINE

## DAP0032C

## PowerPAD™ TSSOP - 1.2 mm max height

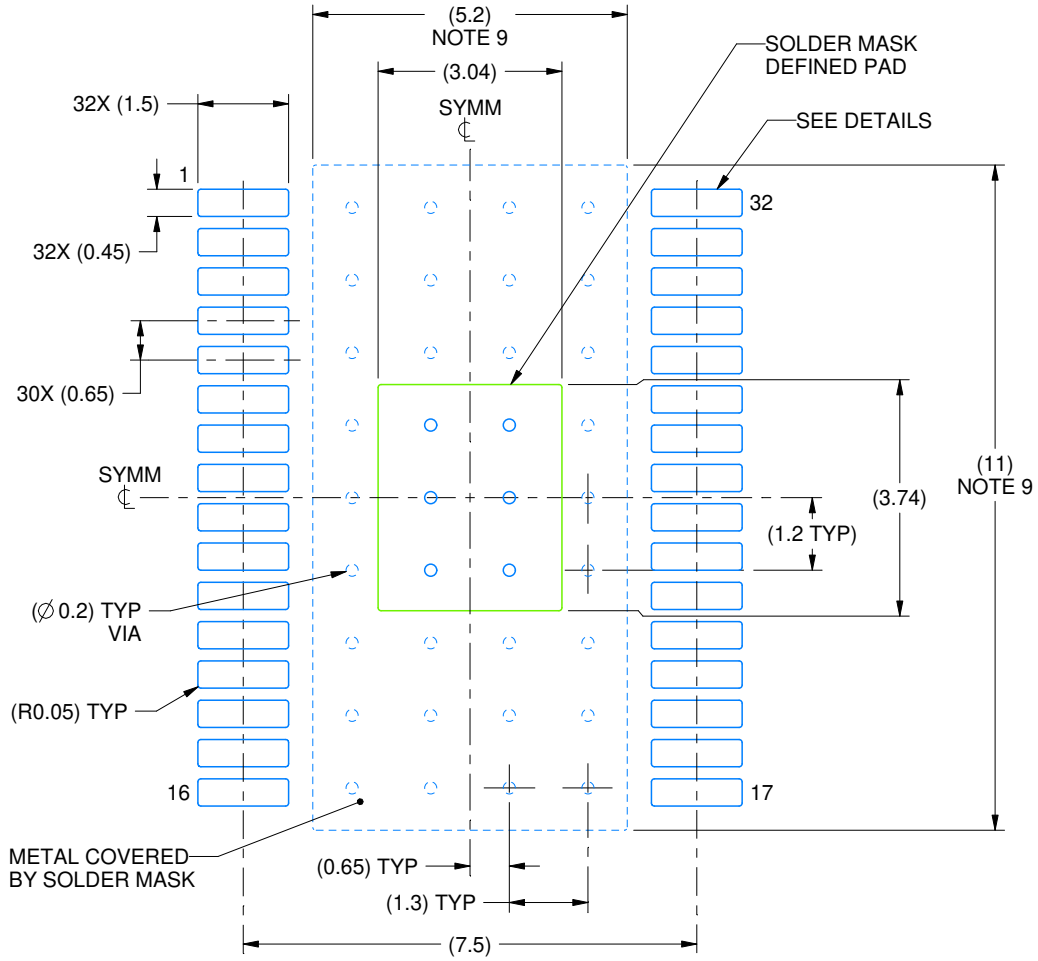
PLASTIC SMALL OUTLINE



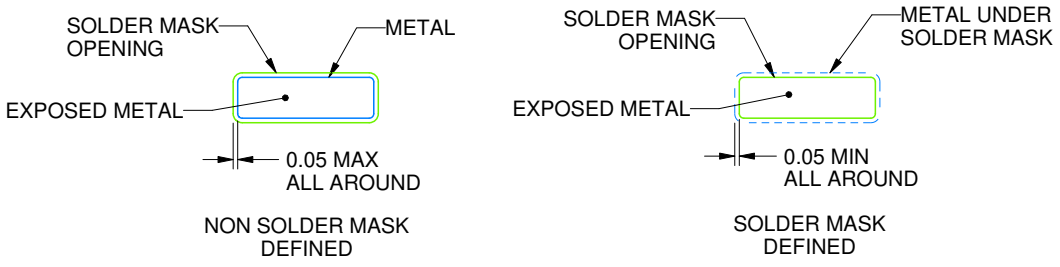

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

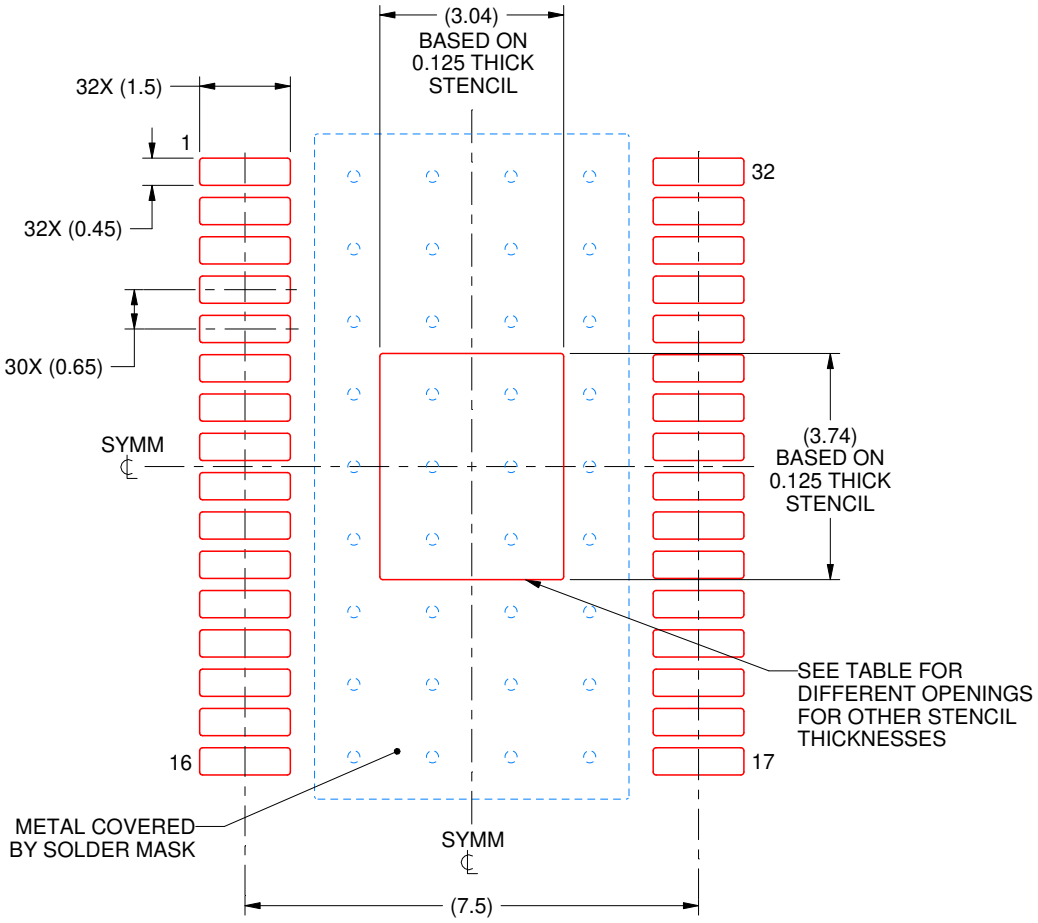



SOLDER MASK DETAILS
NOT TO SCALE

4223691/A 05/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.40 X 4.18 |
| 0.125 | 3.04 X 3.74 (SHOWN) |
| 0.15 | 2.78 X 3.41 |
| 0.175 | 2.57 X 3.16 |

4223691/A 05/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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