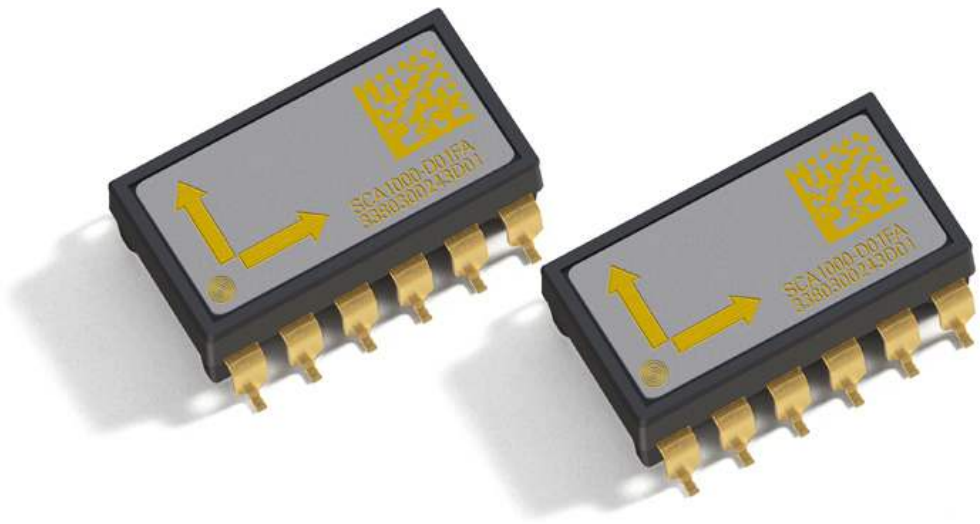
PRODUCT SPECIFICATION FOR
ZY-DUAL AXIS ACCELEROMETER
SCA1020 – D06



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1 General description

The SCA1020 accelerometer consists of two silicon bulk micro machined sensing element chips and a signal conditioning ASIC. The chips are mounted on a pre-molded package and wire bonded to appropriate contacts. The sensing elements and ASIC are protected with silicone gel and lid. The sensor has 12 SMD legs (Gull-wing type).

1.1 Block diagram

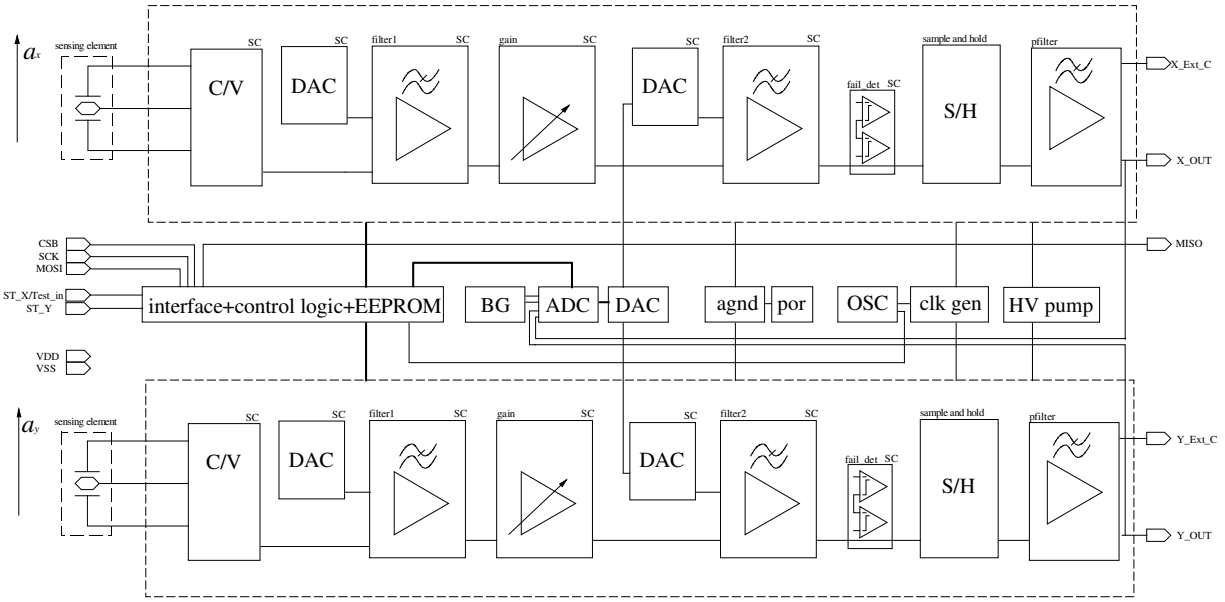


Figure 1. Block diagram of the SCA1020

1.2 SCA1020 family Accelerometer Features

- Single +5V supply
- Two ratiometric analog outputs in relation to supply voltage (Vdd = 4.75....5.25V)
  - Wide load driving capability
- Serial Peripheral Interface (SPI) compatible
  - Provides digital output for both channels
  - Supports testing and programming
- Non-volatile programming features
  - Factory programmable filter settings (400Hz, 1 kHz, WB, Ext_C)
  - Offset and sensitivity calibration
  - Linear temperature compensation
- Enhanced failure detection features
  - True self test by deflecting the sensing elements' proof mass by electrostatic force. Deflection voltage is adjustable with two memory bits for both channels. The self-test is channel specific, and separately activated for both channels by digital on-off commands via dedicated pins or via SPI bus.

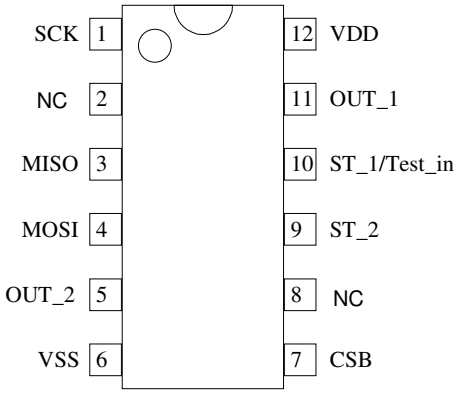
- Continuous sensing element interconnection failure check

2 Electrical specifications

2.1 Electrical Connection

The following is a typical requirement for electrical interface to the SCA1020. If special over voltage or reverse polarity protection is needed, please contact VTI Technologies for application information.

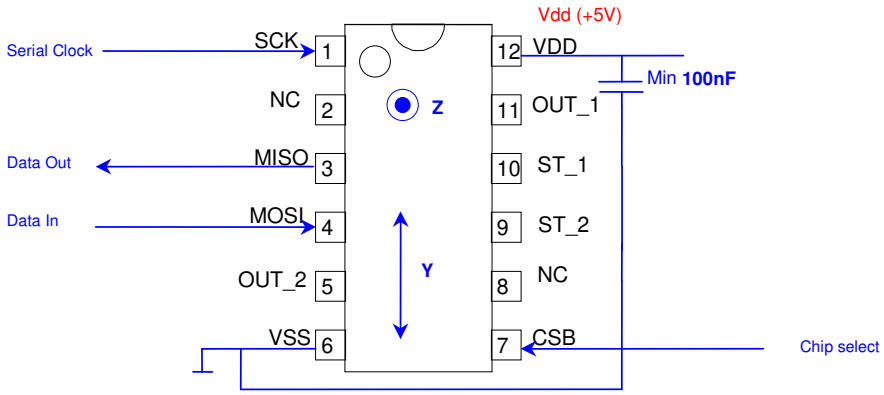
If self test (Pins 9 and 10) is not used, it should be left floating / grounded



No.	Node	I/O	Description
1	SCK	Input	Serial clock
2	NC	NC	NC
3	MISO	Output	Master in slave out; data output
4	MOSI	Input	Master out slave in; data input
5	Out_2	Output	Y axis Output (Ch 2)
6	VSS	Power	Negative supply voltage (V_{SS})
7	CSB	Input	Chip select (active low). If only analog outputs are used this should be connected to Vdd or left floating.
8	NC	NC	NC
9	ST_2	Input	Self test input for Y axis (Ch 2)
10	ST_1 / Test_in	Input	Self test input for Z axis (Ch 1) / Analog test input
11	Out_1	Output	Z axis output (Ch 1)
12	VDD	Power	Positive supply voltage (V_{DD})

Figure 2. Pin layout and description of the SCA1020

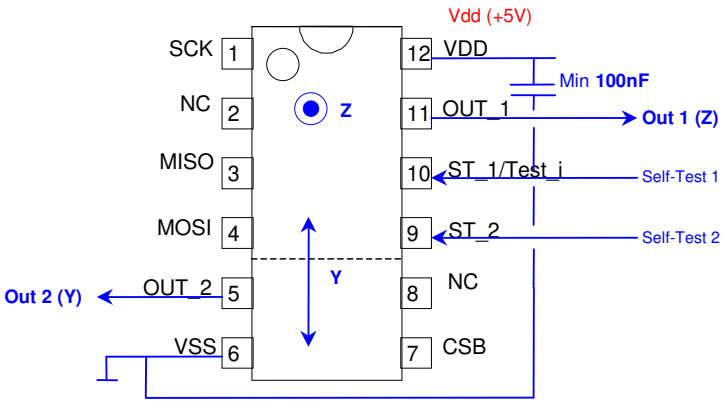
2.1.1 Recommended connection when SPI interface is used



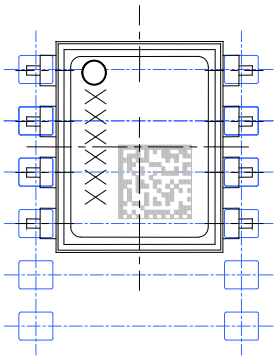
Recommended SPI-Output connection on PCB

2.1.2 Recommended connection when analog output is used

When SCA1020 is used in Analog mode and the PCB is designed correctly the SCA610 / 620 and SCA1020 are interchangeable. If the PCB layout is designed for SCA1020, then SCA610 / 620 can be used for single axis applications. Pins 1, 2, 3, 4 and 8 can be connected to GND (pins 2 and 8 can be connected also to Vdd) but for the best EMC performance these pins should be left floating. CSB pin can be pulled up but it is recommended to left floating. The output of SCA610 / 620 corresponds to the output of channel 1 in the SCA1020



Recommended Analog output

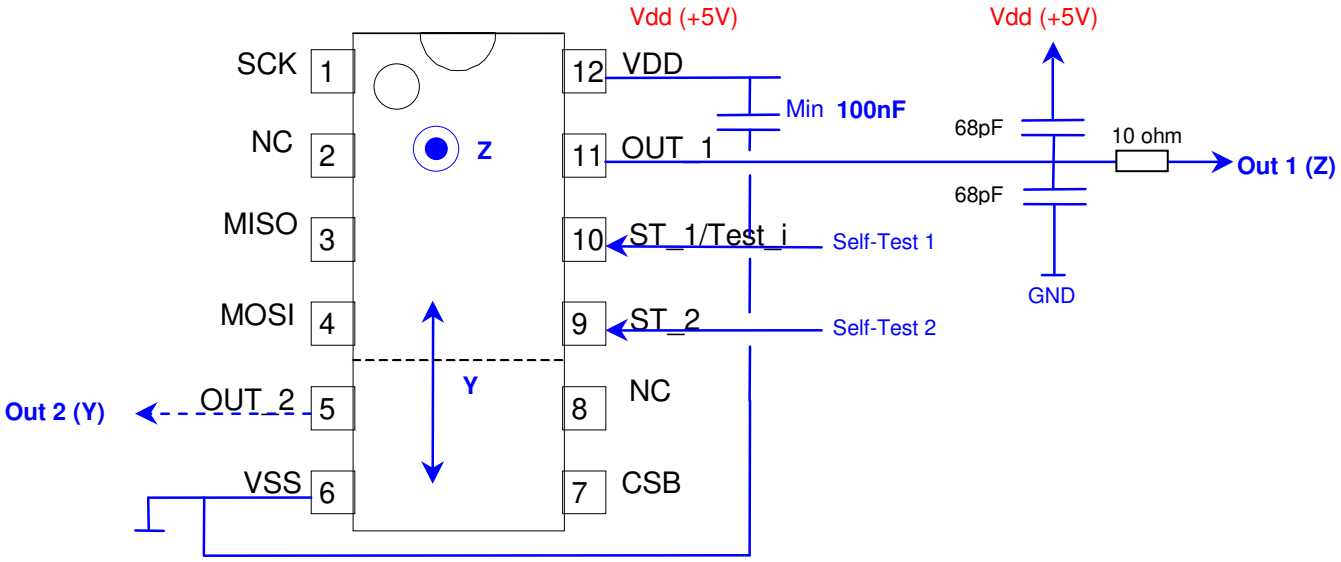


SCA610 or SCA620 connected to the SCA1020 lay-out

2.1.3 Recommended EMC protection circuitry

The purpose of the following recommendation is to give generic EMC protection guidelines for the SCA1020. EMC susceptibility is highly dependent on the PCB layout and therefore the component values given here can be different depending on the actual PCB layout. With the following circuitry and properly designed PCB the part will pass 200V/m EMC susceptibility tests.

Please note that only channel 1 output protection circuitry is presented. Similar kind of circuit must be also at the channel 2 output.



Recommended EMC protection circuitry

2.2 Absolute maximum ratings

Supply voltage (V_{DD})	-0.3 V to +5.5V (continuous) -0.3V to 7V (5 seconds during 1 minutes cycle)
Voltage at input / output pins	-0.3V to (V_{DD} + 0.3V)
ESD	
HBM (Human Body Model)	±2kV
CDM (Charged Device Model)	±500V
Storage temperature	-55°C to +125°C
Operating temperature	-40°C to +125°C
Mechanical shock	Drop from 1 meter on a concrete surface.

2.3 Electrical Specification of the SCA1020 – D06

2.3.1 Analog Output

Vdd = 5.00V and ambient temperature (23°C±5°C) unless otherwise specified.

KPC[17]	Parameter	Condition	Min.	Typ	Max.	Units
	Z axis (Out_1) Measuring range [1]	Nominal	-1.7		+1.7	g [2]
	Y axis (Out_2) Measuring range [1]	Nominal	-1.7		+1.7	g [2]
	Supply voltage Vdd		4.75	5.0	5.25	V
<CC>	Current consumption	Vdd = 5 V; No load			5.0	mA
	Operating temperature		-40		+125	°C
	Resistive output load (Analog Output)	Vout to Vdd or Vss	10			kOhm
	Capacitive load (Analog Output)	Vout to Vdd or Vss			20	nF
	Min. output voltage; Vdd = 5V	10k from Vout to Vdd	0		0.25	V
	Max. output voltage; Vdd = 5V	10k from Vout to Vss	4.75		5.00	V
<CC>	Z axis (Out_1) Offset (output at 0g) [3, 13]	@ room temperature		Vdd/2		V
<CC>	Z axis (Out_1) Sensitivity [4, 13]	@ room temperature		0.24 x Vdd		V/g
<SC>	Z axis (Out_1) Offset Error (output at 0g) [5, 13]	RT(23±5°C) -20...+85°C -40…+125°C	-40 -75 -90	- - -	+40 +75 +90	mg
<SC>	Z axis (Out_1) Offset Temperature Dependency (output at 0g) [5, 13,14]	-20...+85°C -40…+125°C	-35 -50	- -	+35 +50	mg
<SC>	Z axis (Out_1) Sensitivity error [6, 13]	-40...+85°C -40...+125°C	-4	±3 -	+4	%
<CC>	Y axis (Out_2) Offset (output at 0g) [3, 13]	@ room temperature		Vdd/2		V
<CC>	Y axis (Out_2) Sensitivity [4, 13]	@ room temperature		0.24 x Vdd		V/g
<SC>	Y axis (Out_2) Offset Error (output at 0g) [5, 13]	RT(25±5°C) -20...+85°C -40…+125°C	-40 -75 -90	- - -	+40 +75 +90	mg
<SC>	Y axis (Out_2) Offset Temperature Dependency (output at 0g) [5, 13,14]	-20...+85°C -40…+125°C	-35 -50	- -	+35 +50	mg
<SC>	Y axis (Out_2) Sensitivity error [6, 13]	-40...+85°C -40...+125°C	-4	±3 -	+4	%
	Typical non-linearity [7]	Range = -1g...+1g	-20	-	+20	mg
	Z axis (Out_1) Frequency response -3dB [8]		20	50	80	Hz
	Y axis (Out_2) Frequency response -3dB [8]		20	50	80	Hz
	Ratiometric error [9]	Vdd = 4.75...5.25V	-2	-	2	%
<SC>	Cross-axis sensitivity [10]	@ room temperature			3.5	%
	Output noise [11]	From DC...4kHz			5	mVrms
	Start-up delay	Reset and parity check			10	ms
	Self test input pull down current	Vdd = 5V	10	21	30	µA
	T1: T st-on[15]	Self test ON period. Controlled externally by user	10		100	ms
	T2: Tsat.del. [15]	Saturation delay. Time when element beam remains still out from linear operating range.			20	ms

	T3: T recov. [15]	Recovery time when element is back in linear operating range			50	ms
	T4: T stab. [15] = T2+T3	Stabilization time, when self test is released.			70	ms
	T5: T r [15]	Rise time during self test, when Vout reach V2			10	ms
	V2 [15]	Vout during self test	4.75			V
	V3 [15, 16]	Stabilized output voltage after self-test is released.	0.95*V1	V1	1.05 * V1	

Note 1. The measuring range is limited only by the sensitivity, offset and supply voltage rails of the device

Note 2. 1g = 9.82m/S^2

Note 3. Offset specified as Voffset = Vout(0g) [V]. See note 13.

Note 4. Sensitivity specified as Vsens = {Vout(+1g) - Vout(-1g)}/2 [V/g]. See note 13

Note 5. Offset error specified as Offset Error = {Vout(0g) - Vdd/2} / Vsens [g]
Vsens = Nominal sensitivity
Vdd/2 = Nominal offset
See note 13.

Note 6. Sensitivity error specified as Sensitivity Error = { [Vout(+1g) - Vout(-1g)] / 2 - Vsens} / Vsens x 100% [%]
Vsens = Nominal sensitivity
See note 13.

Note 7. From straight line through -1g and +1g.

Note 8. The frequency response is determined by the sensing element's internal gas damping. The output has true DC (0Hz) response.

Note 9. The ratiometric error is specified as.

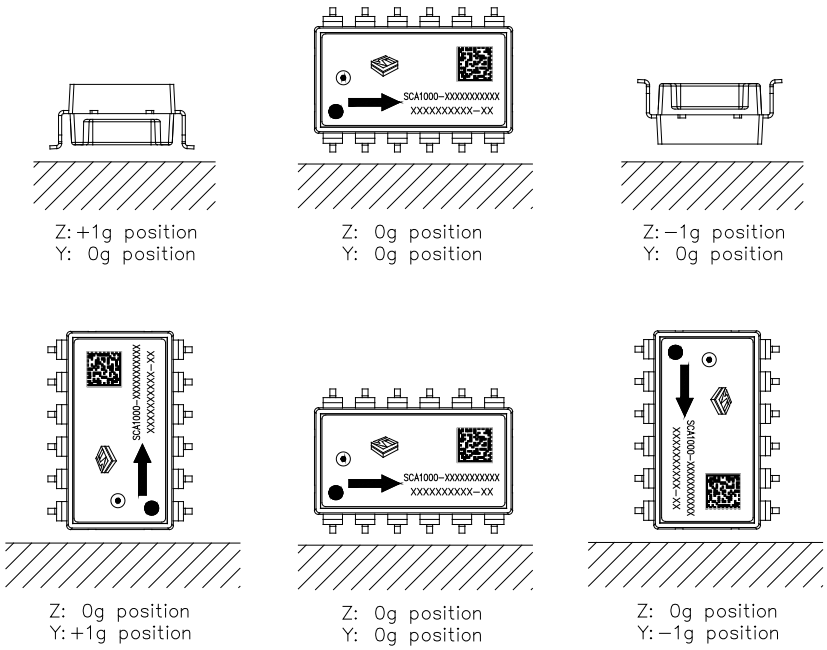
$$RE = 100\% \times \left(1 - \frac{Vout(@\,Vx) \times \frac{5.00V}{Vx}}{Vout(@5V)} \right)$$

Note 10. The cross-axis sensitivity determines how much acceleration, perpendicular to the measuring axis, couples to the output. The total cross-axis sensitivity is the geometric sum of the sensitivities of the two axes that are perpendicular to the measuring axis.

Note 11. In addition, supply voltage noise couples to the output due to the ratiometric nature of the accelerometer.

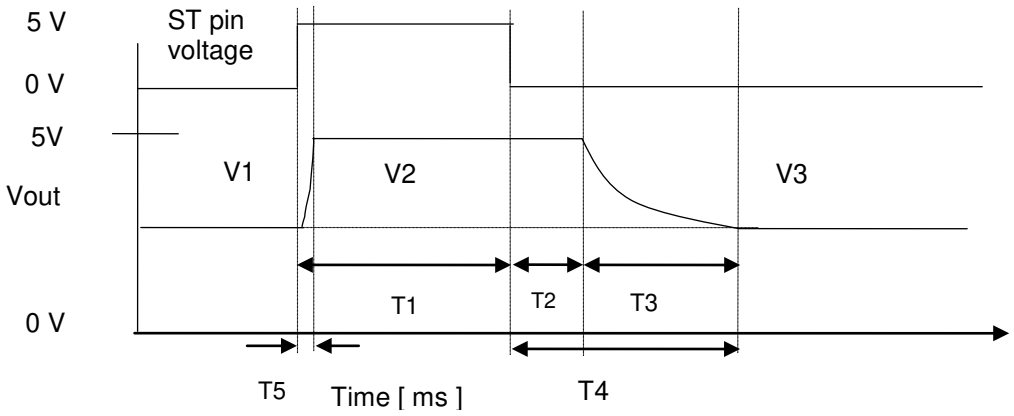
Note 12. The self-test will increase the output voltage. The output will go to Vdd rail. The purpose of the self-test is to check out the total functionality of the sensor. It is not meant for calibration or auto zeroing.

Note 13. Measuring positions



Note 14. Offset Temperature Dependency (Offset Tdep) specified as
Offset Tdep = {Vout(0g@RT) - Vout(0g@T) } / Vsens [g]
Vout(0g@RT) = Vout(0g) at room temperature (23±5°C)
Vout(0g@T) = Vout(0g) at temperature T
Vsens = Nominal sensitivity
See note 13.

Note 15. Self-test waveforms at 0g position (Z=0g and Y=0g):



Note 16. V1= Initial output Voltage before self-test activation
V3= Output voltage after self-test has been removed and after stabilization time. Please note that the error band specified for V3 is to guarantee that the output is within 5% of the initial value after the specified stabilization time.
After longer time V1=V3.

Note 17. CC= Critical Characteristics. Must be 100% monitored during production
SC= Significant Characteristic. The process capability (Cpk) must be better than 1.33, which allows sample based testing. If process is not capable the part will be 100% tested

2.3.2 Digital Output

Vdd = 5.00V and ambient temperature unless otherwise specified.

Parameter	Condition	Min.	Typ	Max.	Units
Output load	@500kHz			1	nF
SPI clock frequency				500	kHz
Internal A/D conversion time				150	µs
Data transfer time	@500kHz			38	µs

3 SPI Interface

Serial peripheral interface (SPI) is a 4-wire synchronous serial interface. Data communication is enabled with low active Slave Select or Chip Select wire (CSB). Data is transmitted with 3-wire interface consisting of serial data input (MOSI), serial data output (MISO) and serial clock (SCK). Every SPI system consists of one master and one or more slaves, where the master is defined as the microcomputer that provides the SPI clock, and the slave is any integrated circuit that receives the SPI clock from the master.

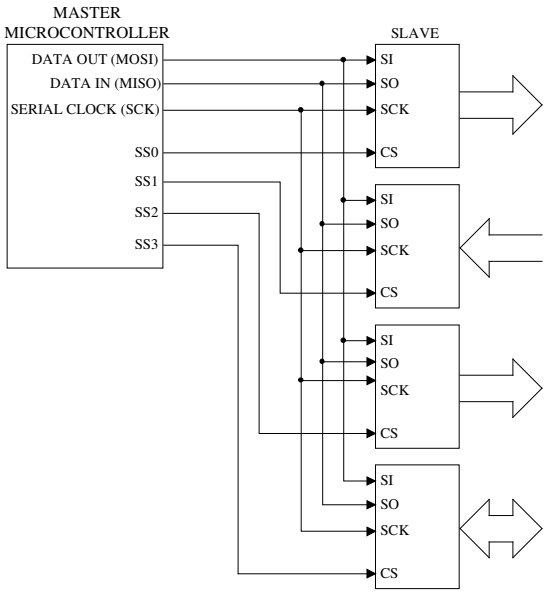


Figure 4. Typical SPI connection

The SPI interface of this ASIC is designed to support almost any micro controller that uses software implemented SPI. However it is not designed to support any particular hardware implemented SPI found in many commercial micro controllers. Serial peripheral interface in this product is used in testing and calibration purposes as well as in the final application. In normal use some testing and calibration commands are disabled and have not been documented here. This ASIC operates always as a slave device in the master-slave operation mode. The data transfer between the master (µP test machine etc.) and ASIC is performed serially with four wire system.

MOSI	master out slave in	µP → ASIC
MISO	master in slave out	ASIC → µP
SCK	serial clock	µP → ASIC
CSB	chip select (low active)	µP → ASIC

Each transmission starts with a falling edge on CSB and ends with the rising edge. During the transmission, commands and data are controlled by SCK and CSB according to the following rules:

- commands and data are shifted MSB first LSB last
- each output data/status-bits are shifted out on the falling edge of SCK (MISO line)
- each bit is sampled on the rising edge of SCK (MOSI line)

- after the device is selected with CSB going low, an 8-bit command is received. The command defines the operations to be performed
- the rising edge of CSB ends all data transfer and resets internal counter and command register
- if an invalid command is received, no data will be shifted into chip and the MISO will remain in high impedance state until the falling edge of CSB. This will reinitialize the serial communication.
- to be able to perform any other command than those listed in Table 1. *SPI commands,* the lock register content has to be set correctly. If other command is feed without correct lock register content, no data will be shifted into chip and the MISO will remain in high impedance state until the falling edge of CSB.
- data transfer to MOSI continues right after the command is received in all cases where data is to be written to ASIC's internal registers
- data transfer out from MISO starts with a falling edge of SCK right after the last bit of SPI command is sampled in on the rising edge of SCK
- maximum data transfer speed exceeds 500 kHz clock rate

SPI command can be an individual command or a combination of command and data. In the case of combined command and data, the input data follows uninterruptedly the SPI command and the output data is shifted out parallel with the input data.

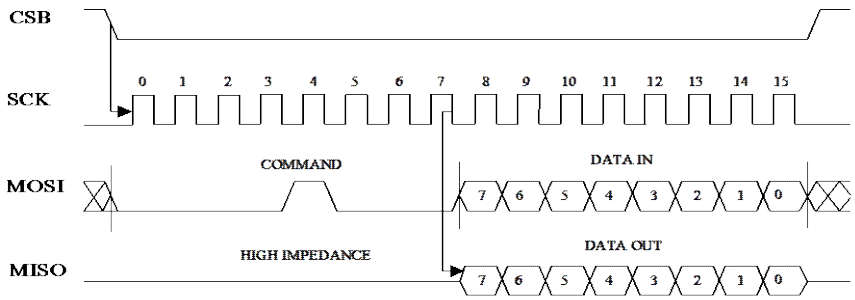


Figure 5. One command and data transmission over the SPI

After power up the circuit starts up in measure mode. This is the operation mode that is used in the final application.

3.1 DC characteristics of SPI interface

Supply voltage is 5 V unless otherwise noted. Current flowing into the circuit has positive values.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input terminal CSB						
Pull up current	V_{IN} = 0 V	I_{PU}	13	22	35	µA
Input high voltage		V_{IH}	4		Vdd+0.3	V
Input low voltage		V_{IL}	-0.3		1	V
Hysteresis		V_{HYST}		0.23*Vdd		V
Input capacitance		C_{IN}		2		pF
Input terminal MOSI, SCK						
Pull down current	V_{IN} = 5 V	I_{PD}	9	17	29	µA
Input high voltage		V_{IH}	4		Vdd+0.3	V
Input low voltage		V_{IL}	-0.3		1	V
Hysteresis		V_{HYST}		0.23*Vdd		V
Input capacitance		C_{IN}		2		pF
Output terminal MISO						
Output high voltage	I > -1mA	V_{OH}	Vdd-0.5			V
Output low voltage	I < 1 mA	V_{OL}			0.5	V
Tristate leakage	0 < V_{MISO} < Vdd	I_{LEAK}		5	100	pA

Table 1. DC characteristics of SPI interface

3.2 AC characteristics of SPI interface

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Terminal CSB, SCK						
Time from CSB (10%) to SCK (90%)[1]		T_{LS1}	120			ns
Time from SCK (10%) to CSB (90%)[1]		T_{LS2}	120			ns
Terminal SCK						
SCK low time	Load capacitance at MISO < 2 nF	T_{CL}	1			µs
SCK high time	Load capacitance at MISO < 2 nF	T_{CH}	1			µs
Terminal MOSI, SCK						
Time from changing MOSI (10%, 90%) to SCK (90%)[1]. Data setup time		T_{SET}	30			ns
Time from SCK (90%) to changing MOSI (10%,90%)[1]. Data hold time		T_{HOL}	30			ns
Terminal MISO, CSB						
Time from CSB (10%) to stable MISO (10%, 90%)[1].	Load capacitance at MISO < 15 pF	T_{VAL1}	10		100	ns
Time from CSB (90%) to high impedance state of MISO[1].	Load capacitance at MISO < 15 pF	T_{LZ}	10		100	ns
Terminal MISO, SCK						
Time from SCK (10%) to stable MISO (10%, 90%)[1].	Load capacitance at MISO < 15 pF	T_{VAL2}			100	ns
Terminal CSB						
Time between SPI cycles, CSB at high level (90%)		T_{LH}	15			µs

[1] not production tested

Table 2. AC characteristics of SPI interface

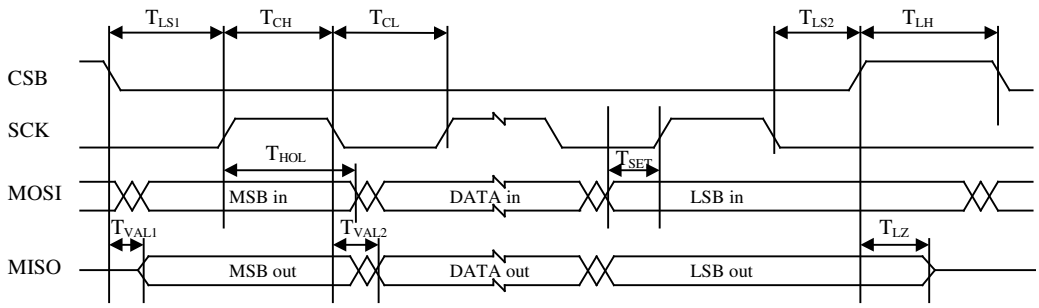


Figure 6. SPI bus timing diagram

3.3 SPI Commands

This SPI interface utilizes an 8-bit instruction (or command) register. The list of commands available to end-user is presented in Table 3.

Command name	Command format	Description:
MEAS	00000000	Measure mode (normal operation mode after power on)
RWTR	00001000	Read and write temperature data register
RDSR	00001010	Read status register
RLOAD	00001011	Reload NV data to memory output register
STX	00001110	Activate Self test for Z-channel
STY	00001111	Activate Self test for Y-channel
RDAX	00010000	Read Z-channel acceleration through SPI
RDAY	00010001	Read Y-channel acceleration through SPI

Table 3. SPI commands

Measure mode (MEAS): Standard operation mode after power-up. During normal operation, MEAS command is exit command from Self-Test.

Read and write temperature data register (RWTR): Temperature data register can be read during normal operation without affecting the circuit operation. Temperature data register is loaded in every 150 μs, and the load operation is disabled whenever the CSB signal is low, hence CSB has to stay high at least 150 μs prior the RWTR command in order to guarantee correct data. The data transfer is as presented in Figure 5 and data is transferred MSB first. In normal operation, it doesn't matter what data is written to temperature data register during RWTR command and hence all zeros is recommended.

Read status register (RDSR): Read status register command provides access to the status register. Status register format is shown in Table 4. Bold values in Definition column are the expected values during normal operation.

Bit	Definition
Bit 3 (PERR)	**Bit 3 = 0 Parity check hasn't detected errors** Bit 3 = 1 Parity error detected
Bit 2 (TEST)	**Bit 2 = 0 Analog test mode isn't active** Bit 2 = 1 Analog test mode is active
Bit 1 (LOCK)	Bit 1 = 0 Lock register is open **Bit 1 = 1 Lock register is locked**
Bit 0 (PD)	**Bit 0 = 0 circuit is not in power down mode** Bit 0 = 1 circuit is in power down mode

Table 4. Status register bit definitions

Reload NV data to memory output register (RLOAD): Reads NV data from EEPROM to the memory output register.

Self test for Z-channel (STX): STX command activates the circuit's self test function for the Z-channel. Internal charge pump is activated and high voltage is applied to the Z-channel acceleration sensor element electrode. This causes electrostatic force, which deflects the beam of the sensing element and simulates the acceleration to the positive direction. Z-channel self-test is de-activated by giving MEAS command.

Self test for Y-channel (STY): STY command activates the circuit's self test function for the Y-channel. Internal charge pump is activated and high voltage is applied to the Y-channel acceleration sensor element electrode. This causes electrostatic force, which deflects the beam of the sensing element and simulates the acceleration to the positive direction. Y-channel self-test is de-activated by giving MEAS command.

Read Z-channel acceleration (RDAX): RDAX command provides access to AD converted Z-channel acceleration signal stored in acceleration data register X. During normal operation acceleration data register X is loaded in every 150 μs, and the load operation is disabled whenever the CSB signal is low, hence CSB has to stay high at least 150 μs prior the RDAX command in order to guarantee correct data. Data output is an 11-bit digital word, which is feed out MSB first and LSB last. (See Figure 7).

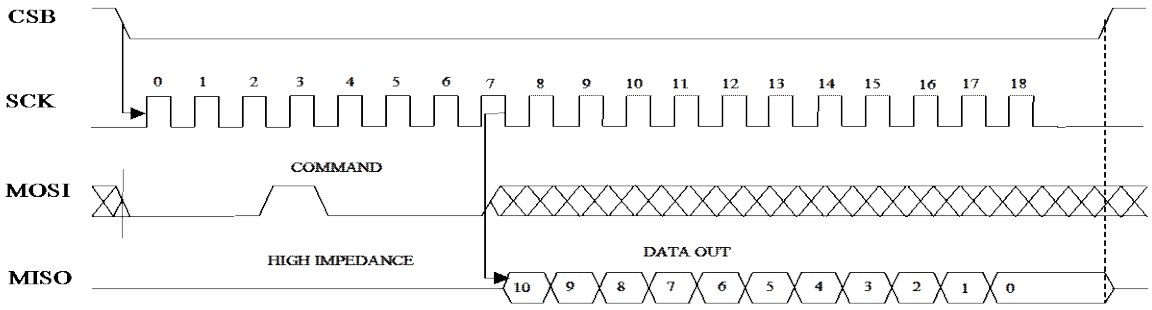


Figure 7. RDAX command and data transmission over the SPI

Read Y-channel acceleration (RDAY): RDAY command provides access to AD converted Y-channel acceleration signal which is stored in acceleration data register Y. During normal operation acceleration data register Y is loaded in every 150 μs and the load operation is disabled whenever the CSB signal is low, hence CSB has to stay high at least 150 μs prior the RDAY command in order to guarantee correct data. Data output is an 11-bit digital word, which is feed out MSB first and LSB last

Detailed information on all SPI commands is presented in document *IC008 Dual Axis Acceleration Sensor ASIC, Digital Specification.*

4 Mechanical specification

	Lead frame material:	Copper
	Plating:	Nickel followed by Gold
	Solderability:	JEDEC standard: JESD22-B102-C
<CC>	Co-planarity error	0.1mm max.

4.1 Dimensions

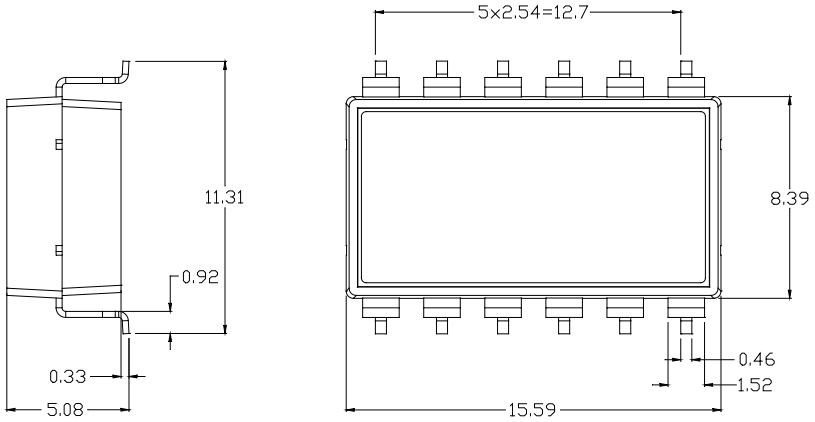
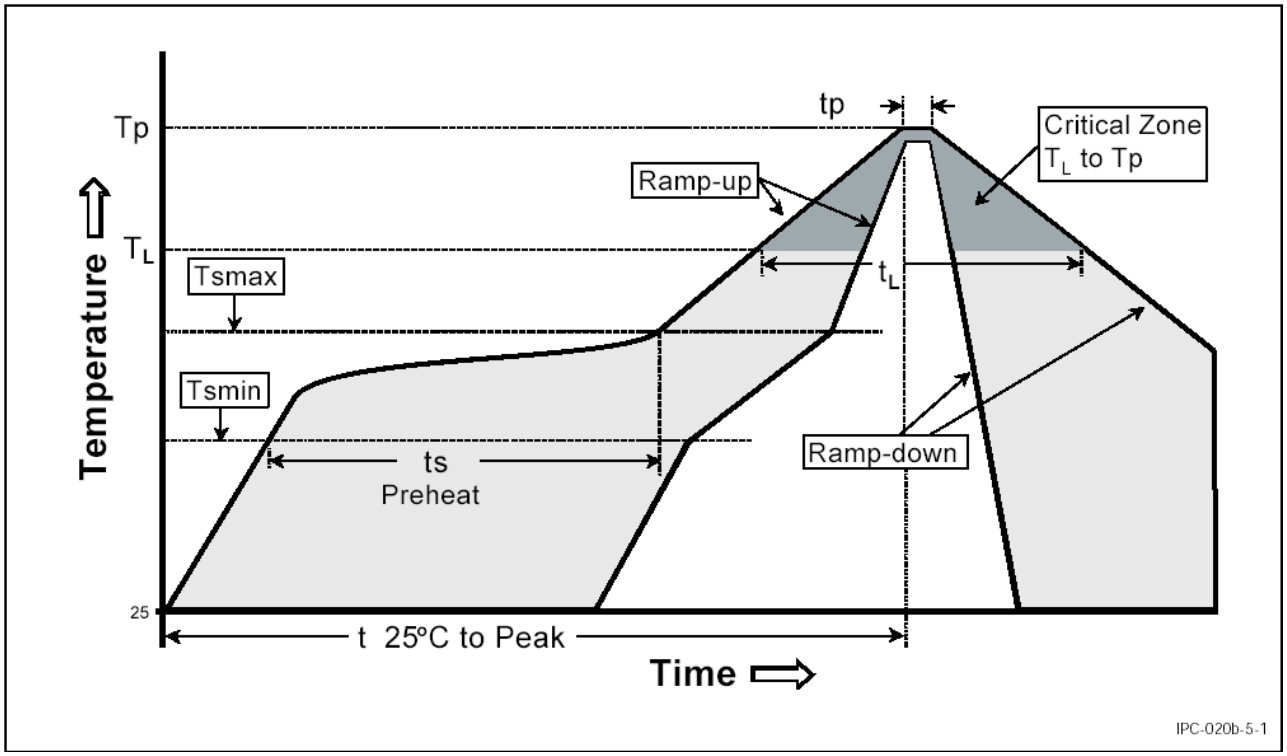


Figure 8. Mechanical dimensions of the SCA1020

5 Mounting

The SCA1020 is suitable for Sn-Pb eutectic and Pb- free soldering process and mounting with normal SMD pick-and-place equipment.

Recommended SCA1020 body temperature profile during reflow soldering:



Profile feature	Sn-Pb Eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature min (T_{smin}) - Temperature max (T_{smax}) - Time (min to max) (ts)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Tsmax to T_L - Ramp up rate		3°C/second max
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak temperature (T_P)	240 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature (T_P)	10-30 seconds	20-40 seconds
Ramp-down rate	6°C/second max	6°C/second max
Time 25° to Peak temperature	6 minutes max	8 minutes max

Figure 9. Recommended SCA1020 body temperature profile during reflow soldering. Ref. IPC/JEDEC J-STD-020B.

Note. Preheating time and temperatures according to solder paste manufacturer.

Component body temperature during the soldering should be measured from the body of the component.

The Moisture Sensitivity Level of the part is 3 according to the IPC/JEDEC J-STD-020B. The part should be delivered in a dry pack. The manufacturing floor time (out of bag) in the customer's end is 168 hours.
Maximum soldering temperature is 250°C/40sec.

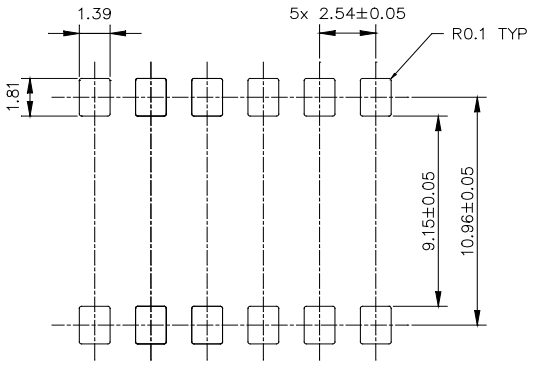


Figure 10. Recommended PCB lay-out

Notes:

- It is important that the part is parallel to the PCB plane and that there is no angular alignment error from intended measuring direction during assembly process.
  - 1° mounting alignment error will increase the cross-axis sensitivity by 1.7%
  - 1° mounting alignment error will change the output by 17mg
- To achieve the highest accuracy and to minimize resonance, it is recommended to glue the accelerometer to the PCB before soldering
- Wave soldering is not recommended.
- A supply voltage by-pass capacitor (>100nF) must be used and located as close as possible to the Vdd and GND pins.
- Note: When the accelerometer is oriented in such a way that the arrow points toward the earth, the output will decrease. Please also note that you can rotate the part around the measuring axis for optimum mounting location.