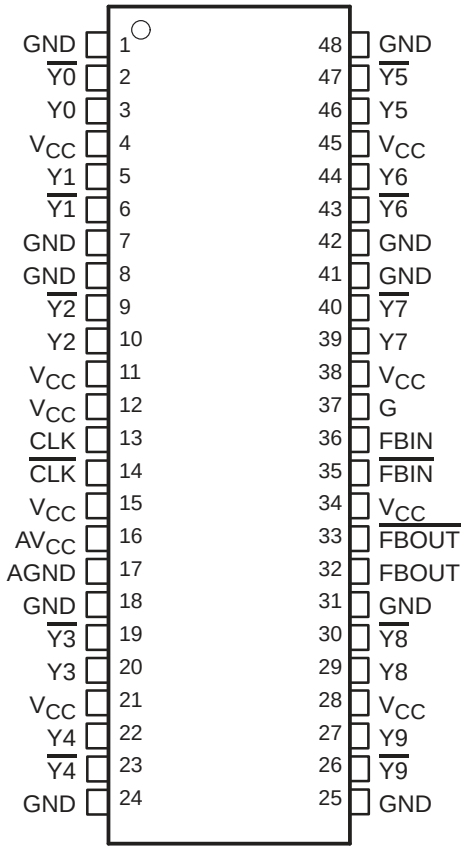
- **Phase-Lock Loop Clock Distribution for Double Data Rate Synchronous DRAM Applications**
- **Distributes One Differential Clock Input to Ten Differential Outputs**
- **External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Clock Input**
- **Operates at $V_{CC}$ = 2.5 V and $AV_{CC}$ = 3.3 V**
- **Packaged in Plastic 48-Pin (DGG) Thin Shrink Small-Outline Package (TSSOP)**
- **Spread Spectrum Clocking Tracking Capability to Reduce EMI**

**DGG PACKAGE**
**(TOP VIEW)**




## description

The CDC857-2 and CDC857-3 are high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. They use a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. The CDC857-3 operates at 3.3 V (PLL) and 2.5 V (output buffer). The CDC857-2 operates at 2.5 V (PLL and output buffer).

One bank of ten inverting and noninverting outputs provide ten low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50%, independent of the duty cycle at CLK.
All outputs can be enabled or disabled via a single output enable input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to high impedance state (3-state).

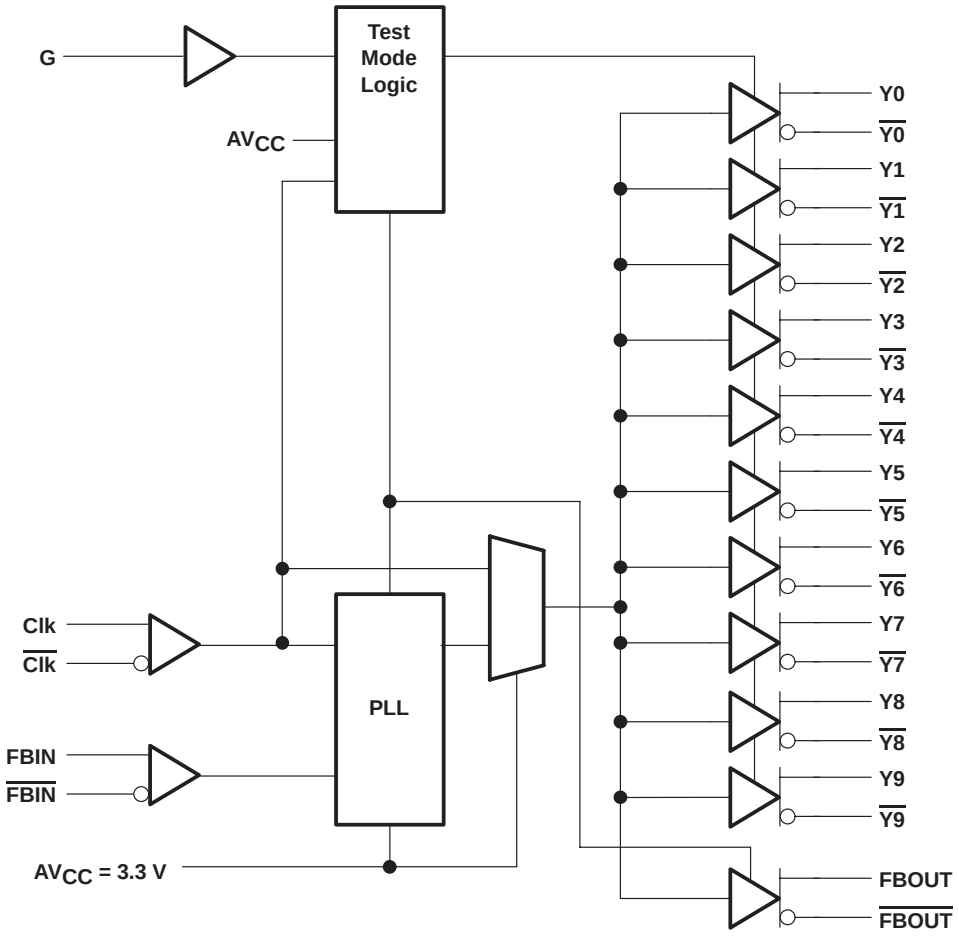
Unlike many products containing PLLs, the CDC857 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuity, the CDC857 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping $AV_{CC}$ to ground. If $AV_{CC}$ is at GND and $V_{CC}$ = ON, 2 falling edges on G cause the PLL to run with FBOUT being enabled and all other outputs being disabled, after $AV_{CC}$ ramps up to its specified $V_{CC}$ value, with G being kept low. The CDC857 is characterized for operation from 0°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | OUTPUTS | | | | PLL |
|---|---|---|---|---|---|---|---|
| G | CLK | $\overline{CLK}$ | Y | $\overline{Y}$ | FBOUT | $\overline{FBOUT}$ | |
| L | X | X | Z | Z | Z | Z | OFF |
| H | L | H | L | H | L | H | RUN |
| H | H | L | H | L | H | L | RUN |
| H | < 20 MHz | < 20 MHz | Z | Z | Z | Z | OFF |

## logic symbol




NOTE A: All outputs are connected to $V_{CC}$ = 2.5 V.

**SPECIAL TEST MODES**

| INPUTS | | | | OUTPUTS | | | | COMMENTS |
|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $AV_{CC}$ | G | CLK† | Y | $\overline{Y}$ | FBOUT | $\overline{FBOUT}$ | |
| ON | 0 V | L | L | Z | Z | Z | Z | Clock Mode |
| ON | 0 V | L | H | Z | Z | Z | Z | Clock Mode |
| ON | 0 V | H | L | L | H | L | H | Clock Mode |
| ON | 0 V | H | H | H | L | H | L | Clock Mode |
| ON | UP‡ | ↓§ | L | Z | Z | L | H | PLL Mode |
| ON | UP‡ | ↓§ | H | Z | Z | H | L | PLL Mode |

† Only one signal shown for this differential input.
‡ $AV_{CC}$ ramped up after two (2) high-to-low transitions on G input & G being low.
§ At least two (2) high-to-low transitions during $AV_{CC}$ = 0.

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AGND | 17 | Ground | Analog ground. AGND provides the ground reference for the analog circuitry. |
| $AV_{CC}$ | 16 | Power | Analog power supply. $AV_{CC}$ provides the power reference for the analog circuitry. In addition, $AV_{CC}$ can be used to bypass the PLL for test purposes. When $AV_{CC}$ is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs. During disable (G = 0), the PLL is powered down. |
| CLK<br>$\overline{CLK}$ | 13<br>14 | I | Clock input, CLK provides the clock signal to be distributed by the CDC857 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal. |
| FBIN<br>$\overline{FBIN}$ | 36<br>35 | I | Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN. |
| FBOUT<br>$\overline{FBOUT}$ | 32<br>33 | O | Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. |
| G | 37 | I | Output bank enable. G is the output enable for outputs Y and $\overline{Y}$. When G is low outputs Y are disabled to a high-impedance state. When G is high, all outputs Y are enabled and switch at the same frequency as CLK. |
| GND | 1, 7, 8, 18, 24, 25, 31, 41, 42, 48 | Ground | Ground |
| $V_{CC}$ | 4, 11, 12, 15, 21, 28, 34, 38, 45 | Power | Power supply |
| Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9 | 3, 5, 10, 20, 22, 46, 44, 39, 29, 27 | O | Clock outputs. These outputs provide low-skew copies of CLK. |
| $\overline{Y0}$, $\overline{Y1}$, $\overline{Y2}$, $\overline{Y3}$, $\overline{Y4}$, $\overline{Y5}$, $\overline{Y6}$, $\overline{Y7}$, $\overline{Y8}$, $\overline{Y9}$ | 2, 6, 9, 19, 23, 47, 43, 40, 30, 26 | O | Clock outputs. These outputs provide low-skew copies of $\overline{CLK}$. |

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ or $AV_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range $V_I$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ +0.5 V
Output voltage range, $V_O$, (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ +0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$ . . . . . ±50 mA
Continuous total output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) . . . . . 89°C/W
Storage temperature range $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 4)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | | 2.3 | | 2.7 | V |
| Analog supply voltage, $AV_{CC}$ | CDC857–2 | | 2.3 | | 2.7 | V |
| | CDC857–3 | | 3 | | 3.6 | V |
| Low–level input voltage, $V_{IL(G)}$ | | G input | | | $0.3 \times V_{CC}$ | V |
| High–level input voltage, $V_{IH(G)}$ | | G input | $0.7 \times V_{CC}$ | | | V |
| DC input signal voltage (see Note 5) | | CLK, FBIN | –0.3 | | $V_{CC}$+0.3 | V |
| Differential input signal voltage, $V_{ID}$ (see Note 6) | dc | CLK, FBIN | 0.35 | | $V_{CC}$+0.6 | V |
| | ac | CLK, FBIN | 0.7 | | $V_{CC}$+0.6 | V |
| Differential cross-point input voltage (see Note 7) | | | $V_{CC}$/2–0.2 | $V_{CC}$/2 | $V_{CC}$/2+0.2 | V |
| High-level output current, $I_{OH}$ | | | | | –12 | mA |
| Low-level output current, $I_{OL}$ | | | | | 12 | mA |
| Input slew rate, SR | | | 1 | | | V/ns |
| Operating free-air temperature, $T_A$ | | | 0 | | 85 | °C |

NOTES: 4. Unused inputs must be held high or low to prevent them from floating.
5. DC input signal voltage specifies the allowable dc execution of differential input.
6. Differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level (see figure 3).
7. Differential cross-point voltage is expected to track variations of $V_{CC}$ and is the voltage at which the differential signals must be crossing.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input voltage | All input pins | $V_{CC}$ = 2.3 V, $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = min to max, $I_{OH}$ = –1 mA | $V_{CC}$–0.1 | | | V |
| | | | $V_{CC}$ = 2.3 V, $I_{OH}$ = –12 mA | 1.7 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = min to max, $I_{OL}$ = 1 mA | | | 0.1 | V |
| | | | $V_{CC}$ = 2.3 V, $I_{OL}$ = 12 mA | | | 0.6 | |
| $I_{OH}$ | High-level output current | | $V_{CC}$ = 2.3 V, $V_O$ = 1 V | –18 | –32 | | mA |
| $I_{OL}$ | Low-level output current | | $V_{CC}$ = 2.3 V, $V_O$ = 1.2 V | 26 | 35 | | mA |
| $V_O$ | Output voltage swing | | For load condition see Figure 3 | 1.1 | | $V_{CC}$–0.4 | V |
| $I_I$ | Input current | G | $V_{CC}$ = 2.7 V, $V_I$ = 0 V to 2.7 V | | | ±10 | µA |
| | | CLK, FBIN | $V_{CC}$ = 2.7 V, $V_I$ = 0 V to 2.7 V | | | ±10 | |
| $I_{OZ}$ | High-impedance output current | | $V_{CC}$ = 2.7 V, $V_O$ = $V_{CC}$ or GND | | | ±10 | µA |
| $V_{OC}$ | Output crossing point voltage‡ | | | ($V_{CC}$/2)– 0.1 | $V_{CC}$/2 | ($V_{CC}$/2)+ 0.1 | V |
| $I_{CCZ}$ | Supply current, disabled | | $AV_{CC}$ and $V_{CC}$ = max, G = L or no input CLK signal | | 500 | 800 | µA |
| $I_{CC}$ | Supply current on $V_{CC}$ (see Figure 7) | | $V_{CC}$ = 2.7 V, $f_O$ = 167 MHz, All outputs switching 16 pF in 60 Ω environment, See Figure 3 | | 235 | 300 | mA |
| $AI_{CC}$ | Supply current on $AV_{CC}$ | CDC857–2 | $AV_{CC}$ = 2.7 V, $f_O$ = 167 MHz | | 9 | 12 | mA |
| | | CDC857–3 | $AV_{CC}$ = 3.6 V, $f_O$ = 167 MHz | | 15 | 19 | |
| $C_I$ | Input capacitance | | $V_{CC}$ = 2.5 V, $V_I$ = $V_{CC}$ or GND | | 2 | | pF |
| $C_O$ | Output capacitance | | $V_{CC}$ = 2.5 V, $V_O$ = $V_{CC}$ or GND | | 3 | | pF |

† All typical values are at respective nominal $V_{CC}$.

‡ The value of $V_{OC}$ is expected to be |VTR + VCP|/2. In case of each clock directly terminated by a 120-Ω resistor, where VTR is the true input signal voltage and VCP is the complementary input signal voltage (see Figure 3).

## timing requirements over recommended ranges or supply voltage and operating free–air temperature

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_C$ | Clock frequency | | 66 | 167 | MHz |
| | Input clock duty cycle | | 40% | 60% | |
| | Stabilization time† | | | 0.1 | ms |

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed–frequency, fixed–phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

## switching characteristics

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$‡ | Low–to high level propagation delay time (see Figure 5) | CLK mode/CLK to any output | 1.5 | 3.5 | 6 | ns |
| $t_{PHL}$‡ | High–to low level propagation delay time (see Figure 5) | CLK mode/CLK to any output | 1.5 | 3.5 | 6 | ns |
| $t_{en}$ | Output enable time | CLK mode/G to any Y output | | 3 | | ns |
| $t_{dis}$ | Output disable time | CLK mode/G to any Y output | | 3 | | ns |
| $t_{(jitter)}$ | Jitter (peak-to–peak) | 66 MHz | | | 120 | ps |
| | | 100/125/133/167 MHz | | | 75 | |
| $t_{(jitter)}$ | Jitter (cycle-to-cycle) | 66 MHz | | | 110 | ps |
| | | 100/125/133/167 MHz | | | 65 | |
| $t_{(phase\ error)}$ | Phase error (see Figure 4) | All differential input and output terminals are terminated with 120 Ω/ 16 pF as shown in Figure 2 | –150 | | 150 | ps |
| $t_{skew(0)}$ | Output skew (see Figure 4) | | | | 100 | ps |
| $t_{skew(p)}$ | Pulse skew | | | | 100 | ps |
| | Duty cycle§ (see Figure 6) | 66 MHz to 100 MHz | 49.5% | | 50.5% | |
| | | 101 MHz to 167 MHz | 49% | | 51% | |
| $t_r$, $t_f$ | Output rise and fall times (20% – 80%) | Load = 120 Ω/16 pF | 650 | 800 | 950 | ps |

‡ Refers to transition of noninverting output.

§ While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = $t_{wH}/t_c$, were the cycle time ($t_c$) decreases as the frequency goes up.

## APPLICATION EXAMPLE

**Table 1. Clock Structure and SDRAM Loads per Clock**

| CLOCK STRUCTURE | NUMBER of SDRAM LOADS PER CLOCK | CAPACITIVE LOADING ON THE PLL OUTPUTS (pF) | |
|---|---|---|---|
| | | MIN | MAX |
| 1 | 2 | 5 | 8 |
| 2 | 4 | 10 | 16 |

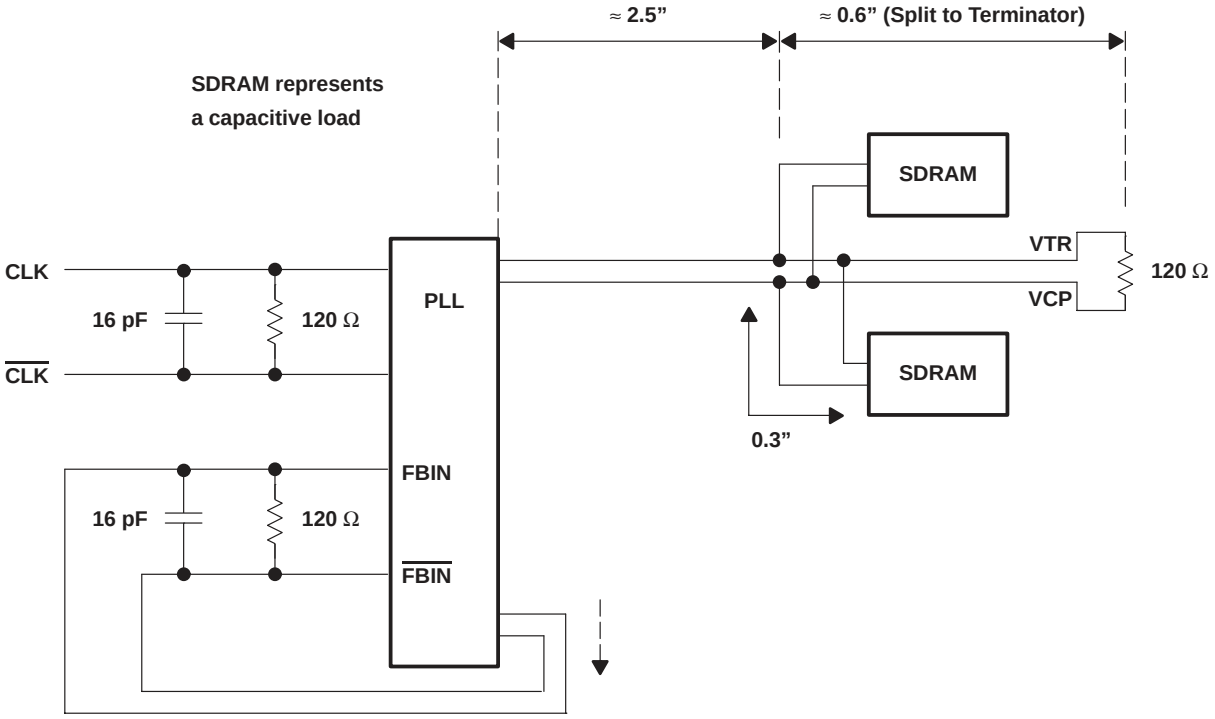



**Figure 1. Clock Structure #1**

## APPLICATION EXAMPLE

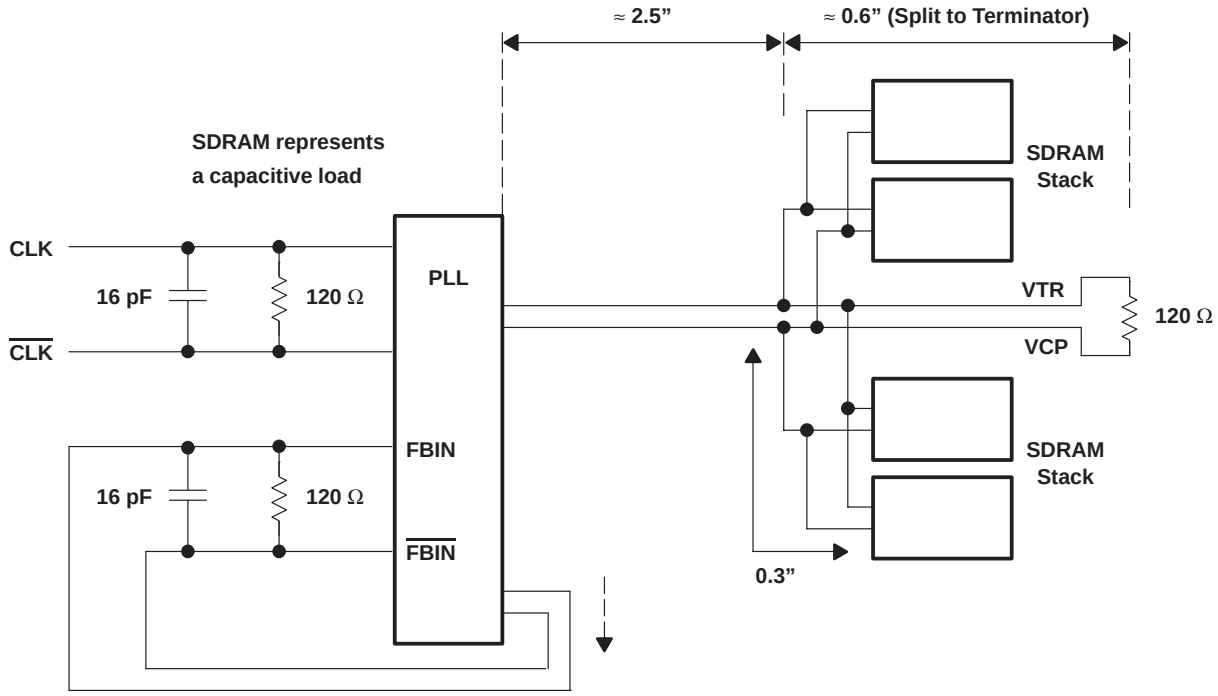



**Figure 2. Clock Structure #2**

### differential clock signals

Figure 3 shows the differential clocks are directly terminated by a 120-Ω resistor.

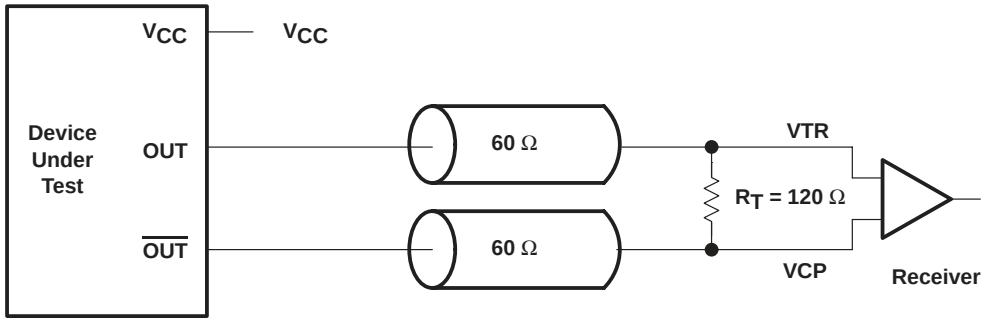



**Figure 3. Differential Signal Using Direct Termination Resistor**

## PARAMETER MEASUREMENT INFORMATION

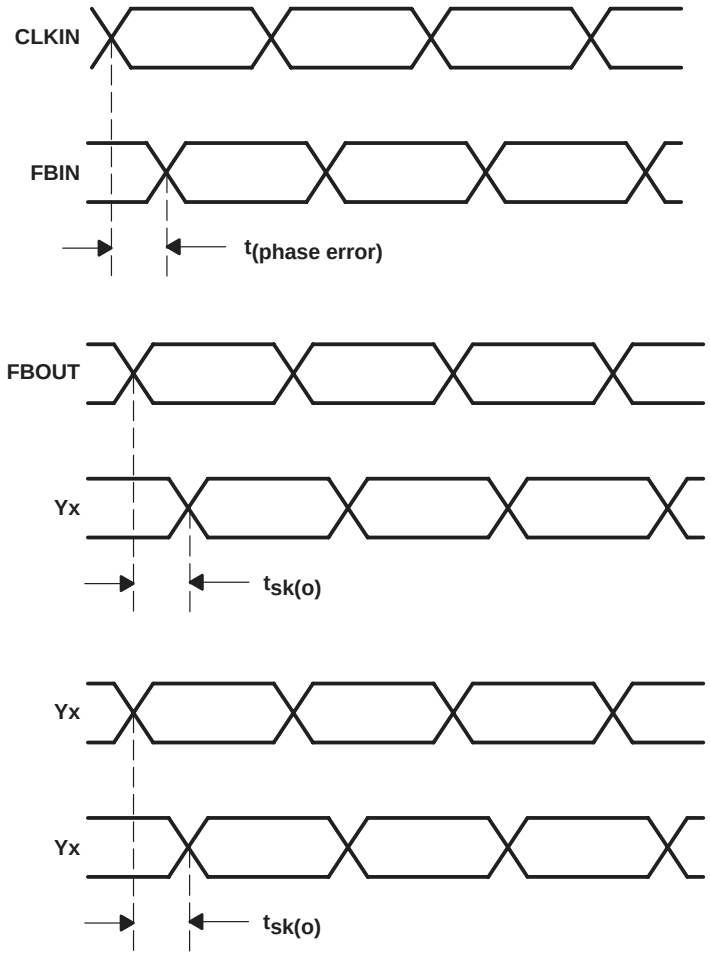



**Figure 4. Phase Error and Skew Waveforms**

## PARAMETER MEASUREMENT INFORMATION

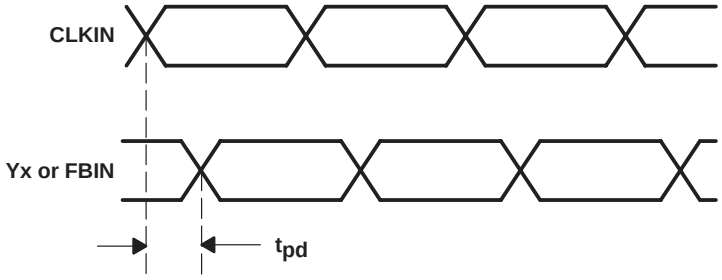
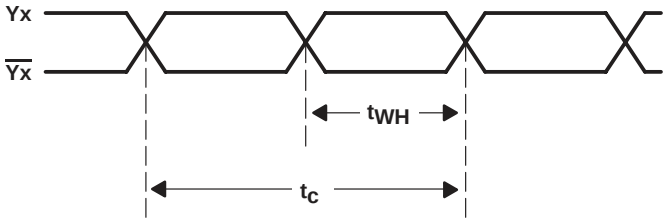
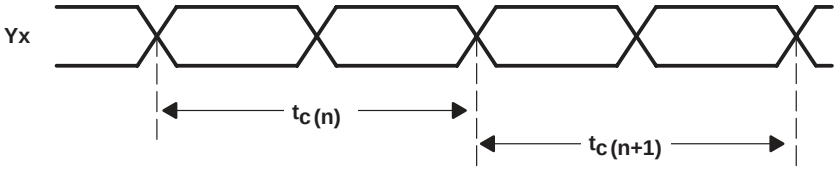



**Figure 5. Propagation Delay Time; $t_{PLH}$, $t_{PHL}$**




NOTE A: Duty cycle = $t_{WH}/t_c$

**Figure 6. Output Duty Cycle**



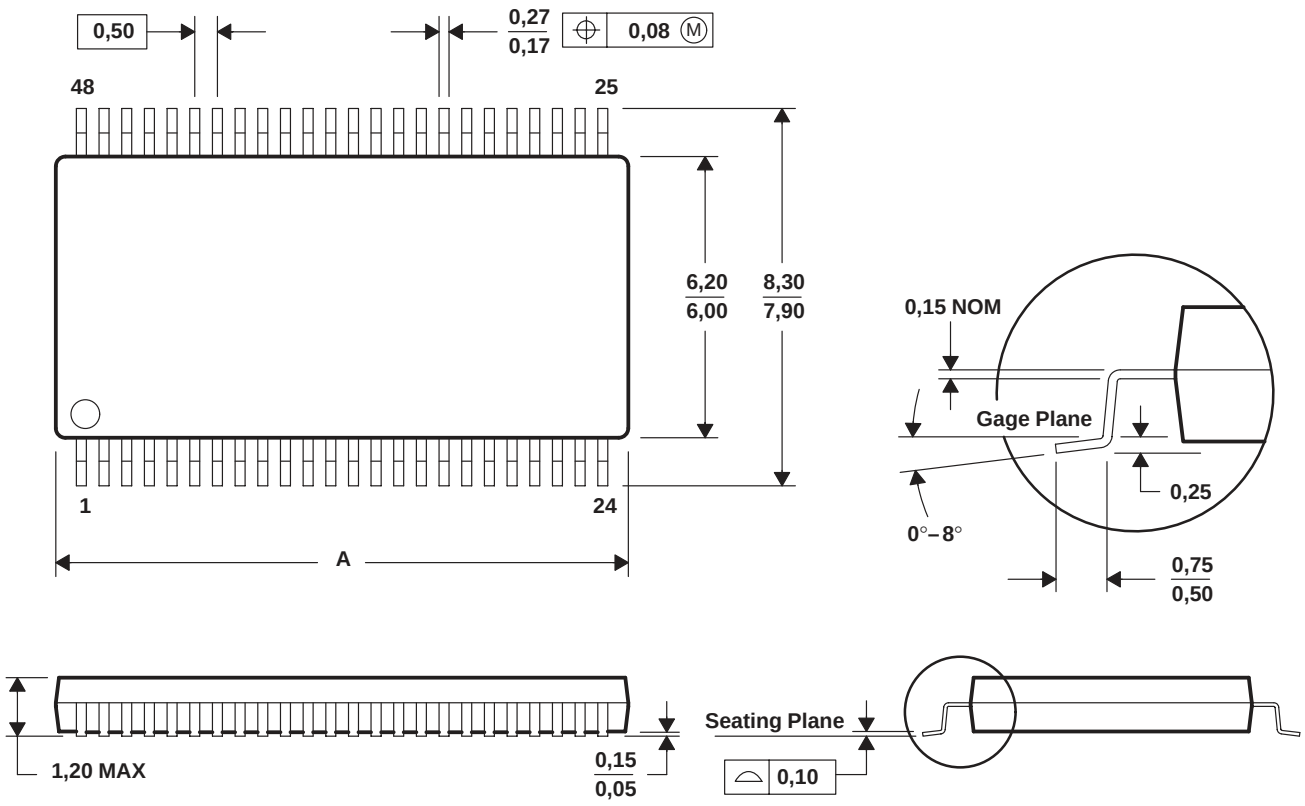

NOTE A: Cycle-to-cycle jitter = $|t_{c(n)} - t_{c(n+1)}|$ over 2000 consecutive cycles.

**Figure 7. Cycle-to-Cycle Jitter**

## MECHANICAL DATA

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PIN SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

**4040078/F 12/97**

NOTES: B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold protrusion not to exceed 0,15.
E. Falls within JEDEC MO-153

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