User's Guide

BUF802RGTEVM User's Guide

ABSTRACT

This user's guide describes the characteristics, operation, and use of the BUF802RGTEVM. This evaluation module (EVM) is an evaluation and development kit for the BUF802 wide-bandwidth, low noise, JFET input buffer. A circuit description, schematic diagram, layout prints, and bill of materials are included in this document.

Throughout this document, the abbreviation EVM and the term evaluation module are synonymous with the BUF802RGTEVM.

See BUF802 Wide-Bandwidth, 2.3 nV/√Hz, JFET Input Buffer for more information on the device.

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Trademarks

1 Introduction

The BUF802RGTEVM is designed to easily demonstrate the functionality and versatility of the buffer. The EVM features two separate circuit configurations: a composite loop with a precision amplifier and a standalone BUF802 circuit. It can be used with split or single supplies, andand includes SMA connectors on analog inputs and outputs for easy operation. The layout is optimized to reduce parasitic coupling and provide the best signal fidelity across frequency.

- Includes standalone device circuit and composite loop with precision amplifier
- Potentiometer to trim offset of low frequency composite path
- Layout configured to minimize parasitic coupling
- Easy to use SMA connectors for all input and output signals

2 Configuration and Usage

The BUF802RGTEVM includes a configuration as a standalone buffer (bottom half of board) and a composite loop with a precision amplifier (top half of board). Each ciruict configuration features their own indpendent power supply and signal connections to avoid any potential interference between the two circuits. Default component values are included in the Figure 8-2 section, but may be altered as desired by the user.

3 Power Connections

The BUF802RGTEVM is built for default split-supply configurations, but can also be used with a single supply if all common mode inputs are kept within proper ranges. Both circuits feature banana plug connections for V_{CC}, Ground, and V_{EE}. By default each circuit is populated with high quality decoupling capacitors to ensure adiquate high frequency supply decoupling to improve performance and avoid instabilities.

4 Input and Output Connections

The BUF802RGTEVM board includes SMA connectors on the signal input and outputs for each circuit configuration. The input and output traces are matched for 50-Ω characteristic impedance to easily interface with standard test equipment.

5 Stand-Alone Buffer Configuration

The bottom half of the board features the BUF802 in a standalone circuit configuration. This circuit is very similar to the one used to generate AC performance data in the BUF802 datasheet. In this configuration the BUF802 acts as a simple AC coupled buffer with a 50-Ω input impednace created by R29. With the input AC coupled, the test point T9 MUST be bonnected to a DC bias voltage for the circuit to function properly. The voltage on T9 sets the bias to the input stage of the BUF802 and should be set within the input common mode range of the device. To DC couple the input, the capacitor C44 can be replaced with a zero Ohm resistor and then the DC portion of the input signal will provide the bias to the input of the amplifier and the connection to T9 is no longer needed.

The output of the circuit features a resistor network (R24, R25, R27) that presents a 100-Ω load to the BUF802 while providing a 50-Ω impednace match for connecting to test equipment. This matching network creates an attenuation of approximately 0.27 V/V that should be accounted for when making measurements.

6 Composite Loop Configuration

The BUF802 device can be configured multiple ways in composite loops with a precision amplifier to handle low frequency high accuracy signals. The top board of the BUF802RGTEVM features the device in composite mode *CL Mode* configuration as referenced in BUF802 Wide-Bandwidth, 2.3 nV/√Hz, JFET Input Buffer. In this configuration, the precision amplifier (U2) handles the low frequency signals in the circuit and then the BUF802 takes over for high frequency signals. The poteniometer R16 or an optional DAC input on J3 can be used to adjust the gain matching between the low frequency and high frequency paths. By default R16 is not configured for ideal matching and the user should adjust the potentiometer for a flat transition between low and high frequency gains. For more detailed information on configuring the device for *CL Mode* operation, please refer to the BUF802 Wide-Bandwidth, 2.3 nV/√Hz, JFET Input Buffer.

7 External Clamping

The BUF802RGTEVM composite loop circuit also includes footprints for optional clamping diodes D1 and D2. These diodes are attached to the CLH and CLL pins, which are then connected to the supplies through series resistors R1 and R2 respectively. These diodes can be populated in cases where the 100 mA current rating of the internal diode clamps is insufficient. When using external clamping, disable the BUF802's internal protection by connecting CLH and CLL to the positive and negative supply respectively.

8 Schematic

Figure 8-1 and Figure 8-2 show the BUF802RGTEVM schematic with the default device population for both circuits.

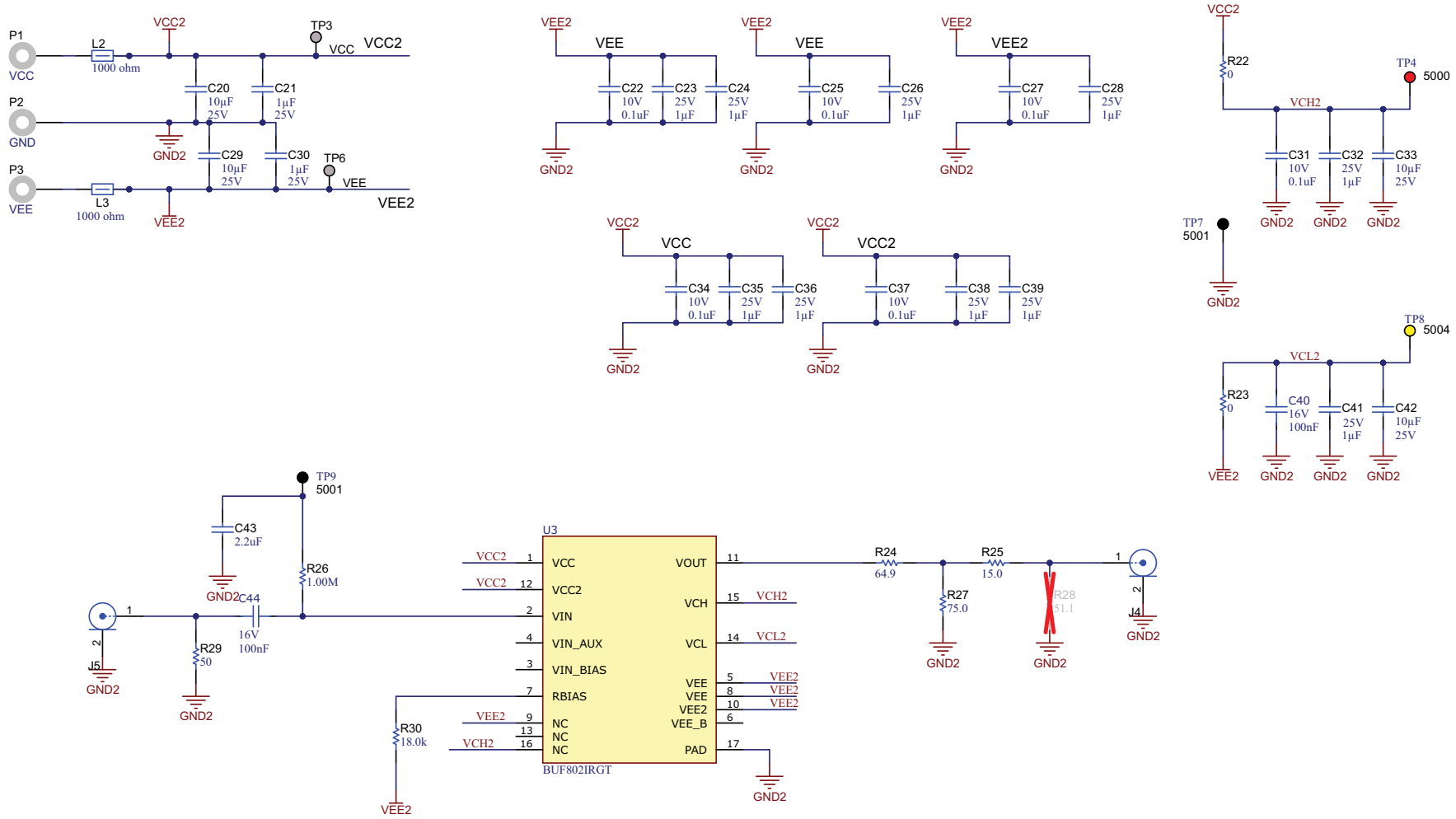

Figure 8-1. BUF802RGTEVM Standalone Configuration Schematic

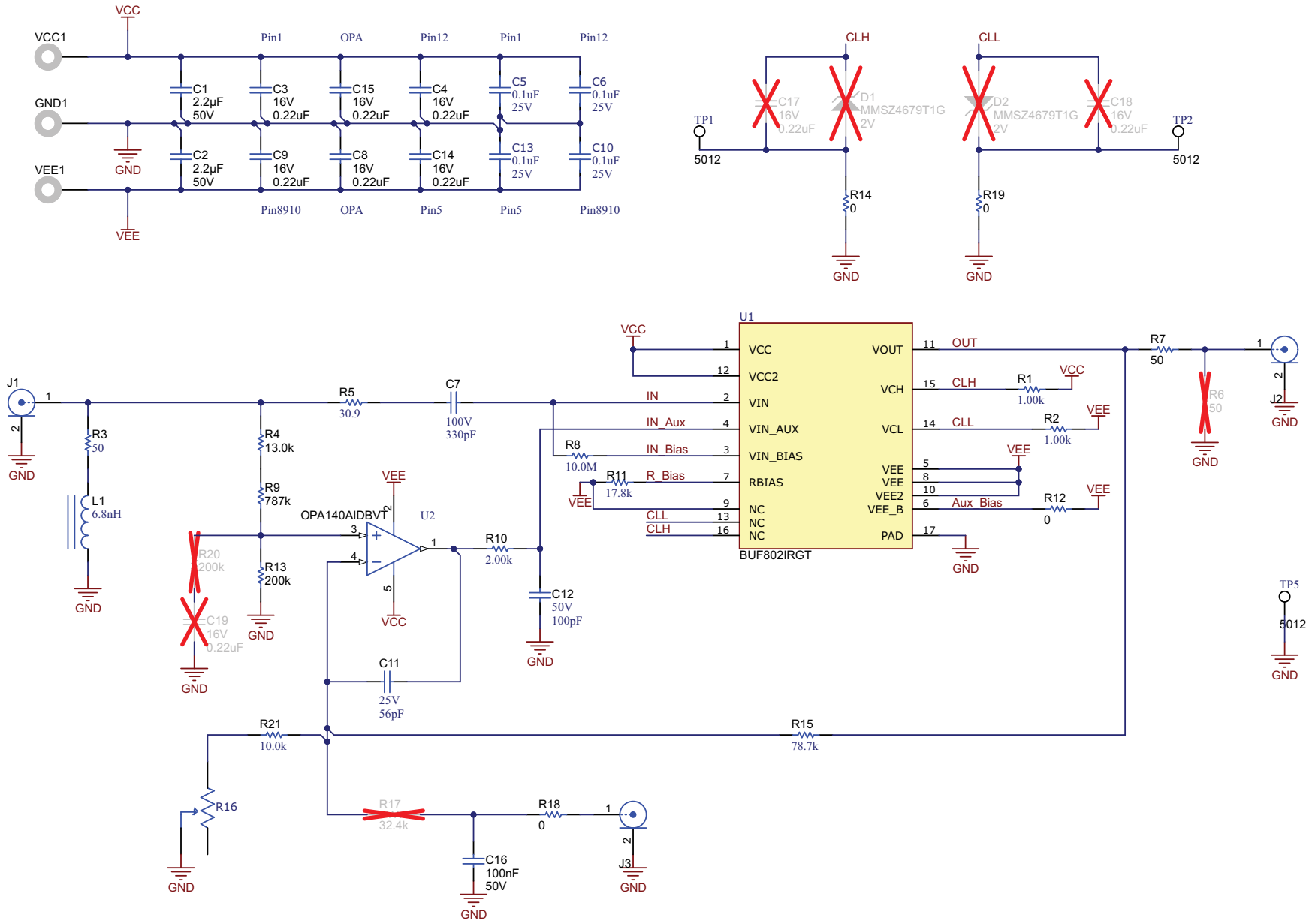

Figure 8-2. BUF802RGTEVM Composite Configuration Schematic

9 Layout Prints

Figure 9-1 through Figure 9-8 show the PCB layers for the BUF802RGTEVM standalone circuit and composite circuit respectively.

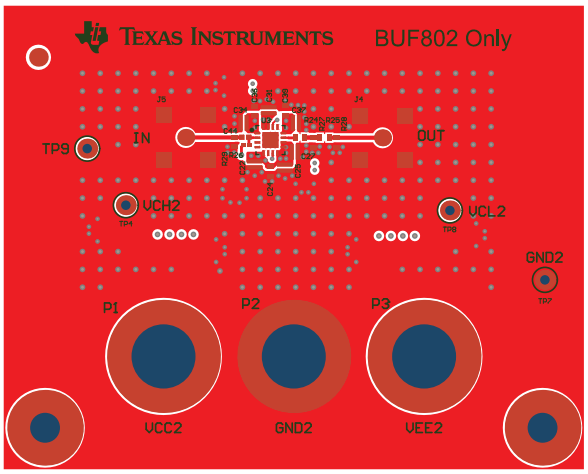

Figure 9-1. Standalone Configuration Top Layers

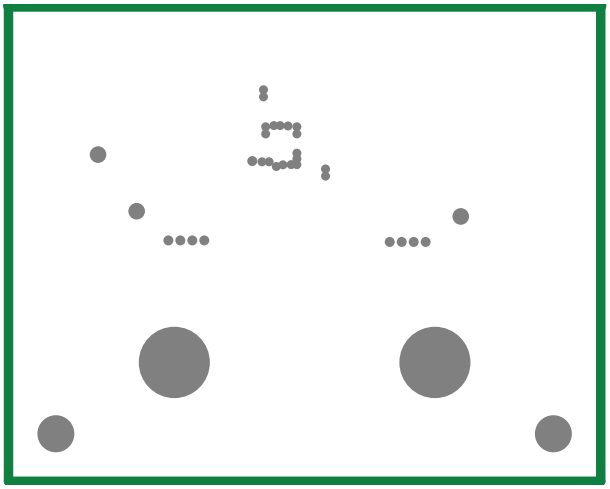

Figure 9-2. Standalone Configuration Ground Layer

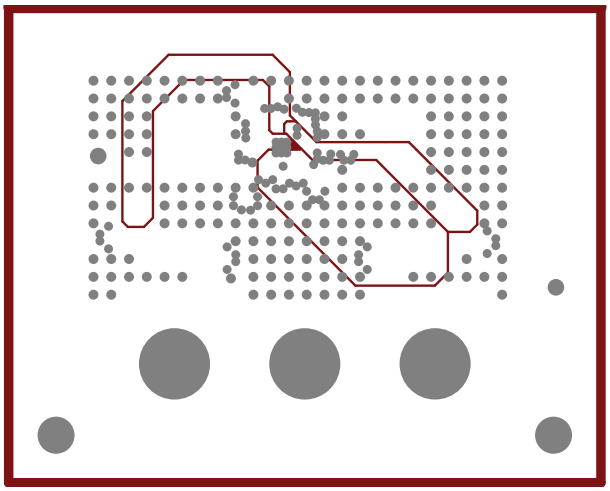

Figure 9-3. Standalone Configuration Power Layer

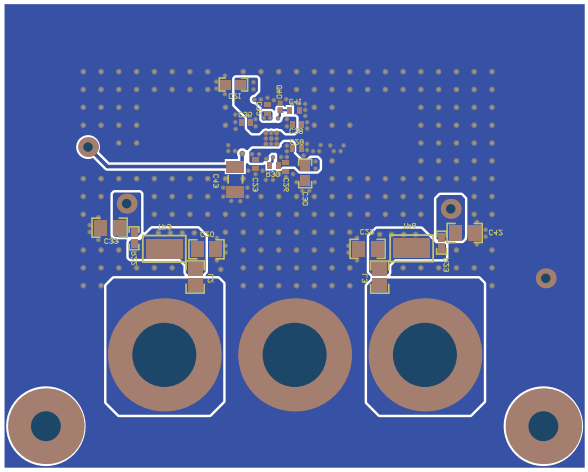

Figure 9-4. Standalone Configuration Bottom Layers

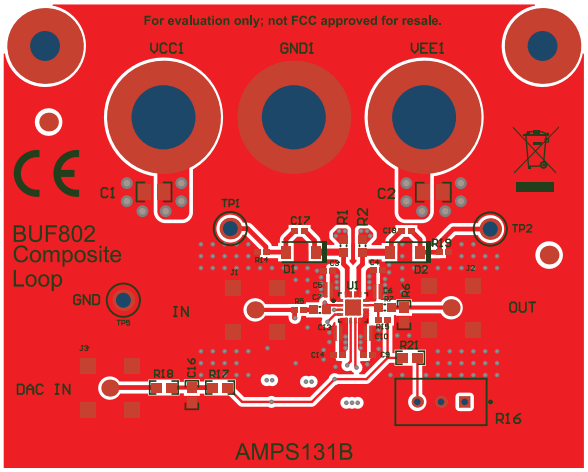

Figure 9-5. Composite Configuration Top Layers

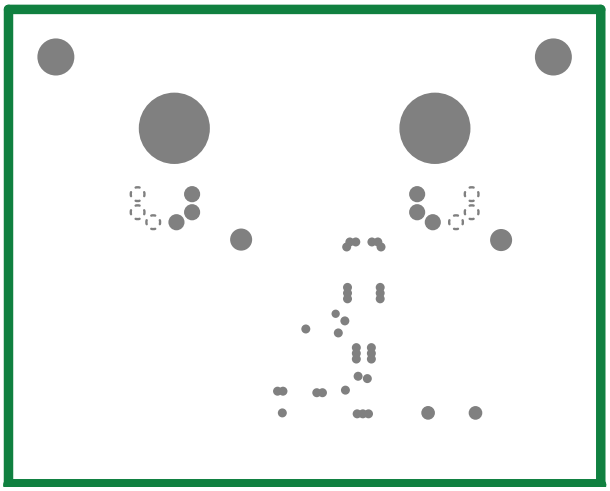

Figure 9-6. Composite Configuration Ground Layer

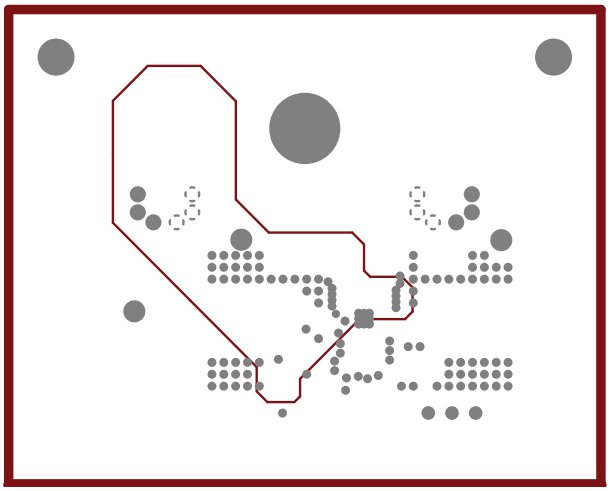

Figure 9-7. Composite Configuration Power Layer

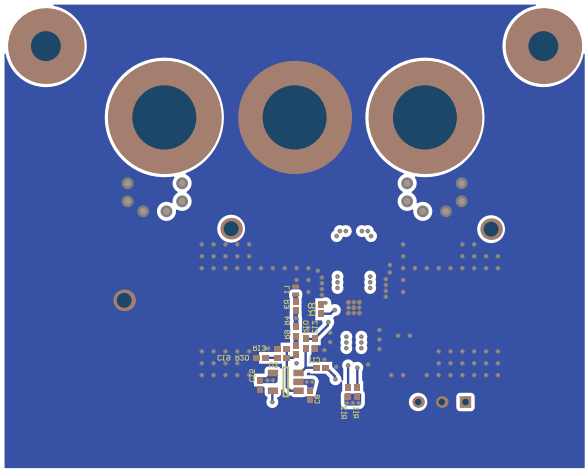

Figure 9-8. Composite Configuration Bottom Layers

10 Related Documentation

- *BUF802 Wide-Bandwidth, 2.3 nV/√Hz, JFET Input Buffer* data sheets

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2021) to Revision A (February 2022)	Page
• Updated the *Introduction* section through *External Clamping* section	2
• Added the *BUF802RGTEVM Standalone Configuration Schematic*	4
• Updated the *Layouts* in the *Layout Prints* section	6

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