Low Capacitance, +12 V / +5 V / +3 V, Triple SPDT (Triple 2:1) Analog Switch / Multiplexer

DESCRIPTION

The DG9454E is a high precision triple SPDT (triple 2:1) analog switch / multiplexer with enhanced performance on low power consumption. The part features low parasitic capacitance, low leakage, and low charge injection over the full signal range which make it an ideal switch for healthcare, data acquisition, and instrument products. Its compact size, light weight, low power consumption, and low voltage control capability are of advantages in portable consumer applications such as goggles.

The DG9454E is designed to operate from a 3 V to 16 V supply at V+, and 2.5 V to 5.5 V at V_L, while guarantees 1.8 V logic compatible over the full operation voltage range.

Processed with advanced CMOS technology, the DG9454E conducts equally well in both directions, offers rail to rail analog signal handling and can be used both as a multiplexer as well as a de-multiplexer.

The DG9454E operating temperature is specified from -40 °C to +125 °C. It is available in ultra-compact 1.8 mm x 2.6 mm miniQFN16 package of lead (Pb)-free nickel-palladium-gold device termination. It is represented by the lead (Pb)-free "-E4" suffix. The nickel-palladium-gold device terminations meet all JEDEC® standards for reflow and MSL ratings.

FEATURES

- Operates with V+ = 3 V to 16 V, V_L = 2.5 V to 5.5 V
- Guaranteed 1.8 V logic control at full V+ range
- Low power consumption, both I+ and I_L < 1 µA
- Low parasitic capacitance:
  $C_{D(ON)}$: 8.8 pF
  $C_{D(OFF)}$: 4 pF
  $C_{S(OFF)}$: 3.1 pF
- High bandwidth: 356 MHz
- Low charge injection over the full signal range
- Compact miniQFN16 package (1.8 mm x 2.6 mm x 0.55 mm)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

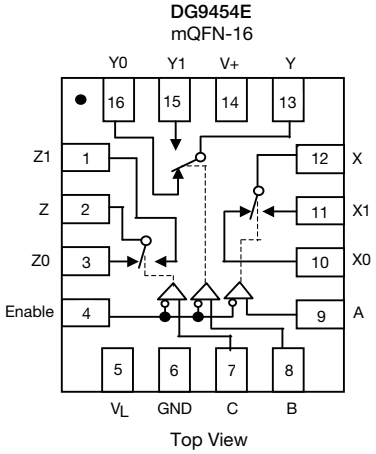
APPLICATIONS

- Medical and healthcare systems
- Data acquisition systems
- Meters and instruments
- Games and Goggles
- Automatic test equipment
- Process control and automation
- Communication systems
- Battery powered systems

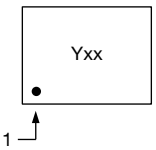
BENEFITS

- Low power consumption
- Precision switching
- Low voltage logic interface
- Bi-directional rail to rail signal switching
- Compact package option
- Extended operation temperature range

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View



Device Marking: Jxx for DG9454E (miniQFN16)

xx = Date/Lot Traceability Code

TRUTH TABLE

ENABLE INPUT	SELECT INPUTS			ON SWITCHES
	C	B	A	DG9454E
H	X	X	X	All Switches Open
L	L	L	L	X to X0, Y to Y0, Z to Z0
L	L	L	H	X to X1, Y to Y0, Z to Z0
L	L	H	L	X to X0, Y to Y1, Z to Z0
L	L	H	H	X to X1, Y to Y1, Z to Z0
L	H	L	L	X to X0, Y to Y0, Z to Z1
L	H	L	H	X to X1, Y to Y0, Z to Z1
L	H	H	L	X to X0, Y to Y1, Z to Z1
L	H	H	H	X to X1, Y to Y1, Z to Z1

ORDERING INFORMATION

TEMP. RANGE	PACKAGE	PART NUMBER	MIN. ORDER / PACK. QUANTITY
-40 °C to +85 °C lead (Pb)-free	16-Pin miniQFN	DG9454EEN-T1-GE4	Tape and reel, 3000 units

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		LIMIT	UNIT
Digital Inputs [a], V_S, V_D, V_L		GND - 0.3 to (V+) + 0.3 or 30 mA, whichever occurs first	V
V+ to GND		-0.3 to +18	
Continuous Current (any terminal)		30	mA
Peak Current, S or D (pulsed 1 ms, 10 % duty cycle)		100	
Storage Temperature		-65 to +150	°C
Power Dissipation [b]	16-Pin miniQFN [c, d]	525	mW
Thermal Resistance [b]	16-Pin miniQFN [d]	152	°C/W
Latch-Up (per JESD78)		100	mA
ESD Human Body Model (HBM); per ANSI / ESDA / JEDEC JS-001		2500	V

Notes

a. Signals on SX, DX, V_L or INX exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.6 mW/°C above 70 °C.
d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS FOR UNIPOLAR SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, V_L = 2.7 V $V_{IN(A, B, C \text{ and enable})}$ = 1.8 V, 0.5 V [a]	TEMP.[b]	TYP.[c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN.[d]	MAX.[d]	MIN.[d]	MAX.[d]	
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	0	12	0	12	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = 0.7 V, 6 V, 11.3 V	Room	85	-	103	-	103	Ω
			Full	-	-	133	-	125	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = 0.7 V, 11.3 V	Room	1.24	-	8	-	8	
			Full	-	-	8	-	8	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = 0.7 V, 6 V, 11.3 V	Room	27	-	37	-	37	
			Full	-	-	44	-	43	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 13.2 V, V_L = 2.7 V V_D = 1 V / 12.2 V, V_S = 12.2 V / 1 V	Room	± 0.05	-1	1	-1	1	nA
			Full	-	-50	50	-5	5	
	$I_{D(off)}$		Room	± 0.07	-1	1	-1	1	
			Full	-	-50	50	-5	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 13.2 V, V_L = 2.7 V V_D = V_S = 1 V / 12.2 V	Room	± 0.07	-1	1	-1	1	
			Full	-	-50	50	-5	5	
Digital Control									
Logic Low Input Voltage	V_{INL}	V_L = 2.7 V	Full	-	-	0.5	-	0.5	V
Logic High Input Voltage	V_{INH}		Full	-	1.8	-	1.8	-	
Logic Low Input Current	I_L	$V_{IN(A0, A1, A2 \text{ and enable})}$ under test = 0.5 V	Full	0.02	-1	1	-1	1	µA
Logic High Input current	I_H	$V_{IN(A0, A1, A2 \text{ and enable})}$ under test = 1.8 V	Full	0.02	-1	1	-1	1	
Dynamic Characteristics									
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see Fig. 1, 2, 3	Room	79	-	119	-	119	ns
			Full	-	-	134	-	126	
Enable Turn-On Time	$t_{ON(EN)}$		Room	70	-	110	-	110	
			Full	-	-	130	-	116	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	51	-	91	-	91	
			Full	-	-	95	-	94	
Break-Before-Make Time Delay	t_D		Room	17	-	-	-	-	
			Full	-	1	-	1	-	
Charge Injection [e]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Full	5.84	-	-	-	-	pC
Off Isolation [e]	OIRR	f = 1 MHz, R_L = 50 Ω, C_L = 5 pF 100 kHz	Room	-95	-	-	-	-	dB
		1 MHz	Room	-85	-	-	-	-	
		10 MHz	Room	-65	-	-	-	-	
Crosstalk [e]	X_{TALK}	100 kHz	Room	-92	-	-	-	-	
		1 MHz	Room	-73	-	-	-	-	
		10 MHz	Room	-53	-	-	-	-	
Bandwidth, -3 dB [e]	BW	R_L = 50 Ω	Room	356	-	-	-	-	MHz
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	3.1	-	-	-	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$		Room	4	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$		Room	8.8	-	-	-	-	
Total Harmonic Distortion [e]	THD	Signal = 1 V_{RMS}, 20 Hz to 20 kHz, R_L = 600 Ω	Room	0.075	-	-	-	-	%

SPECIFICATIONS FOR UNIPOLAR SUPPLIES									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, V_L = 2.7 V $V_{IN(A, B, C \text{ and enable})}$ = 1.8 V, 0.5 V [a]	TEMP.[b]	TYP.[c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN.[d]	MAX.[d]	MIN.[d]	MAX.[d]	
Power Supply									
Power Supply Range	I+	$V_{IN(A, B, C \text{ and enable})}$ = 0 V or 12 V	Room	0.05	-	1	-	1	µA
			Full	-	-	10	-	10	
Ground Current	I_{GND}		Room	0.05	-1	-	-1	-	
			Full	-	-10	-	-10	-	
Logic Supply Current	I_L	V_L = 2.7 V	Room	0.05	-	1	-	1	
			Full	-	-	10	-	10	

Notes

a. V_{IN} = input voltage to perform proper function.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.

SPECIFICATIONS FOR UNIPOLAR SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V_L = 2.7 V, $V_{IN(A, B, C \text{ and enable})}$ = 1.8 V, 0.5 V [a]	TEMP. [b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	0	5	0	5	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = 0 V, 3.5 V	Room	125	-	147	-	147	Ω
			Full	-	-	176	-	168	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = 3.5 V	Room	1.33	-	8	-	8	
			Full	-	-	8	-	8	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = 0 V, 3 V	Room	21	-	31	-	31	
			Full	-	-	25	-	29	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 5.5 V, V- = 0 V, V_D = 1 V / 4.5 V, V_S = 4.5 V / 1 V	Room	± 0.03	-1	1	-1	1	nA
			Full	-	-50	50	-5	5	
	$I_{D(off)}$		Room	± 0.03	-1	1	-1	1	
			Full	-	-50	50	-5	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 5.5 V, V- = 0 V, V_D = V_S = 1 V / 4.5 V	Room	± 0.03	-1	1	-1	1	
			Full	-	-50	50	-5	5	
Digital Control									
$V_{IN(A, B, C \text{ and enable})}$ Low	V_{IL}	V_L = 2.7 V	Full	-	-	0.6	-	0.6	V
$V_{IN(A, B, C \text{ and enable})}$ High	V_{IH}	V_L = 2.7 V	Full	-	1.8	-	1.8	-	
Input Current, V_{IN} Low	I_L	$V_{IN(A, B, C \text{ and enable})}$ under test = 0.6 V	Full	0.02	-1	1	-1	1	µA
Input Current, V_{IN} High	I_H	$V_{IN(A, B, C \text{ and enable})}$ under test = 1.8 V	Full	0.02	-1	1	-1	1	
Dynamic Characteristics									
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF, see Fig. 1, 2, 3	Room	95	-	135	-	135	ns
			Full	-	-	164	-	152	
Enable Turn-On Time	t_{ON}		Room	80	-	120	-	120	
			Full	-	-	138	-	129	
Enable Turn-Off Time	t_{OFF}		Room	58	-	98	-	98	
			Full	-	-	106	-	103	
Break-Before-Make Time Delay	t_D		Room	45	-	-	-	-	
			Full	-	24	-	15	-	
Charge Injection [e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Full	1.44	-	-	-	-	pC
Off Isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz	Room	-95	-	-	-	-	dB
Channel-to-Channel Crosstalk [e]	X_{TALK}		Room	-92	-	-	-	-	
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	3.5	-	-	-	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$		Room	4.5	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$		Room	10.2	-	-	-	-	
Power Supply									
Power Supply Current	I+	$V_{IN(A, B, C \text{ and enable})}$ = 0 V or 5 V	Room	0.05	-	1	-	1	µA
			Full	-	-	10	-	10	
Ground Current	I_{GND}		Room	-0.05	-1	-	-1	-	
			Full	-	-10	-	-10	-	
Logic Supply Current	I_L	V_L = 2.7 V	Room	0.05	-	1	-	1	
			Full	-	-	10	-	10	

Notes

a. V_{IN} = input voltage to perform proper function.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.

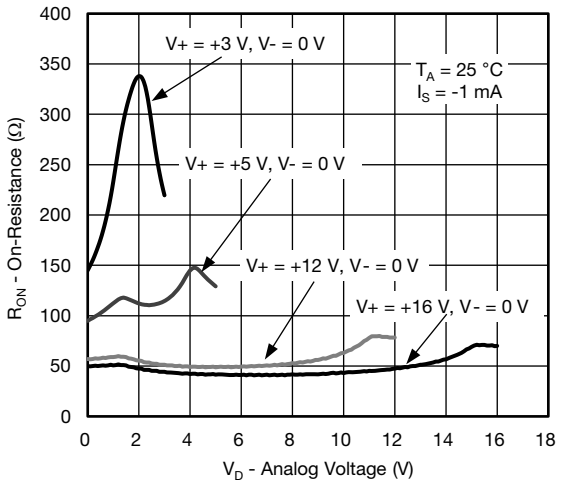
SPECIFICATIONS FOR UNIPOLAR SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, V_L = 2.7 V $V_{IN(A, B, C AND ENABLE)}$ = 1.5 V, 0.6 V [a]	TEMP. [b]	TYP. [c]	-40 °C to +125 °C MIN. [d]	-40 °C to +125 °C MAX. [d]	-40 °C to +85 °C MIN. [d]	-40 °C to +85 °C MAX. [d]	UNIT
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	0	3	0	3	V
On-Resistance	R_{ON}	I_S = 1 mA, V_D = 1.5 V	Room	221	-	-	-	-	Ω
			Full	-	-	-	-	-	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 3.3 V, V_L = 2.7 V V_D = 0.3 V / 3 V, V_S = 3 V / 0.3 V	Room	± 0.02	-1	1	-1	1	nA
			Full	-	-50	50	-5	5	
	$I_{D(off)}$		Room	± 0.02	-1	1	-1	1	
			Full	-	-50	50	-5	5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 3.3 V, V_L = 2.7 V V_S = V_D = 0.3 V / 3 V	Room	± 0.02	-1	1	-1	1	
			Full	-	-50	50	-5	5	
Digital Control									
Logic Low Input Voltage	V_{INL}	V_L = 2.7 V	Full	-	-	0.6	-	0.6	V
Logic High Input Voltage	V_{INH}		Full	-	1.8	-	1.8	-	
Logic Low Input Current	I_L	$V_{IN(A0, A1, A2 and enable)}$ under test = 0.6 V	Full	0.02	-1	1	-1	1	µA
Logic High Input Current	I_H	$V_{IN(A0, A1, A2 and enable)}$ under test = 1.8 V	Full	0.02	-1	1	-1	1	
Dynamic Characteristics									
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF see Fig. 1, 2, 3	Room	161	-	-	-	-	ns
			Full	-	-	-	-	-	
Enable Turn-On Time	$t_{ON(EN)}$		Room	120	-	-	-	-	
			Full	-	-	-	-	-	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	79	-	-	-	-	
			Full	-	-	-	-	-	
Break-Before-Make Time Delay	t_D		Room	98	-	-	-	-	
			Full	-	-	-	-	-	
Charge Injection [e]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Full	0.58	-	-	-	-	pC
Off Isolation [e]	OIRR	f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, 100 kHz	Room	-95	-	-	-	-	dB
Crosstalk [e]	X_{TALK}	f = 1 MHz, R_L = 50 Ω, C_L = 5 pF, 100 kHz	Room	-92	-	-	-	-	
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	3.7	-	-	-	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$		Room	4.7	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$		Room	10.4	-	-	-	-	
Power Supply									
Power Supply Range	I+	$V_{IN (A, B, C and enable)}$ = 0 V or 3 V	Room	0.05	-	1	-	1	µA
			Full	-	-	10	-	10	
Ground Current	I_{GND}		Room	0.05	-1	-	-1	-	
			Full	-	-10	-	-10	-	
Logic Supply Current	I_L	V_L = 2.7 V	Room	0.05	-	1	-	1	
			Full	-	-	10	-	10	

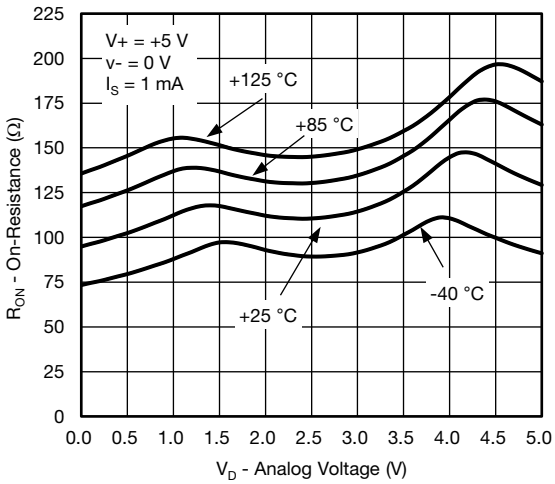
Notes

a. V_{IN} = input voltage to perform proper function.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.

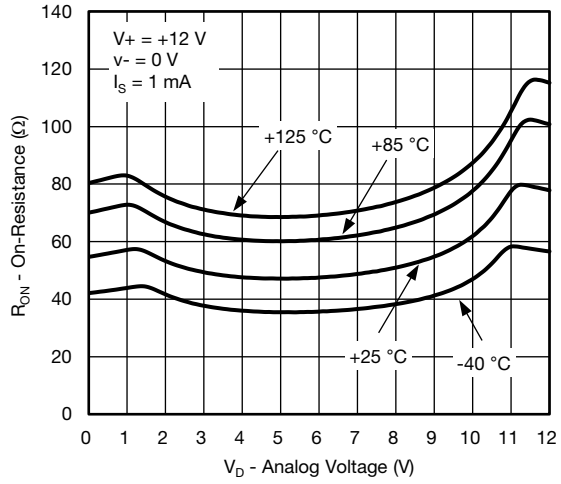
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



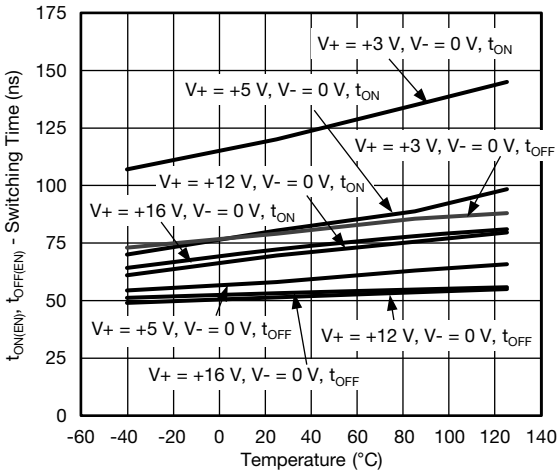
On-Resistance vs. V_D and Signal Supply Voltage



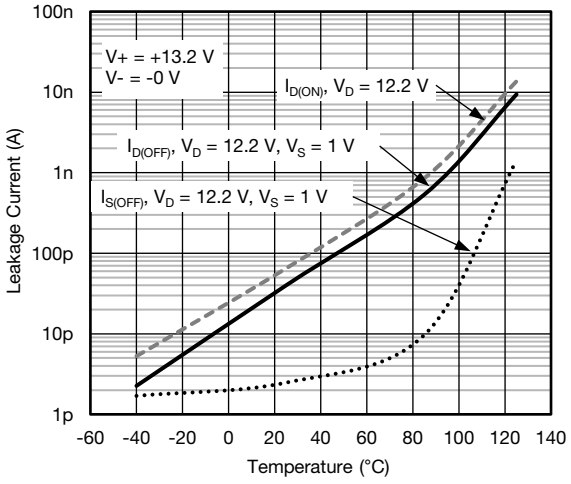
On-Resistance vs. Analog Voltage and Temperature



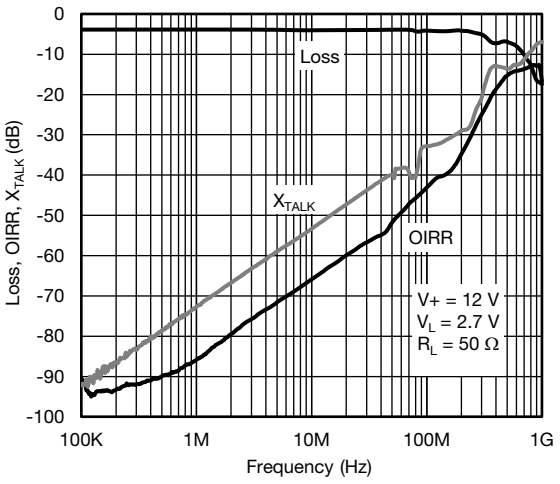
On-Resistance vs. Analog Voltage and Temperature



Switching Time vs. Temperature

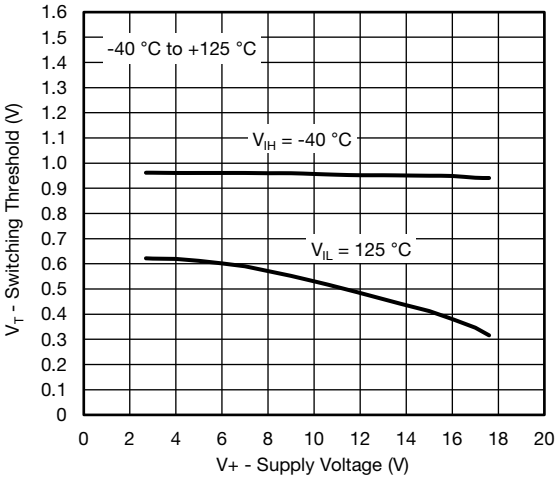


Leakage Current vs. Temperature

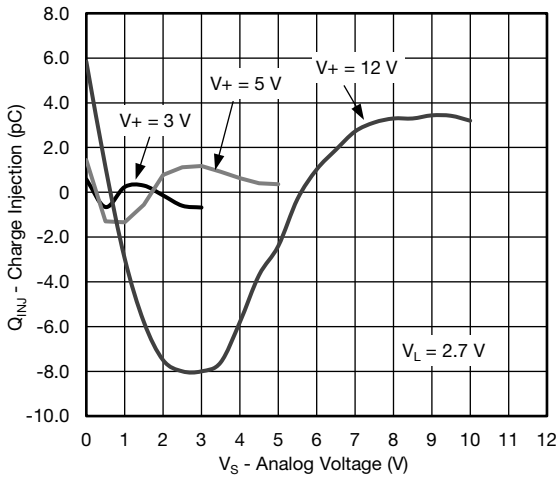


Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

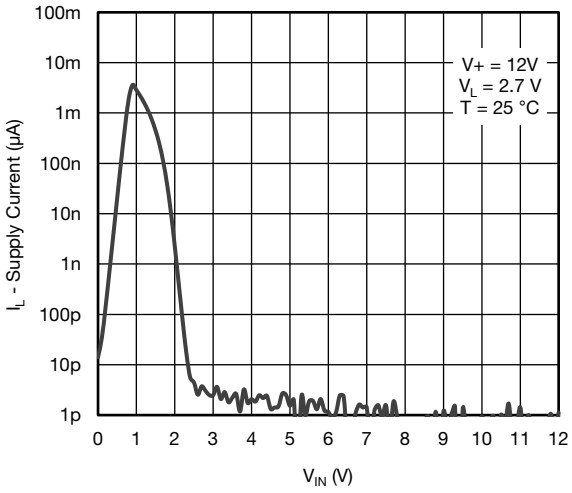
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Switching Threshold vs. Logic Supply Voltage

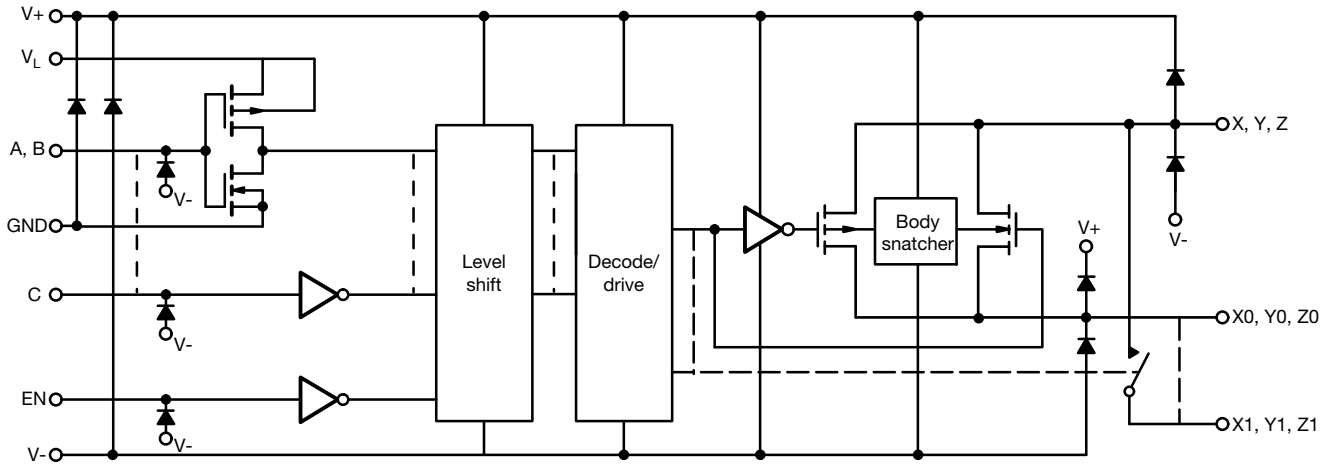


Charge Injection vs. Analog Voltage



I_L vs. V_{IN}

SCHEMATIC DIAGRAM (typical channel)



TEST CIRCUITS

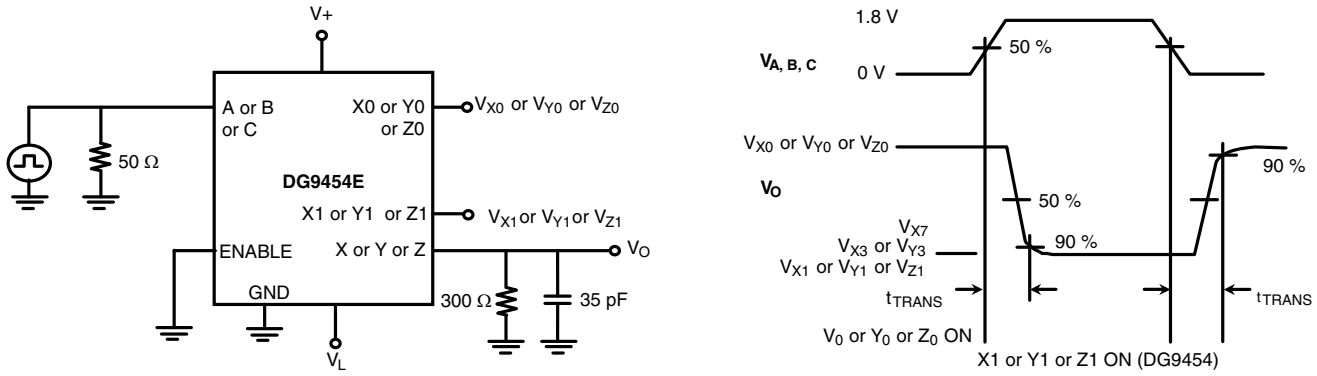


Fig. 1 - Transition Time

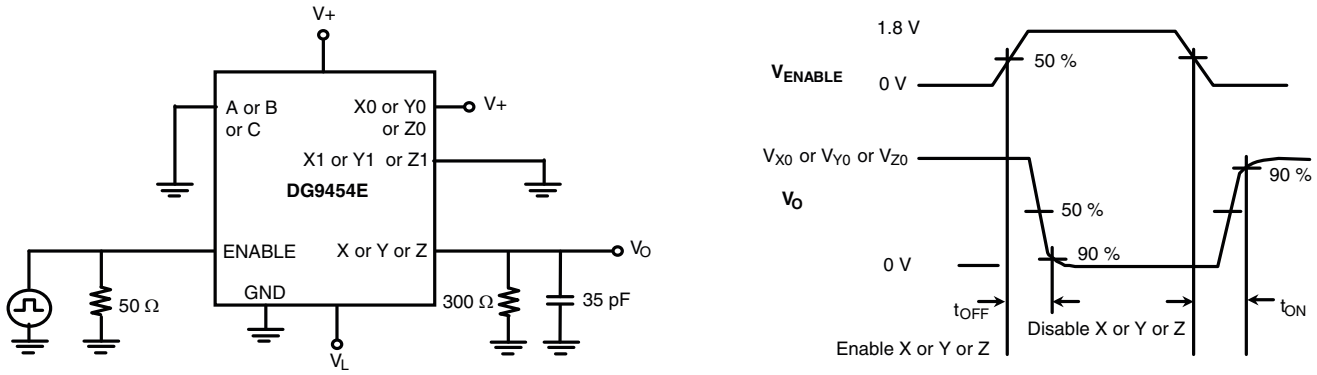


Fig. 2 - Enable Switching Time

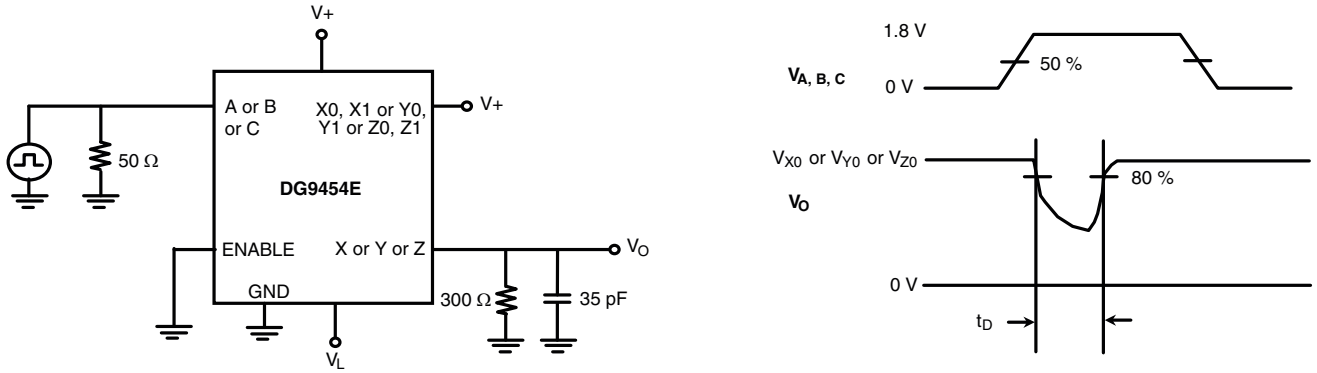
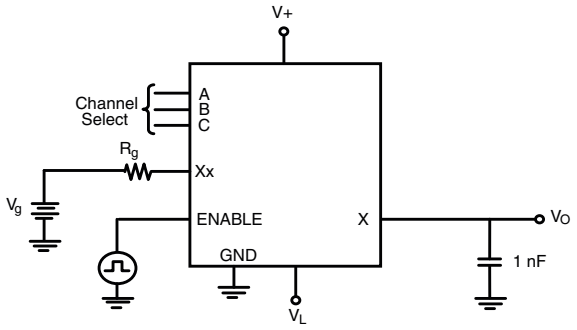


Fig. 3 - Break-Before-Make

TEST CIRCUITS



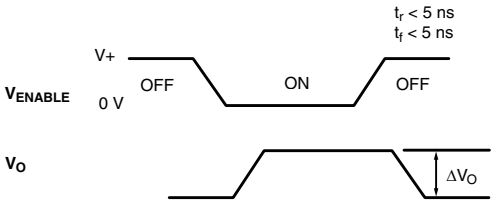
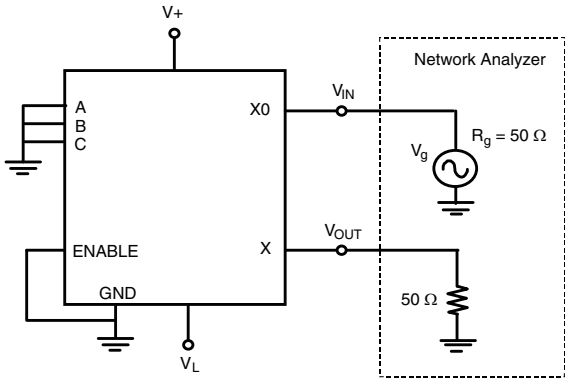
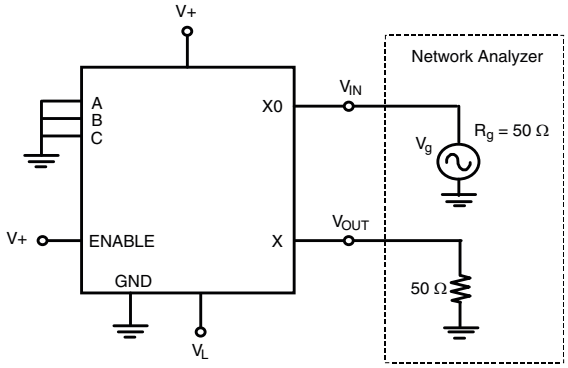


Fig. 4 - Charge Injection



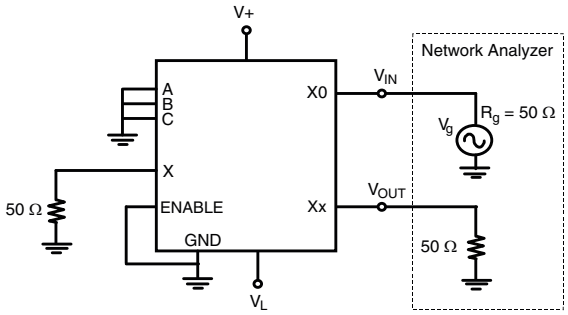
$$\text{Insertion Loss} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Fig. 5 - Insertion Loss



$$\text{Off Isolation} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Fig. 7 - Off Isolation



$$\text{Crosstalk} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Fig. 6 - Crosstalk

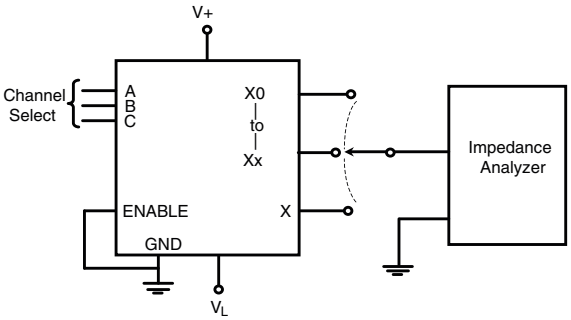
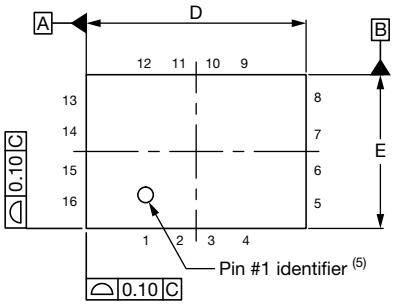


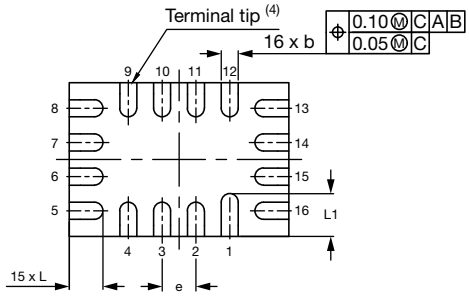
Fig. 8 - Source, Drain Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67172.

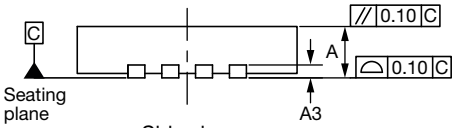
Thin miniQFN16 Case Outline



Top view



Bottom view



Side view

DIMENSIONS	MILLIMETERS (1)			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N (3)	16			16		
Nd (3)	4			4		
Ne (3)	4			4		

Notes

(1) Use millimeters as the primary measurement.

(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.

(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.

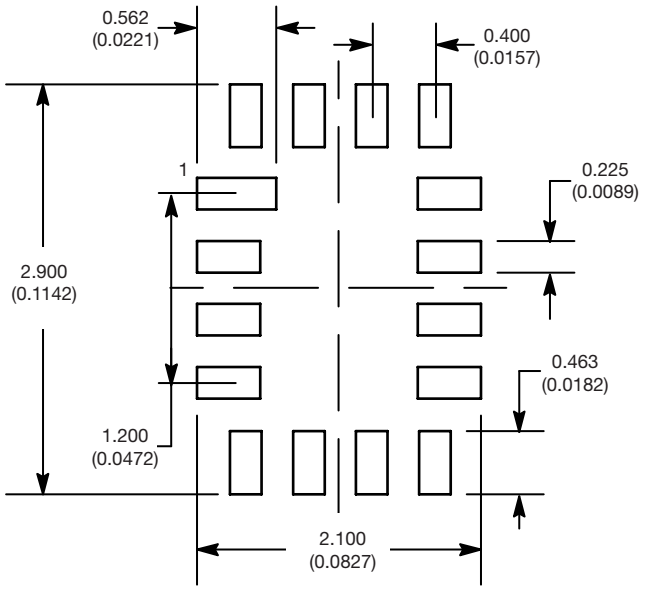
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.

(6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16
DWG: 6023

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint
Dimensions in mm (inch)

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