

# JSN, Unencapsulated Stacked Chip with Flat Terminations, 63 – 250 VDC, for DC Link (Automotive Grade)

## Overview

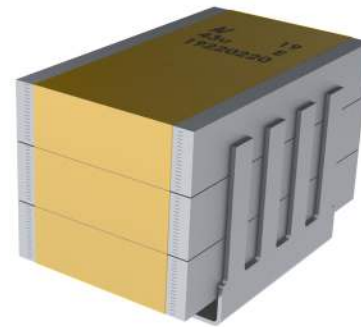
JSN is a jumbo stacked, naked metallized polyester film capacitor with flat terminations. Automotive grade devices meet the demanding Automotive Electronics Council's AEC-Q200 qualification requirements.

## Applications

JSN (Jumbo Stacked Naked) film capacitor is designed for applications requiring high reliability, long life, and severe working conditions, with high frequency SMPS, DC/DC and AC/DC converters, input/output filter in power supplies, DC-Link, industrial and automotive SMPS and inverters.

## Benefits

- Rated voltage: 63 – 250 VDC
- Rated voltage: 40 – 160 VAC
- Capacitance range: 5.6 – 82  $\mu$ F
- Capacitance tolerance:  $\pm$ 10%,  $\pm$ 20%
- Climatic category: 55/125/56
- RoHS compliant and lead-free terminations
- Operating temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Automotive Grade (AEC-Q200)
- Low ESR and ESL (high frequency applications)
- No piezoelectric effect
- No DC bias effect in capacitance drop and aging
- Nonpolarized construction (low self-heating in AC filtering applications)
- Inherent self-healing and elasticity properties



## Part Number System

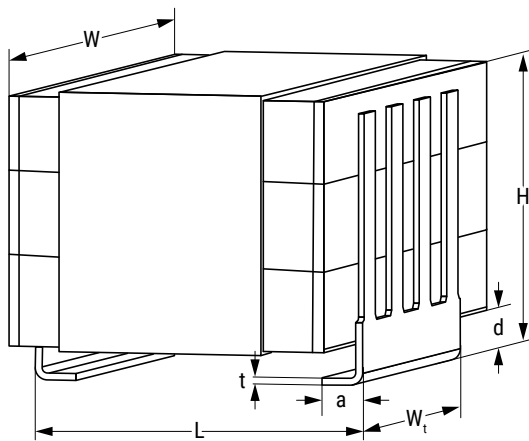
JSN	E	K	5100	M	B	6	L	0
Series	Rated Voltage (VDC)	Size Code	Capacitance Code (pF)	Capacitance Tolerance	Dielectric	Wt Terminal Width (mm)	Packaging	Internal Use
JSN = Jumbo Stacked Naked	D = 63 E = 100 I = 250	K = 6080 J = 60115	Digits 2-4 indicate the first three digits of the capacitance value. First digit indicates the number of zeros to be added.	K = $\pm$ 10% M = $\pm$ 20%	B = Metallized PET	6 = 20	See Ordering Options Table	0 (Standard)

## Ordering Options Table

Packaging Type	Packaging Code
<b>Standard Packaging Options</b>	
Bulk (Tray)	L
Tape & Reel (Standard Reel)*	N

\*Available only for size 60.80

## Dimensions – Millimeters



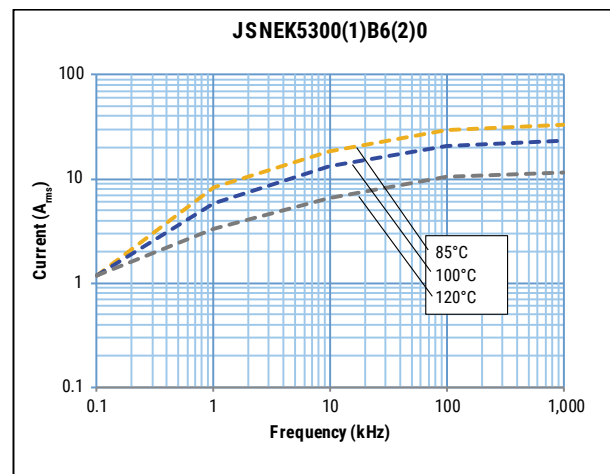
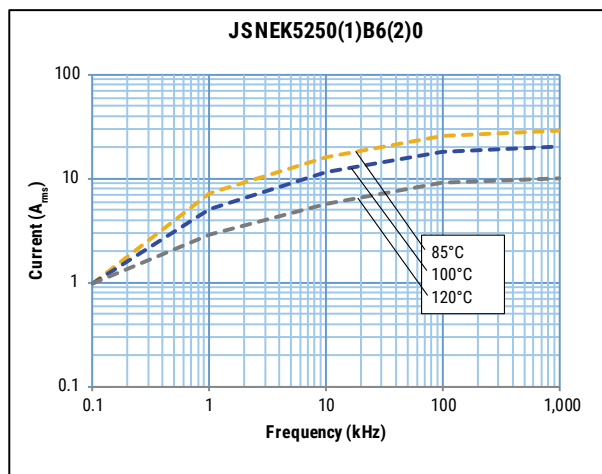
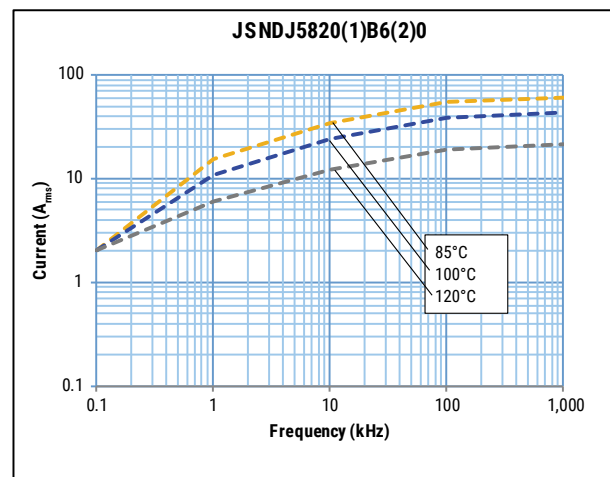
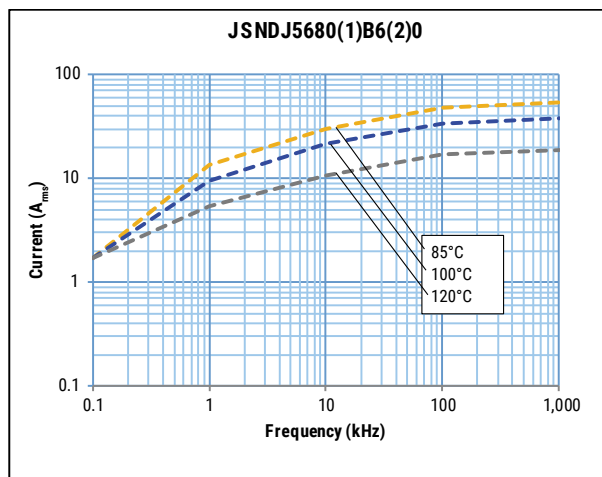
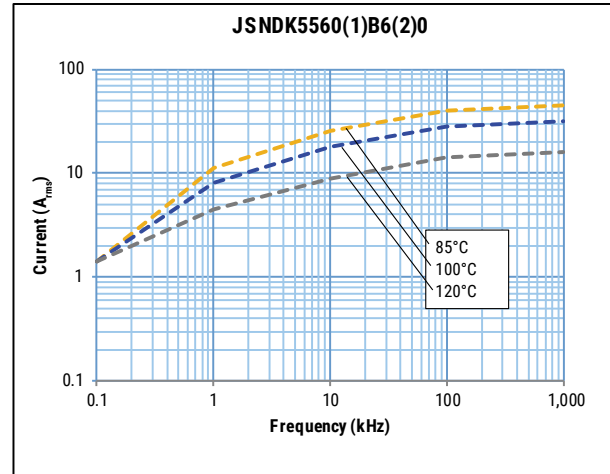
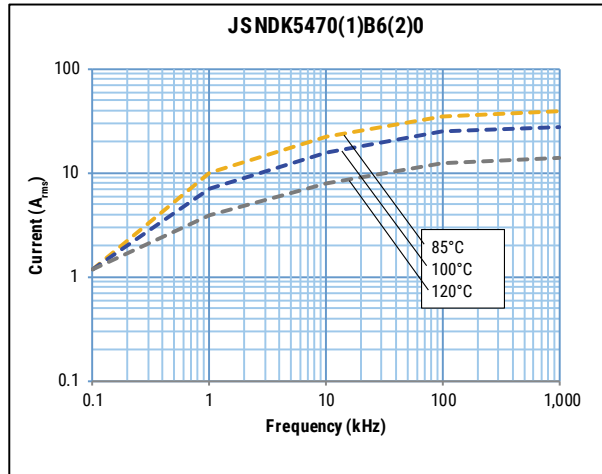
Size Code	Chip Size	W		W <sub>t</sub>		H	L	
		Nominal	Tolerance	Nominal	Tolerance		Nominal	Tolerance
K	6080	21.5	Maximum	20	Maximum	See Part Number Table	17.3	Maximum
J	60115	30.0	Maximum	20	Maximum		17.3	Maximum

Size Code	Chip Size	d		a		t	
		Nominal	Tolerance	Nominal	Tolerance	Nominal	Tolerance
K	6080	2	±1.0	2	±1.0	0.3	±0.1
J	60115	2	±1.0	2	±1.0	0.3	±0.1

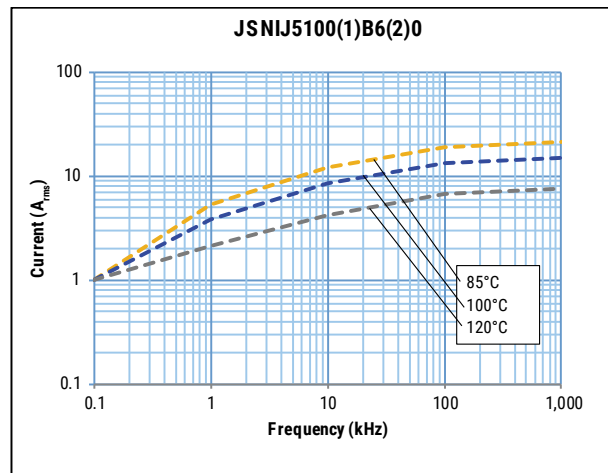
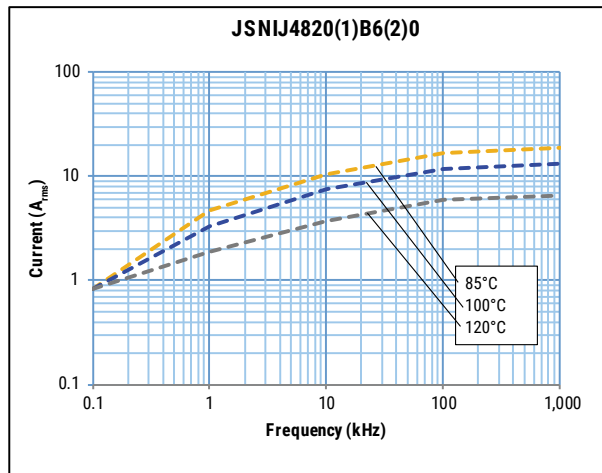
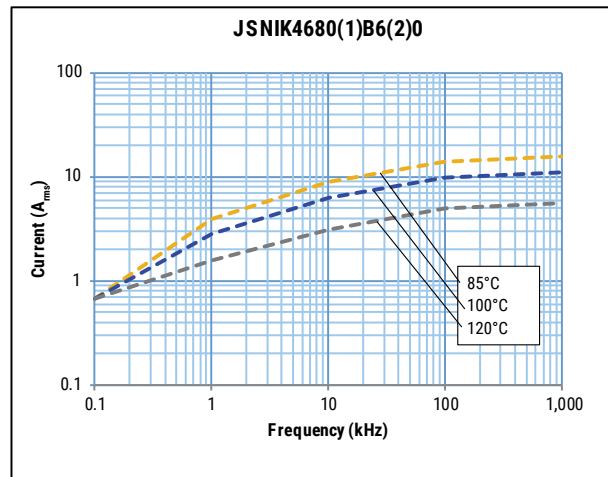
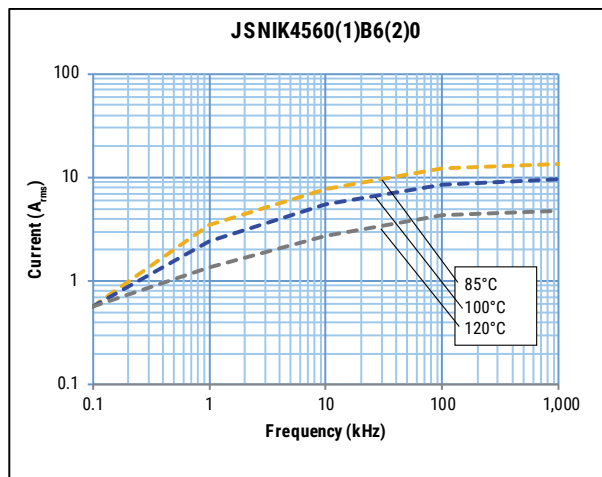
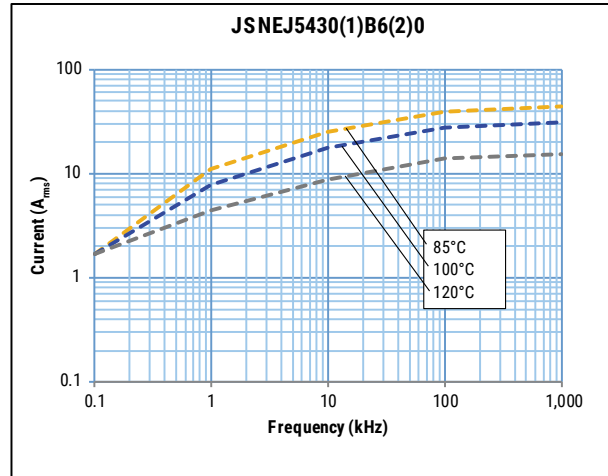
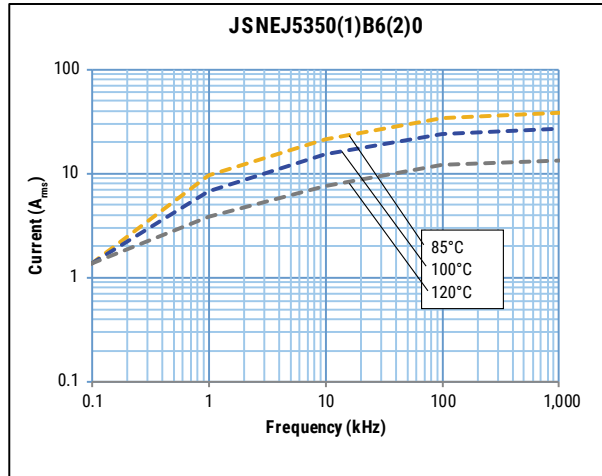
## Performance Characteristics

Voltage Range (VDC)	63	100	250
Voltage Range (VAC)	40	63	160
Capacitance Range ( $\mu\text{F}$ )	47 – 82	25 – 43	5.6 – 10
Capacitance Tolerance	$\pm 10\%$ , $\pm 20\%$		
Category Temperature Range	-55°C to +125°C		
Rated Temperature	+105°C		
Maximum Temperature Exposure	+150°C for maximum 250 hours, no Voltage applied		
Voltage Derating	The rated voltage is decreased by 1.25%/°C from +105°C to +125°C		
Climatic Category	55/125/56 IEC 60068-1		
Test Voltage	1.4 x $V_R$ applied for 2 seconds at +25°C, $\pm 5$		
Insulation Resistance	Measured at +25°C, $\pm 5^\circ\text{C}$		
	$V_R$ (VDC)	Between Terminals	
	63	$\geq 100 \text{ M}\Omega \cdot \mu\text{F}$	
	100	$\geq 250 \text{ M}\Omega \cdot \mu\text{F}$	
250	$\geq 800 \text{ M}\Omega \cdot \mu\text{F}$		
Dissipation Factor	Maximum Values at 25°C, $\pm 5^\circ\text{C}$		
	1 kHz	1.0%	

## Electrical Characteristics & Different Ambient Temperatures



## Electrical Characteristics & Different Ambient Temperatures cont.



## Environmental Test Data

Biased Humidity	
Test Conditions	
Temperature	+40°C ±2°C
Relative Humidity (RH)	93% ±2%
Applied Bias	Rated Voltage
Test Duration	56 days
Performance	
Capacitance Change  Δ C/C	≤ 10%
DF Change (Δtgδ)	≤ 0.5% at 1 kHz
Insulation Resistance	≥ 50% of limit value
Endurance	
Test Conditions	
Temperature	125°C ±2°C
Test Duration	2,000 hours
Voltage Applied	1.25 x V <sub>c</sub>
Performance	
Capacitance Change  Δ C/C	≤ 5%
DF Change (Δtgδ)	≤ 50 x 10 <sup>-4</sup> at 1 kHz
Insulation Resistance	≥ 50% of limit value
Rapid Change of Temperature	
Test Conditions	
Temperature	1 hour at -55°C, 1 hour at +125°C
Number of Cycles	1,000
Performance	
Capacitance Change  Δ C/C	≤ 5%
DF Change (Δtgδ)	≤ 50 x 10 <sup>-4</sup> at 1 kHz
Insulation Resistance	≥ limit value
No Mechanical Damage	

Reflow	
Test Conditions	See Solder Process
Performance	
Capacitance Change  Δ C/C	≤ 3%
DF Change (Δtgδ)	≤ 50 x 10 <sup>-4</sup> at 1 kHz
Insulation Resistance	≥ limit value
No Mechanical Damage	
Bending	
Test Conditions	
Deflection	1 – 6 mm
Performance	
Capacitance Change  Δ C/C	≤ 1%
No visible damage on the terminations (peeling) neither on the body (cracking)	

## Environmental Compliance

All KEMET surface mount capacitors are RoHS compliant.



**Table 1 – Ratings & Part Number Reference**

VDC	VAC	Capacitance Value (μF)	Size Code	Chip Size	Dimensions in mm			dV/dt (V/μs)	KEMET Internal Part Number	Customer Part Number
					W <sub>MAX</sub>	H <sub>MAX</sub>	L <sub>MAX</sub>			
63	40	47	K	6080	21.5	15.4	17.3	25	SNDK5470(1)B6(2)0	JSNDK5470(1)B6(2)0
63	40	56	K	6080	21.5	17.8	17.3	25	SNDK5560(1)B6(2)0	JSNDK5560(1)B6(2)0
63	40	68	J	60115	30	15.7	17.3	25	SNDJ5680(1)B6(2)0	JSNDJ5680(1)B6(2)0
63	40	82	J	60115	30	17.8	17.3	25	SNDJ5820(1)B6(2)0	JSNDJ5820(1)B6(2)0
100	63	25	K	6080	21.5	15.4	17.3	27	SNEK5250(1)B6(2)0	JSNEK5250(1)B6(2)0
100	63	30	K	6080	21.5	17.8	17.3	27	SNEK5300(1)B6(2)0	JSNEK5300(1)B6(2)0
100	63	35	J	60115	30	15.4	17.3	27	SNEJ5350(1)B6(2)0	JSNEJ5350(1)B6(2)0
100	63	43	J	60115	30	17.8	17.3	27	SNEJ5430(1)B6(2)0	JSNEJ5430(1)B6(2)0
250	160	5.6	K	6080	21.5	15.3	17.3	40	SNIK4560(1)B6(2)0	JSNIK4560(1)B6(2)0
250	160	6.8	K	6080	21.5	17.8	17.3	40	SNIK4680(1)B6(2)0	JSNIK4680(1)B6(2)0
250	160	8.2	J	60115	30	16	17.3	40	SNIJ4820(1)B6(2)0	JSNIJ4820(1)B6(2)0
250	160	10	J	60115	30	18.3	17.3	40	SNIJ5100(1)B6(2)0	JSNIJ5100(1)B6(2)0
VDC	VAC	Capacitance Value (μF)	Size Code	Chip Size	W <sub>MAX</sub>	H <sub>MAX</sub>	L <sub>MAX</sub>	dV/dt (V/μs)	KEMET Internal Part Number	Customer Part Number

(1)  $K = \pm 10\%$ ,  $M = \pm 20\%$ .

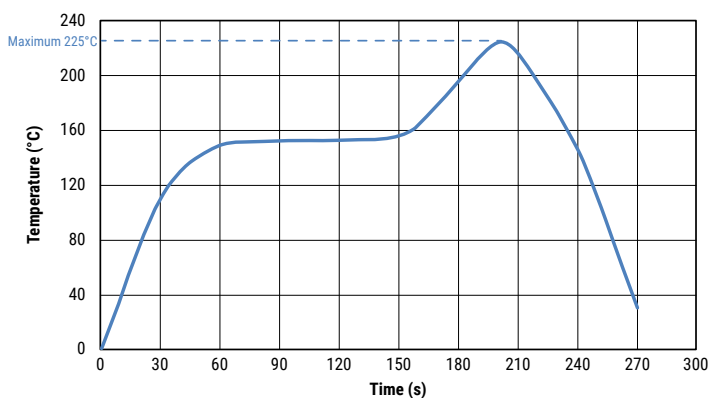
(2) Insert packaging code. See Ordering Options Table for available options.

## Soldering Process

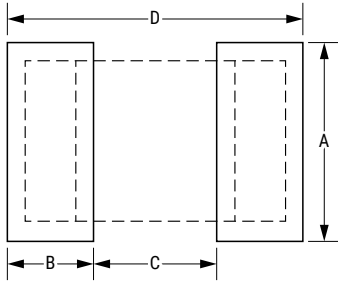
JSN Series capacitors are to be mounted with reflow process (see thermal profile) or gluing.

Reflow soldering temperature measured on the top body surface of the component: Preheating temperature should be less than 160°C. The peak temperature must not exceed 225°C.

If two reflow processes are needed, make sure that before the second reflow the temperature on the capacitor's surface is lower than 50°C.

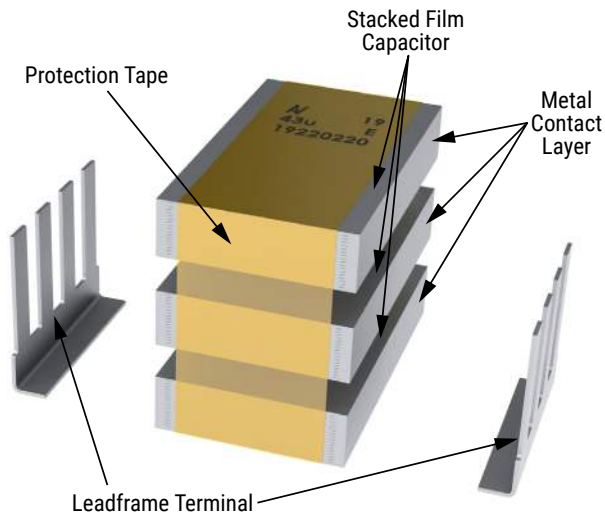


## Landing



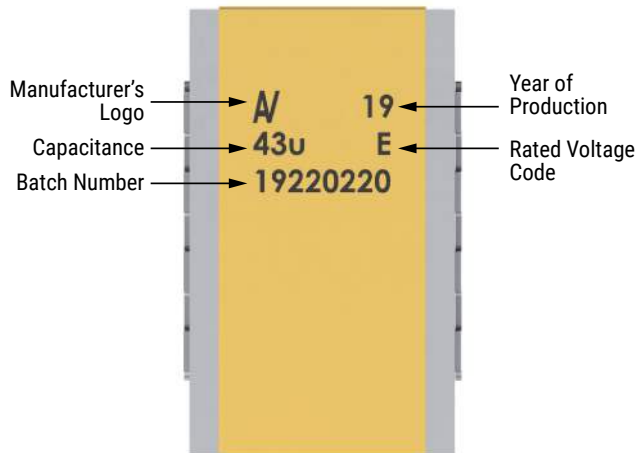
Size Code	Dimensions in mm			
	A	B	C	D
60.80	21.9	5.0	10.2	20.2
60.115	30.4	5.0	10.2	20.2
Sn/Ag/Cu soldering paste (Suggested thickness: 0.20 – 0.25 mm)				

## Construction





## Marking



## Flux & Cleaning

KEMET recommends using a no-clean flux with a halogen content lower than 0.1%. To clean the PCB assembly KEMET recommends to use a suitable solvent like Isopropyl alcohol, deionized water, or neutral pH detergents. Aggressive solvents shall not be used. For any different cleaning solvent used please contact KEMET Technical Services to analyze the potential impact on KEMET products.

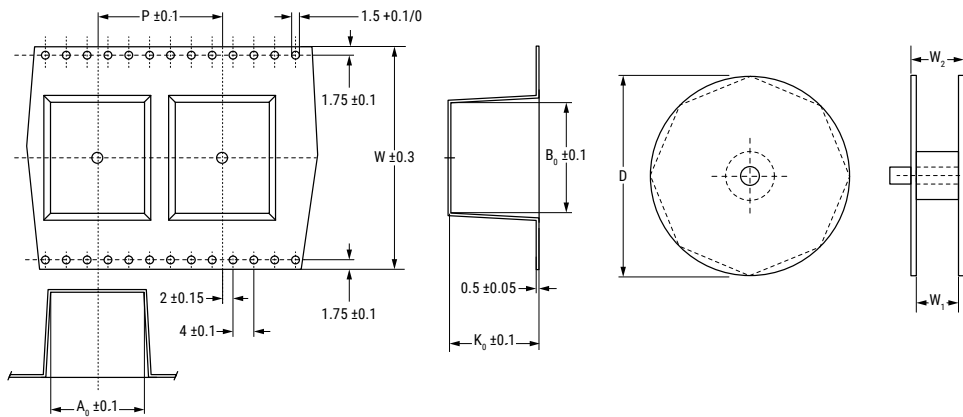
## Storage and Moisture Recommendations

KEMET SMD film capacitors are supplied in a moisture barrier bag (MBB) Class 1. We can guarantee a 24 month shelf life (temperature  $\leq 40^{\circ}\text{C}$ /relative humidity  $\leq 90\%$ ). After the MBB has been opened, components may stay in areas with controlled temperature and humidity (temperature  $\leq 30^{\circ}\text{C}$ /relative humidity  $\leq 60\%$ ) for 72 hours (MSL 4). For longer periods of time and/or higher temperature and/or higher relative humidity values, it is absolutely necessary to protect the components against humidity. If the reel inside the MBB is partially used, KEMET recommends to re-use the same MBB or to avoid areas without controlled temperature and humidity (see above). If the above conditions are not respected, components require baking (minimum time: 24 hours at  $70 \pm 5^{\circ}\text{C}$ ) before the reflow.

## Packaging Quantities

Chip Size (EIA)	Height (mm)	Tray	Reel
6080	All	308	120
60115	All	252	-

## Carrier Taping & Packaging (IEC 60286-2)



Chip Size (EIA) Horizontal Mounting	Taping Specification							
	W	P	A <sub>0</sub>	B <sub>0</sub>	K <sub>0</sub>	D	W <sub>1</sub>	W <sub>2</sub>
	±0.3	±0.1	Nominal	Nominal	Nominal	±2.0	-0/+2	Maximum
6080	44	24	18	22	17	330	44.5	49.5

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