S1C31D01 (rev1.2)

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32-bit Single Chip Microcontroller

- Arm® 32-bit RISC CPU core Cortex®-M0+
- Embedded 256K-byte flash memory and 96K-byte RAM
- Various interfaces such as UART, QSPI, I²C, and USB that support DMA transfer
- Built-in memory display controller
- Low power memory display voltage booster

■ DESCRIPTIONS

The S1C31D01 is a 32-bit MCU with an Arm® Cortex®-M0+ processor included that features low-power operation. It incorporates a lot of serial interface circuits, a memory display controller, and a voltage booster. This MCU is suitable for various kinds of battery-driven controller applications.

■ FEATURES

Model	S1C31D01
CPU	
CPU core	Arm® 32-bit RISC CPU core Cortex®-M0+
Other	Serial-wire debug ports (SW-DP) and a micro trace buffer (MTB) included
Embedded Flash memory	
Capacity	256K bytes (for both instructions and data)
Erase/program count	1,000 times (min.) * When being programmed by the dedicated flash loader
Other	On-board programming function
	Flash programming voltage can be generated internally.
Embedded RAMs	
General-purpose RAM	96K bytes (shared with MDC and MTB)
Instruction cache	512 bytes
DMA Controller (DMAC)	
Number of channels	4 channels
Data transfer path	Memory to memory, memory to peripheral, and peripheral to memory
Transfer mode	Basic, ping-pong, scatter-gather
DMA trigger source	UART3, SPIA, QSPI, I2C, USB, T16B, SNDA, ADC12A, and software
Clock generator (CLG)	
System clock source	4 sources (IOSC/OSC1/OSC3/EXOSC)
System clock frequency (operating frequency)	V_{D1} voltage mode = mode0: 21 MHz (max.) V_{D1} voltage mode = mode1: 2.1 MHz (max.)
IOSC oscillator circuit (boot clock source)	V_{D1} voltage mode = mode0: 20/16/12/8/2/1 MHz (typ.) software selectable V_{D1} voltage mode = mode1: 2/1 MHz (typ.) software selectable
	10 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)
OSC1 oscillator circuit	32.768 kHz (typ.) crystal oscillator
	32kHz (typ.) embedded oscillator
	Oscillation stop detection circuit included
OSC3 oscillator circuit	20.5 MHz (max.) crystal/ceramic oscillator
EXOSC clock input	21 MHz (max.) square or sine wave input
Other	Configurable system clock division ratio
	Configurable system clock used at wake up from SLEEP state
	Operating clock frequency for the CPU and all peripheral circuits is selectable.
I/O port (PPORT)	
Number of general-purpose I/O ports	57 bits (max.)
	Pins are shared with the peripheral I/O.
Number of input interrupt ports	53 bits (max.)
Number of ports that support universal port multiplexer (UPMUX)	30 bits
	A peripheral circuit I/O function selected via software can be assigned to each port.
Timers	
Watchdog timer (WDT2)	Generates NMI or watchdog timer reset.
	Programmable NMI/reset generation cycle
Real-time clock (RTCA)	128–1 Hz counter, second/minute/hour/day/day of the week/month/year counters
	Theoretical regulation function for 1-second correction
	Alarm and stopwatch functions
16-bit timer (T16)	8 channels
	Generates the SPIA and QSPI master clocks, and the ADC12A operating clock/trigger signal.
16-bit PWM timer (T16B)	2 channels
	Event counter/capture function
	PWM waveform generation function
	Number of PWM output or capture input ports: 6 ports/channel

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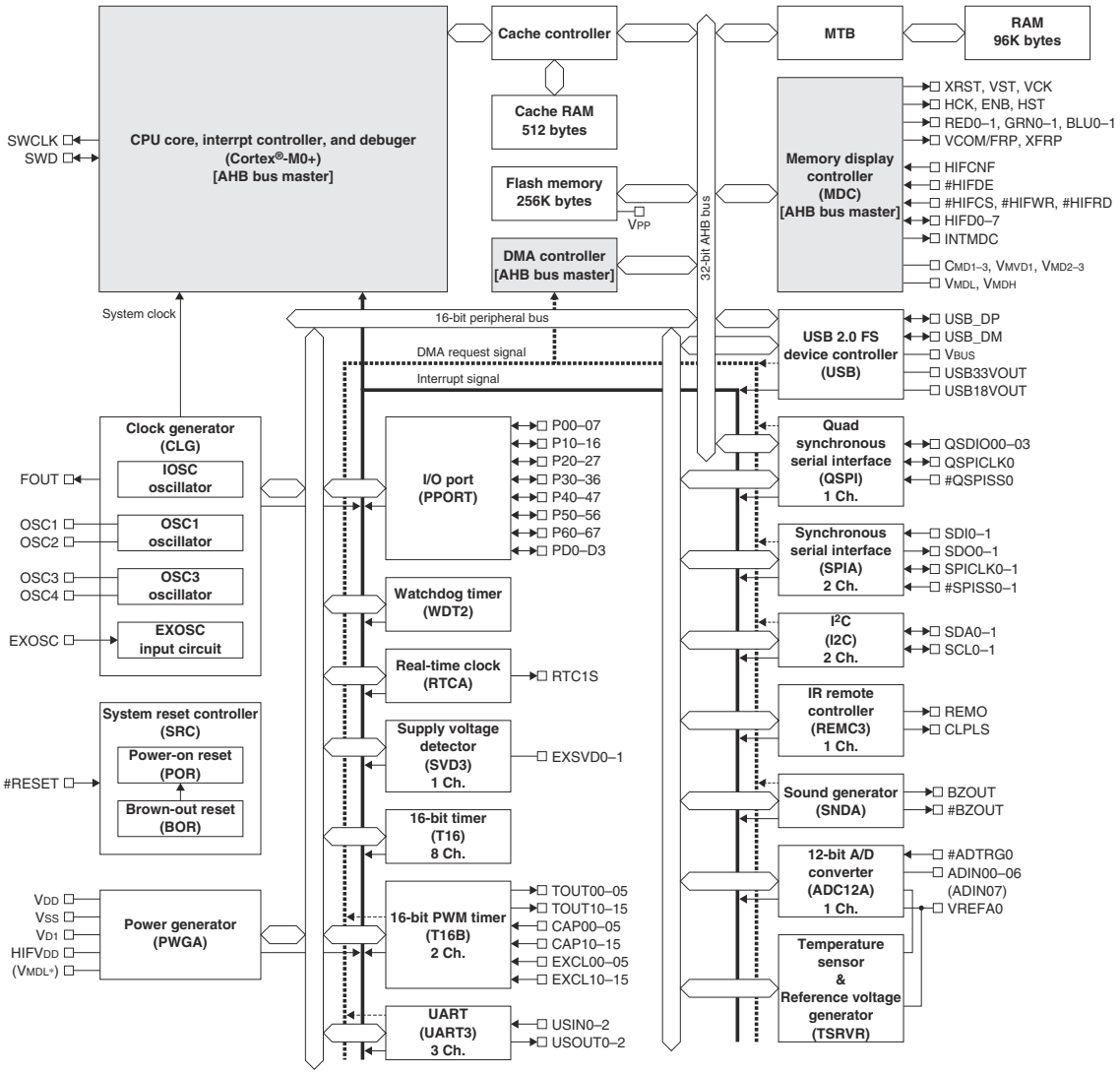
Model	S1C31D01
Supply voltage detector (SVD3)	
Number of channels	1 channel
Detection voltage	V_{DD} or an external voltage (2 external detection ports are available.)
Detection level	V_{DD}: 28 levels (1.8 to 5.0 V)/external voltage: 32 levels (1.2 to 5.0 V)
Other	Intermittent operation mode
	Generates an interrupt or reset according to the detection level evaluation.
Serial interfaces	
UART (UART3)	3 channels
	Baud-rate generator included, IrDA1.0 supported
	Open drain output, signal polarity, and baud rate division ratio are configurable.
	Infrared communication carrier modulation output function
Synchronous serial interface (SPIA)	2 channels
	2 to 16-bit variable data length
	The 16-bit timer (T16) can be used for the baud-rate generator in master mode.
Quad synchronous serial interface (QSPI)	1 channel
	Supports single, dual, and quad transfer modes.
	Low CPU overhead memory mapped access mode that can directly read data from the external flash memory with XIP (eXecute-In-Place) mode.
I^2C (I2C) *1	2 channels
	Baud-rate generator included
USB 2.0 FS device controller (USB)	
Number of transceiver/receiver channels	1 channel
Transfer rate	FS (12 Mbps)
Clock source	OSC3 (12 MHz) + PLL
Number of endpoints	4 endpoints (3 general-purpose endpoints and endpoint 0)
Power supply	Voltage regulators for USB included
Sound generator (SNDA)	
Buzzer output function	512 Hz to 16 kHz output frequencies
	One-shot output function
Melody generation function	Pitch: 128 Hz to 16 kHz ≈ C3 to C6
	Duration: 7 notes/rests (Half note/rest to thirty-second note/rest)
	Tempo: 16 tempos (30 to 480)
	Tie/slur may be specified.
IR remote controller (REMC3)	
Number of transmitter channels	1 channel
Other	EL lamp drive waveform can be generated (by the hardware) for an application example.
	Output inversion function
12-bit A/D converter (ADC12A)	
Conversion method	Successive approximation type
Resolution	12 bits
Number of conversion channels	1 channel
Number of analog signal inputs	8 ports/channel (The temperature sensor output is connected to a port.)
Temperature sensor/reference voltage generator (TSRVR)	
Temperature sensor circuit	Sensor output can be measured using ADC12A.
Reference voltage generator	Reference voltage for ADC12A is selectable from 2.0 V, 2.5 V, V_{DD}, and external input.
Memory display controller (MDC)	
Memory display interfaces	Parallel 6-bit color, SPI 1-bit black and white, SPI 3-bit color, 8-bit parallel/3-/4-wire serial 1/2/4/8 bpp grayscale
Orientations	0, 90, 180, 270 degrees rotation between display buffer and device
Host interface	Indirect 8-bit parallel, SPI, and QSPI
Graphics acceleration	Image/bitmap copy with scaling/rotation and shearing
	Drawing functions (line, rectangle, ellipse, arc)
	Copy and drawing functions can alpha-blend the source pixels with destination pixels.
Power generator	V_{MDL}: 2.7 to 3.4 V output software selectable
	V_{MDH}: 4.4 to 5.05 V output software selectable
Reset	
#RESET pin	Reset when the reset pin is set to low.
Power-on reset	Reset at power on.
Brown-out reset	Reset when the power supply voltage drops (when $V_{DD} \leq 1.45$ V (typ.) is detected).
Key entry reset	Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register).
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register).
Interrupt	
Non-maskable interrupt	6 systems (Reset, NMI, HardFault, SVCall, PendSV, SysTic)
Programmable interrupt	External interrupt: 1 system (4 levels)
	Internal interrupt: 28 systems

Model	S1C31D01	
Power supply voltage		
V_{DD} operating voltage	1.8 to 5.5 V	∗ If V_{DD} > 3.6 V, the V_{D1} voltage mode must be set to mode0.
V_{DD} operating voltage for Flash programming	2.4 to 5.5 V 2.4 to 5.5 V	(when V_{PP} is supplied externally) (when V_{PP} is generated internally)
V_{DD} operating voltage when generating MDC drive voltage	2.0 to 5.5 V	
$HIFV_{DD}$ operating voltage	1.8 to 5.5 V	(power supply voltage for host interface, P2 and P3 port groups)
V_{MDL} voltage when supplying externally	1.8 to 5.5 V	(required when MDC is not used)
Operating temperature		
Operating temperature range	-40 to 85 °C	
Current consumption (Typ. value)		
SLEEP mode ∗2	0.46 µA	IOSC = OFF, OSC1 = OFF, OSC3 = OFF
	0.95 µA	IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OSC3 = OFF, RTCA = ON
HALT mode ∗3	1.7 µA	IOSC = OFF, OSC1 = 32.768 kHz (crystal oscillator), OSC3 = OFF
RUN mode	250 µA/MHz	V_{D1} voltage mode = mode0, CPU = IOSC
	155 µA/MHz	V_{D1} voltage mode = mode1, CPU = IOSC
Shipping form		
1 ∗4	VFBGA5H-81 (P-VFBGA-081-0505-0.50, 5 × 5 mm, t = 1.0 mm, 0.5 mm pitch)	
2	WCSP96 (4.45 × 4.45 mm, t = 0.7 mm, 0.4 mm pitch)	
3 ∗4	TQFP14-80PIN (P-TQFP080-1212-0.50, 12 × 12 mm, t = 1.2 mm, 0.5 mm pitch)	
4	Die form (pad pitch: 80 µm (min.))	

∗1 The input filter in I2C (SDA and SCL inputs) does not comply with the standard for removing noise spikes less than 50 ns.
∗2 SLEEP mode refers to deep sleep mode in the Cortex®-M0+ processor. The RAM retains data even in SLEEP mode.
∗3 HALT mode refers to sleep mode in the Cortex®-M0+ processor.
∗4 Shown in parentheses are JEITA package names.

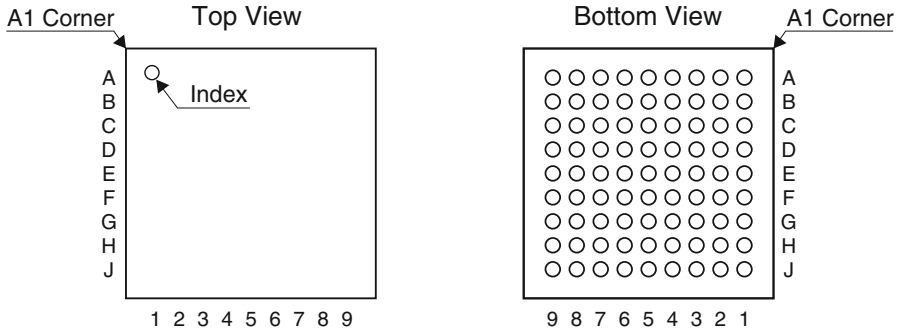
■ BLOCK DIAGRAM



∗ Supply when MDC is not used.

■ PIN CONFIGURATION DIAGRAMS

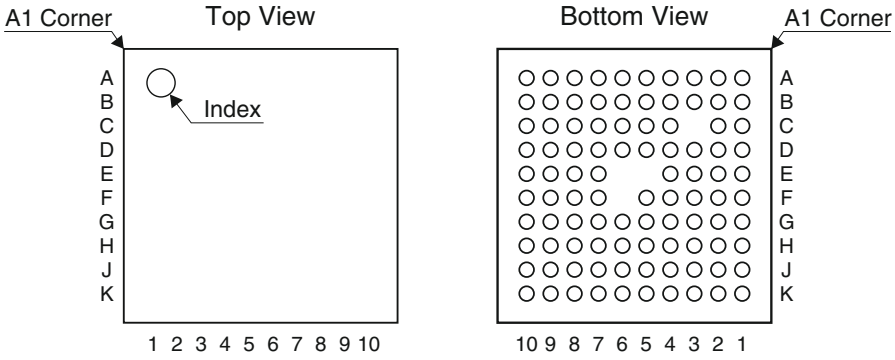
VFBGA5HX-81



Top View

	1	2	3	4	5	6	7	8	9
A	**P47** BLU0	**P45** GRN0	**P42** HST	**P36** INTMDC UPMUX	**P33** HIFD5 UPMUX	**P31** HIFD3 UPMUX	**P27** HIFD1 UPMUX	**P24** #HIFDE UPMUX	**P23** #HIFWR UPMUX
B	**P50** BLU1	**P46** GRN1	**P43** RED0	**P35** HIFD7 UPMUX	**P32** HIFD4 UPMUX	**P30** HIFD2 UPMUX	**P26** HIFD0 UPMUX	**P22** #HIFRD UPMUX	**P21** #HIFCS UPMUX
C	**P52** ENB	**P51** HCK	**P44** RED1	**P40** VCOM	**P34** HIFD6 UPMUX	**HIFV$_{DD}$**	**P25** UPMUX	**P20** HIFCNF UPMUX	**P67** EXCL01
D	**V$_{MDL}$**	**P54** VST	**P53**	**P41** XFRP	**P66** FOUT	**P62** QSDIO01	**P63** QSDIO02	**P65** #QSPISS0	**P64** QSDIO03
E	**V$_{MD3}$**	**V$_{MDH}$**	**USB33VOUT**	**P56** VCK	**P55** XRST	**P16** (ENVPP) EXCL11 UPMUX	**V$_{PP}$**	**P60** QSPICLK0	**P61** QSDIO00
F	**C$_{MD3}$**	**V$_{MD2}$**	**USB18VOUT**	**P13** SPICLK1 UPMUX	N.C.	**SWCLK** PD0	**TEST**	**P14** BZOUT UPMUX EXSVD0	**P15** #ADTRG UPMUX EXSVD1
G	**V$_{MVD1}$**	**C$_{MD2}$**	**P11** SDI1 UPMUX	**P12** SDO1 UPMUX	**P00** UPMUX VREFA0	**P05** RTC1S UPMUX ADIN04	**V$_{D1}$**	**V$_{DD}$**	**OSC2**
H	**V$_{BUS}$**	**C$_{MD1}$**	**P10** #SPISS1 UPMUX	**P01** EXCL00 UPMUX ADIN00	**P04** CLPLS UPMUX ADIN03	**P06** EXOSC UPMUX ADIN05	**SWD** PD1	**#RESET**	**OSC1**
J	**V$_{SS}$**	**USB_DM**	**USB_DP**	**P02** EXCL10 UPMUX ADIN01	**P03** REMO UPMUX ADIN02	**P07** #BZOUT UPMUX ADIN06	**PD2** OSC3	**PD3** OSC4	**V$_{SS}$**

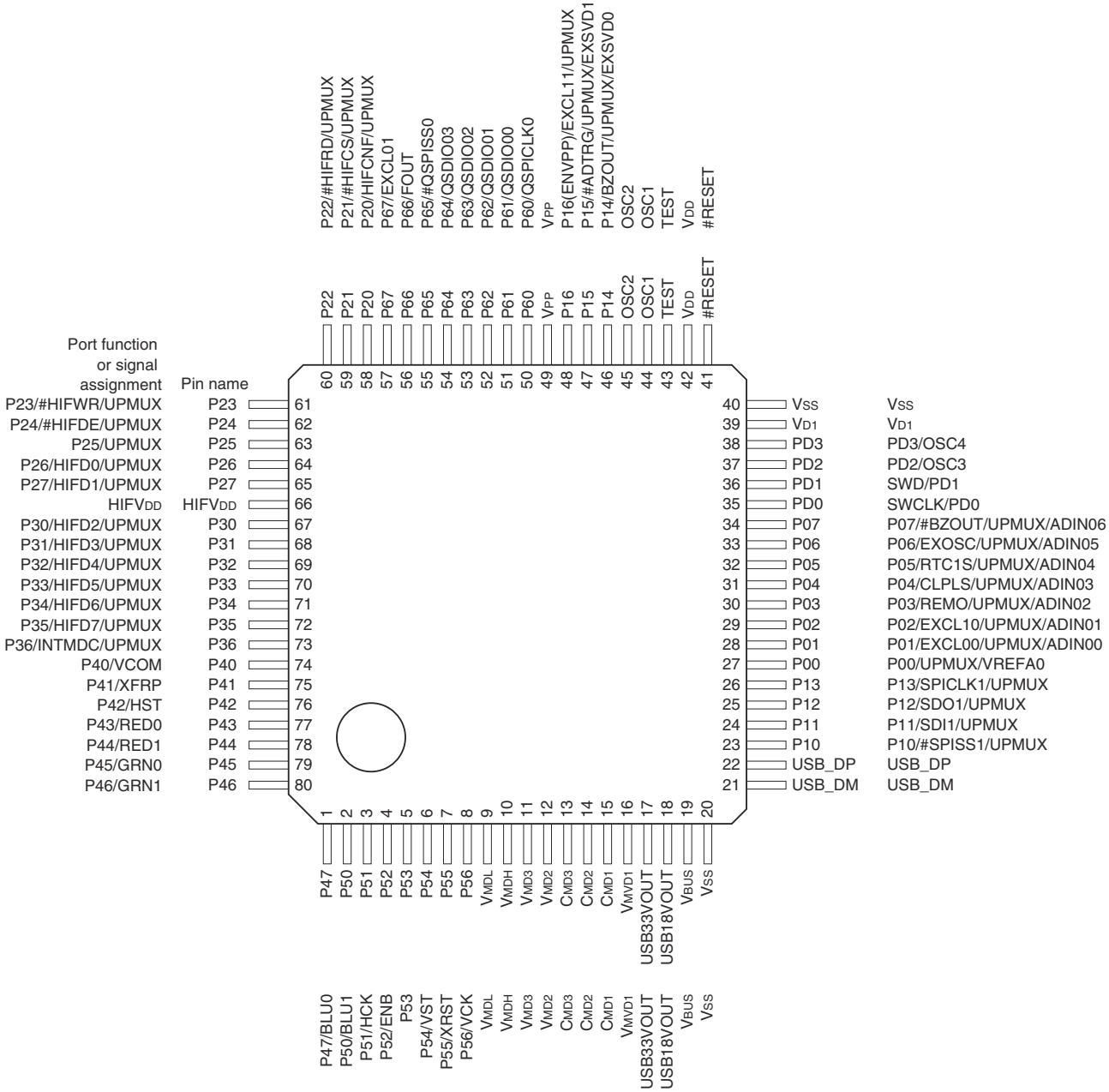
WCSP96



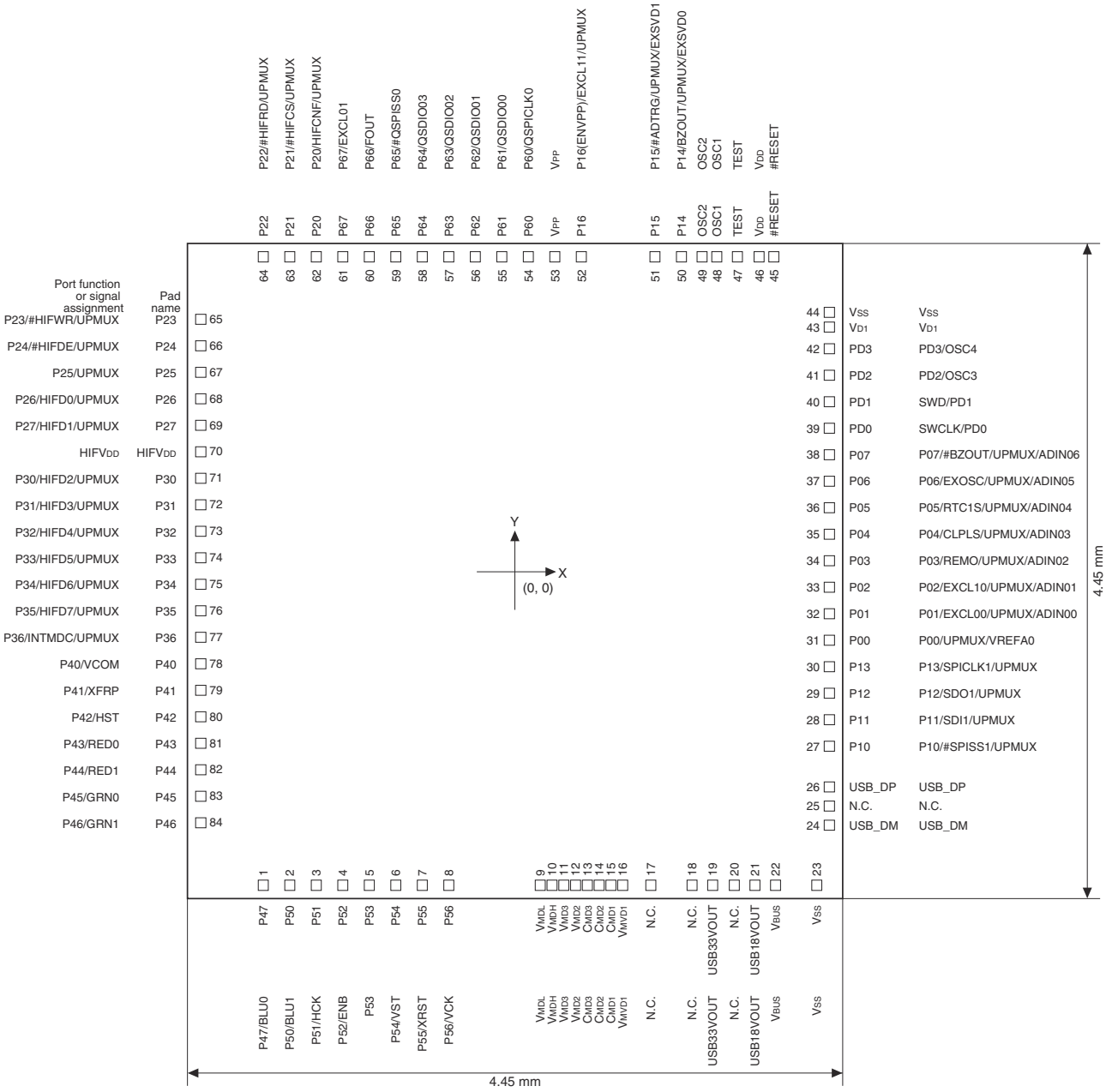
Top View

	1	2	3	4	5	6	7	8	9	10
A	N.C.	N.C.	**P53**	**V_{MDL}**	**V_{MDH}**	**V_{MD2}**	**C_{MD1}**	**V_{MVD1}**	N.C.	N.C.
B	N.C.	N.C.	**P50** BLU1	**P52** ENB	**V_{MD3}**	**C_{MD3}**	**C_{MD2}**	**USB33VOUT**	N.C.	N.C.
C	**P43** RED0	**P44** RED1		**P47** BLU0	**P51** HCK	**P55** XRST	**P56** VCK	**USB18VOUT**	**USB_DM**	**USB_DP**
D	**P40** VCOM	**P41** XFRP	**P42** HST	**P45** GRN0	**P46** GRN1	**P54** VST	**P10** #SPISS1 UPMUX	**V_{BUS}**	**V_{SS}**	**P11** SDI1 UPMUX
E	**P34** HIFD6 UPMUX	**P33** HIFD5 UPMUX	**P35** HIFD7 UPMUX	**P36** INTMDC UPMUX			**P12** SDO1 UPMUX	**P13** SPICLK1 UPMUX	**P01** EXCL00 UPMUX ADIN00	**P00** UPMUX VREFA0
F	**P32** HIFD4 UPMUX	**P31** HIFD3 UPMUX	**P30** HIFD2 UPMUX	**P27** HIFD1 UPMUX	**P63** QSDIO02		**P05** RTC1S UPMUX ADIN04	**P04** CLPLS UPMUX ADIN03	**P02** EXCL10 UPMUX ADIN01	**P03** REMO UPMUX ADIN02
G	**$HIFV_{DD}$**	**P26** HIFD0 UPMUX	**P24** #HIFDE UPMUX	**P67** EXCL01	**P62** QSDIO01	**TEST**	**SWD** PD1	**SWCLK** PD0	**P07** #BZOUT UPMUX ADIN06	**P06** EXOSC UPMUX ADIN05
H	**P25** UPMUX	**P23** #HIFWR UPMUX	**P22** #HIFRD UPMUX	**P66** FOUT	**V_{PP}**	**P14** BZOUT UPMUX EXSVD0	**V_{SS}**	**V_{D1}**	**PD3** OSC4	**PD2** OSC3
J	N.C.	N.C.	**P21** #HIFCS UPMUX	**P65** #QSPISS0	**P60** QSPICLK0	**P15** #ADTRG UPMUX EXSVD1	**V_{DD}**	**#RESET**	N.C.	N.C.
K	N.C.	N.C.	**P20** HIFCNF UPMUX	**P64** QSDIO03	**P61** QSDIO00	**P16** (ENVPP) EXCL11 UPMUX	**OSC2**	**OSC1**	N.C.	N.C.

TQFP14-80PIN



Chip


Port function or signal assignment
Pad name
P23/#HIFWR/UPMUX P23 65
P24/#HIFDE/UPMUX P24 66
P25/UPMUX P25 67
P26/HIFD0/UPMUX P26 68
P27/HIFD1/UPMUX P27 69
HIFVDD HIFVDD 70
P30/HIFD2/UPMUX P30 71
P31/HIFD3/UPMUX P31 72
P32/HIFD4/UPMUX P32 73
P33/HIFD5/UPMUX P33 74
P34/HIFD6/UPMUX P34 75
P35/HIFD7/UPMUX P35 76
P36/INTMDC/UPMUX P36 77
P40/VCOM P40 78
P41/XFRP P41 79
P42/HST P42 80
P43/RED0 P43 81
P44/RED1 P44 82
P45/GRN0 P45 83
P46/GRN1 P46 84
64 P22 P22/#HIFRD/UPMUX
63 P21 P21/#HIFCS/UPMUX
62 P20 P20/HIFCNF/UPMUX
61 P67 P67/EXCL01
60 P66 P66/FOUT
59 P65 P65/#QSPISS0
58 P64 P64/QSDIO03
57 P63 P63/QSDIO02
56 P62 P62/QSDIO01
55 P61 P61/QSDIO00
54 P60 P60/QSPICLK0
53 VPP VPP
52 P16 P16(ENVPP)/EXCL11/UPMUX
51 P15 P15/#ADTRG/UPMUX/EXSVD1
50 P14 P14/BZOUT/UPMUX/EXSVD0
49 OSC2 OSC2
48 OSC1 OSC1
47 TEST TEST
46 VDD VDD
45 #RESET #RESET
44 VSS VSS
43 VD1 VD1
42 PD3 PD3/OSC4
41 PD2 PD2/OSC3
40 PD1 SWD/PD1
39 PD0 SWCLK/PD0
38 P07 P07/#BZOUT/UPMUX/ADIN06
37 P06 P06/EXOSC/UPMUX/ADIN05
36 P05 P05/RTC1S/UPMUX/ADIN04
35 P04 P04/CLPLS/UPMUX/ADIN03
34 P03 P03/REMO/UPMUX/ADIN02
33 P02 P02/EXCL10/UPMUX/ADIN01
32 P01 P01/EXCL00/UPMUX/ADIN00
31 P00 P00/UPMUX/VREFA0
30 P13 P13/SPICLK1/UPMUX
29 P12 P12/SDO1/UPMUX
28 P11 P11/SDI1/UPMUX
27 P10 P10/#SPISS1/UPMUX
26 USB_DP USB_DP
25 N.C. N.C.
24 USB_DM USB_DM
1 P47 P47/BLU0
2 P50 P50/BLU1
3 P51 P51/HCK
4 P52 P52/ENB
5 P53 P53
6 P54 P54/VST
7 P55 P55/XRST
8 P56 P56/VCK
9 VMDL VMDL
10 VMDH VMDH
11 VMD3 VMD3
12 VMD2 VMD2
13 CMD3 CMD3
14 CMD2 CMD2
15 CMD1 CMD1
16 VMVD1 VMVD1
17 N.C. N.C.
18 N.C. N.C.
19 USB33VOUT USB33VOUT
20 N.C. N.C.
21 USB18VOUT USB18VOUT
22 VBUS VBUS
23 VSS VSS
Y
X
(0, 0)
4.45 mm
4.45 mm

■ PIN DESCRIPTIONS

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

I/O:
- I = Input
- O = Output
- I/O = Input/output
- P = Power supply
- A = Analog signal
- Hi-Z = High impedance state

Initial state:
- I (Pull-up) = Input with pulled up
- I (Pull-down) = Input with pulled down
- Hi-Z = High impedance state
- O (H) = High level output
- O (L) = Low level output

Tolerant fail-safe structure:
- ✓ = Over voltage tolerant fail-safe type I/O cell included (see the "I/O Ports" chapter)
  The over voltage tolerant fail-safe type I/O cell allows interfacing without passing unnecessary current even if a voltage exceeding V_{DD} is applied to the port. Also unnecessary current is not consumed when the port is externally biased without supplying V_{DD}.

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
V_{DD}	V_{DD}	P	–	–	Power supply (+)
V_{SS}	V_{SS}	P	–	–	GND
V_{PP}	V_{PP}	P	–	–	Power supply for Flash programming
V_{D1}	V_{D1}	A	–	–	V_{D1} regulator output
V_{MVD1}	V_{MVD1}	A	–	–	MDC power supply booster capacitor connect pin
$C_{MD1–3}$	$C_{MD1–3}$	A	–	–	MDC power supply booster capacitor connect pins
$V_{MD2–3}$	$V_{MD2–3}$	A	–	–	MDC power supply booster output
V_{MDL}	V_{MDL}	P	–	–	Memory display drive voltage output (2.7 to 3.4 V) * I/O power supply (for P4 and P5 port groups) when MDC is not used
V_{MDH}	V_{MDH}	P	–	–	Memory display drive voltage output (4.4 to 5.05 V)
$HIFV_{DD}$	$HIFV_{DD}$	P	–	–	Host interface and I/O power supply (for P2 and P3 port groups)
OSC1	OSC1	A	–	–	OSC1 oscillator circuit input
OSC2	OSC2	A	–	–	OSC1 oscillator circuit output
TEST	TEST	I	I (Pull-down)	–	Test mode enable input
#RESET	#RESET	I	I (Pull-up)	–	Reset input
P00	P00	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	VREFA0	A			12-bit A/D converter Ch.0 reference voltage input
P01	P01	I/O	Hi-Z	–	I/O port
	EXCL00	I			16-bit PWM timer Ch.0 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN00	A			12-bit A/D converter Ch.0 analog signal input 0
P02	P02	I/O	Hi-Z	–	I/O port
	EXCL10	I			16-bit PWM timer Ch.1 event counter input 0
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN01	A			12-bit A/D converter Ch.0 analog signal input 1
P03	P03	I/O	Hi-Z	–	I/O port
	REMO	O			IR remote controller transmit data output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN02	A			12-bit A/D converter Ch.0 analog signal input 2
P04	P04	I/O	Hi-Z	–	I/O port
	CLPLS	O			IR remote controller clear pulse output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN03	A			12-bit A/D converter Ch.0 analog signal input 3
P05	P05	I/O	Hi-Z	–	I/O port
	RTC1S	O			Real-time clock 1-second cycle pulse output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN04	A			12-bit A/D converter Ch.0 analog signal input 4

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P06	P06	I/O	Hi-Z	–	I/O port
	EXOSC	I			Clock generator external clock input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN05	A			12-bit A/D converter Ch.0 analog signal input 5
P07	P07	I/O	Hi-Z	–	I/O port
	#BZOUT	O			Sound generator inverted output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	ADIN06	A			12-bit A/D converter Ch.0 analog signal input 6
P10	P10	I/O	Hi-Z	–	I/O port
	#SPISS1	I			Synchronous serial interface Ch.1 slave-select input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P11	P11	I/O	Hi-Z	–	I/O port
	SDI1	I			Synchronous serial interface Ch.1 data input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P12	P12	I/O	Hi-Z	–	I/O port
	SDO1	O			Synchronous serial interface Ch.1 data output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P13	P13	I/O	Hi-Z	–	I/O port
	SPICLK1	I/O			Synchronous serial interface Ch.1 clock input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P14	P14	I/O	Hi-Z	✓	I/O port
	BZOUT	O			Sound generator output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	EXSVD0	A			Supply voltage detector external voltage detection input 0
P15	P15	I/O	Hi-Z	✓	I/O port
	#ADTRG	I			12-bit A/D converter Ch.0 trigger input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
	EXSVD1	A			Supply voltage detector external voltage detection input 1
P16	P16 (ENVPP)	I/O	Hi-Z	–	I/O port (Flash programming control signal output)
	EXCL11	I			16-bit PWM timer Ch.1 event counter input 1
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P20	P20	I/O	Hi-Z	–	I/O port
	HIFCNF	I			Host interface configuration input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P21	P21	I/O	Hi-Z	–	I/O port
	#HIFCS	I			Indirect 8-bit host interface chip-select input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P22	P22	I/O	Hi-Z	–	I/O port
	#HIFRD	I			Indirect 8-bit host interface read input
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P23	P23	I/O	Hi-Z	–	I/O port
	#HIFWR (HSPICLK)	I			Indirect 8-bit host interface write input (SPI/QSPI host interface clock input)
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P24	P24	I/O	Hi-Z	–	I/O port
	#HIFDE (#HSPISS)	I			Indirect 8-bit host interface device enable input (SPI/QSPI host interface slave-select input)
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P25	P25	I/O	Hi-Z	–	I/O port
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P26	P26	I/O	Hi-Z	–	I/O port
	HIFD0 (HSPID0)	I/O			Indirect 8-bit host interface D0 input/output (SPI/QSPI host interface data input/output)
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P27	P27	I/O	Hi-Z	–	I/O port
	HIFD1 (HSPID1)	I/O			Indirect 8-bit host interface D1 input/output (SPI/QSPI host interface data input/output)
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P30	P30	I/O	Hi-Z	–	I/O port
	HIFD2 (HSPID2)	I/O			Indirect 8-bit host interface D2 input/output (SPI/QSPI host interface data input/output)
	UPMUX	I/O			User-selected I/O (universal port multiplexer)

Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P31	P31	I/O	Hi-Z	–	I/O port
	HIFD3 (HSPID3)	I/O			Indirect 8-bit host interface D3 input/output (SPI/QSPI host interface data input/output)
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P32	P32	I/O	Hi-Z	–	I/O port
	HIFD4 (HSPISEL0)	I/O			Indirect 8-bit host interface D4 input/output (SPI/QSPI host interface SPI mode-select input)
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P33	P33	I/O	Hi-Z	–	I/O port
	HIFD5 (HSPISEL1)	I/O			Indirect 8-bit host interface D5 input/output (SPI/QSPI host interface SPI mode-select input)
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P34	P34	I/O	Hi-Z	–	I/O port
	HIFD6	I/O			Indirect 8-bit host interface D6 input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P35	P35	I/O	Hi-Z	–	I/O port
	HIFD7	I/O			Indirect 8-bit host interface D7 input/output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P36	P36	I/O	Hi-Z	–	I/O port
	INTMDC	O			Host interface interrupt output
	UPMUX	I/O			User-selected I/O (universal port multiplexer)
P40	P40	I/O	Hi-Z	–	I/O port
	VCOM/FR (COM)	O			6-bit color panel interface VCOM/FRP output (SPI panel interface COM output)
P41	P41	I/O	Hi-Z	–	I/O port
	XFRP	O			6-bit color panel interface XFRP output
P42	P42	I/O	Hi-Z	–	I/O port
	HST (SCS, XCS)	O			6-bit color panel interface HST output (SPI panel interface SCS output, 8-bit parallel/3-/4-wire serial grayscale panel interface XCS output)
P43	P43	I/O	Hi-Z	–	I/O port
	RED0 (DOUT2)	O			6-bit color panel interface RED0 output (8-bit parallel grayscale panel interface DOUT2 output)
P44	P44	I/O	Hi-Z	–	I/O port
	RED1 (DOUT3)	O			6-bit color panel interface RED1 output (8-bit parallel grayscale panel interface DOUT3 output)
P45	P45	I/O	Hi-Z	–	I/O port
	GRN0 (DOUT4)	O			6-bit color panel interface GRN0 output (8-bit parallel grayscale panel interface DOUT4 output)
P46	P46	I/O	Hi-Z	–	I/O port
	GRN1 (DOUT5)	O			6-bit color panel interface GRN1 output (8-bit parallel grayscale panel interface DOUT5 output)
P47	P47	I/O	Hi-Z	–	I/O port
	BLU0 (DOUT6)	O			6-bit color panel interface BLU0 output (8-bit parallel grayscale panel interface DOUT6 output)
P50	P50	I/O	Hi-Z	–	I/O port
	BLU1 (DOUT7)	O			6-bit color panel interface BLU1 output (8-bit parallel grayscale panel interface DOUT7 output)
P51	P51	I/O	Hi-Z	–	I/O port
	HCK (DOUT1)	O			6-bit color panel interface HCK output (8-bit parallel grayscale panel interface DOUT1 output)
P52	P52	I/O	Hi-Z	–	I/O port
	ENB (SDO, XWR)	O			6-bit color panel interface ENB output (SPI panel interface SDO output, 8-bit parallel grayscale panel interface XWR output, 3-/4-wire serial grayscale panel interface SDO output)
P53	P53	I/O	Hi-Z	–	I/O port
P54	P54	I/O	Hi-Z	–	I/O port
	VST (SCLK, XRD, SCL)	O			6-bit color panel interface VST output (SPI panel interface SCLK output, 8-bit parallel grayscale panel interface XRD output, 3-/4-wire serial grayscale panel interface SCL output)
P55	P55	I/O	Hi-Z	–	I/O port
	XRST (A0)	O			6-bit color panel interface XRST output (4-wire serial grayscale panel interface A0 output)

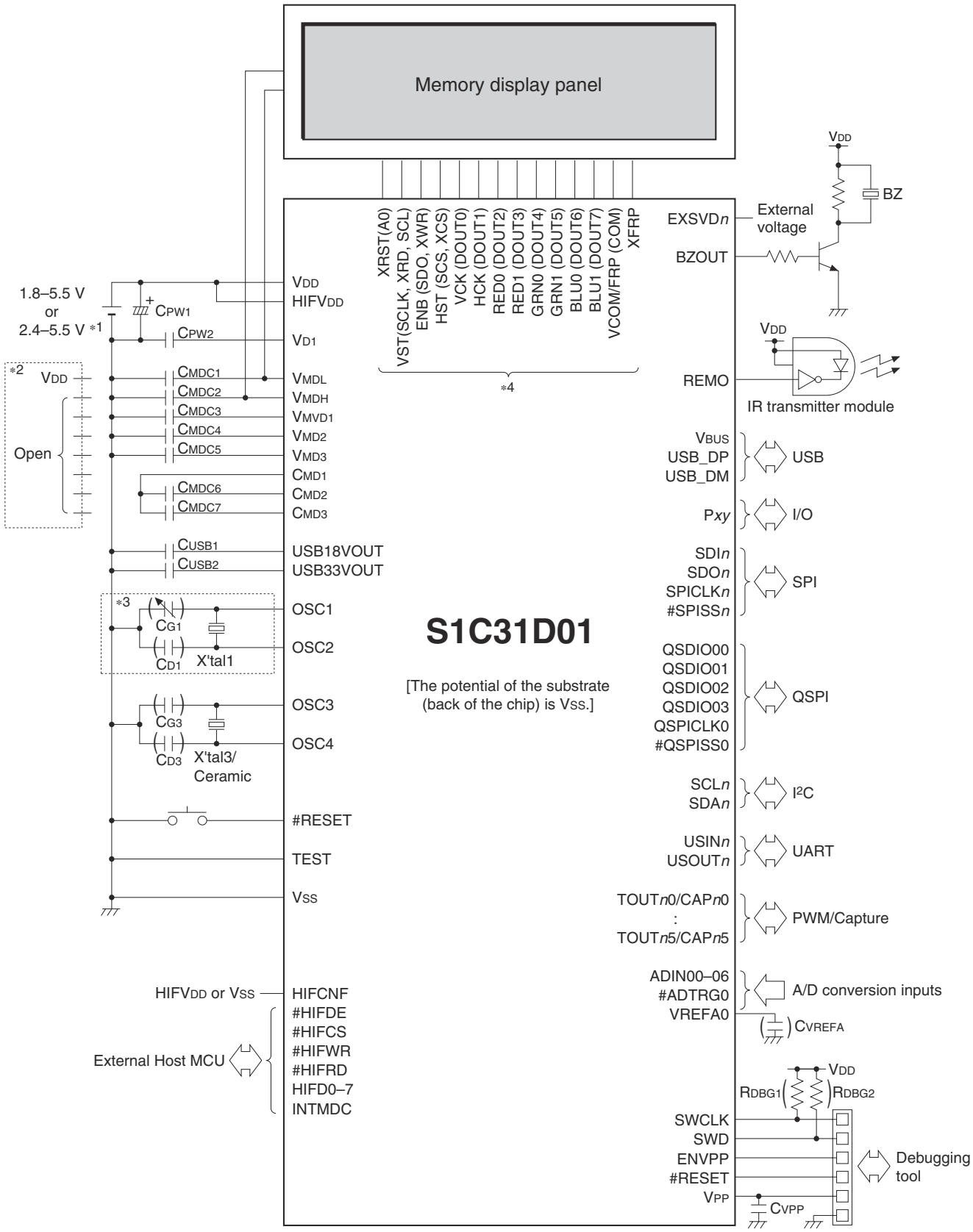
Pin name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function
P56	P56	I/O	Hi-Z	–	I/O port
	VCK (DOUT0)	O			6-bit color panel interface VCK output (8-bit parallel grayscale panel interface DOUT0 output)
P60	P60	I/O	Hi-Z	–	I/O port
	QSPICLK0	I/O			Quad synchronous serial interface Ch.0 clock input/output
P61	P61	I/O	Hi-Z	–	I/O port
	QSDIO00	I/O			Quad synchronous serial interface Ch.0 data input/output
P62	P62	I/O	Hi-Z	–	I/O port
	QSDIO01	I/O			Quad synchronous serial interface Ch.0 data input/output
P63	P63	I/O	Hi-Z	–	I/O port
	QSDIO02	I/O			Quad synchronous serial interface Ch.0 data input/output
P64	P64	I/O	Hi-Z	–	I/O port
	QSDIO03	I/O			Quad synchronous serial interface Ch.0 data input/output
P65	P65	I/O	Hi-Z	–	I/O port
	#QSPISS0	I/O			Quad synchronous serial interface Ch.0 slave-select input/output
P66	P66	I/O	Hi-Z	–	I/O port
	FOUT	O			Clock external output
P67	P67	I/O	Hi-Z	–	I/O port
	EXCL01	I			16-bit PWM timer Ch.0 event counter input 1
PD0	SWCLK	I	I (Pull-up)	–	Serial-wire debugger clock input
	PD0	I/O			I/O port
PD1	SWD	I/O	I (Pull-up)	–	Serial-wire debugger data input/output
	PD1	I/O			I/O port
PD2	PD2	I/O	Hi-Z	–	I/O port
	OSC3	A			OSC3 oscillator circuit input
PD3	PD3	I/O	Hi-Z	–	I/O port
	OSC4	A			OSC3 oscillator circuit output
USB_DP	USB_DP	I/O	I	–	USB D+ signal input/output
USB_DM	USB_DM	I/O	I	–	USB D- signal input/output
VBUS	VBUS	P	–	–	USB VBUS input (5 V input allowed)
USB18VOUT	USB18VOUT	P	–	–	USB 1.8 V regulator output
USB33VOUT	USB33VOUT	P	–	–	USB 3.3 V regulator output

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below. Note, however, that a function cannot be assigned to two or more pins simultaneously.

Peripheral circuit	Signal to be assigned	I/O	Channel number *n*	Function
I²C (I2C)	SCL*n*	I/O	*n* = 0, 1	I2C Ch.*n* clock input/output
	SDA*n*	I/O		I2C Ch.*n* data input/output
UART (UART3)	USIN*n*	I	*n* = 0–2	UART3 Ch.*n* data input
	USOUT*n*	O		UART3 Ch.*n* data output
Synchronous serial interface (SPIA)	SDI*n*	I	*n* = 0	SPIA Ch.*n* data input
	SDO*n*	O		SPIA Ch.*n* data output
	SPICLK*n*	I/O		SPIA Ch.*n* clock input/output
	#SPISS*n*	I		SPIA Ch.*n* slave-select input
16-bit PWM timer (T16B)	TOUT*n*0/CAP*n*0	I/O	*n* = 0–5	T16B Ch.*n* PWM output/capture input 0
	TOUT*n*1/CAP*n*1	I/O		T16B Ch.*n* PWM output/capture input 1

■ BASIC EXTERNAL CONNECTION DIAGRAM



*1: For Flash programming
*2: When the memory display controller is not used
*3: When OSC1 crystal oscillator is selected
*4: The pin configuration depends on the panel to be used.
( ): Do not mount components if unnecessary.

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