

# CD74HC132, CD74HCT132

## High Speed CMOS Logic Quad 2-Input NAND Schmitt Trigger

August 1997

### Features

- Unlimited Input Rise and Fall Times
- Exceptionally High Noise Immunity
- Typical Propagation Delay: 10ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 37\%$ ,  $N_{IH} = 51\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$
- Related Literature
  - CD54HC132F3A and CD54HCT132F3A Military Data Sheet, Document Number 3778

### Description

The Harris CD74HC132, CD74HCT132 each contain four 2-input NAND Schmitt Triggers in one package. This logic device utilizes silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 74HCT logic family is functionally pin compatible with the standard 74LS logic family.

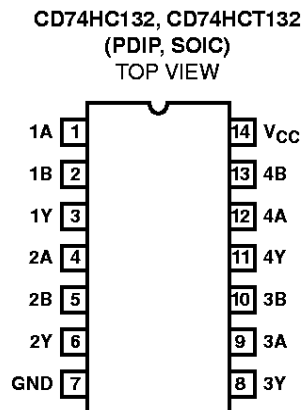
### Ordering Information

PART NUMBER	TEMP. RANGE ( $^\circ C$ )	PACKAGE	PKG. NO.
CD74HC132E	-55 to 125	14 Ld PDIP	E14.3
CD74HCT132E	-55 to 125	14 Ld PDIP	E14.3
CD74HC132M	-55 to 125	14 Ld SOIC	M14.15
CD74HCT132M	-55 to 125	14 Ld SOIC	M14.15

#### NOTE:

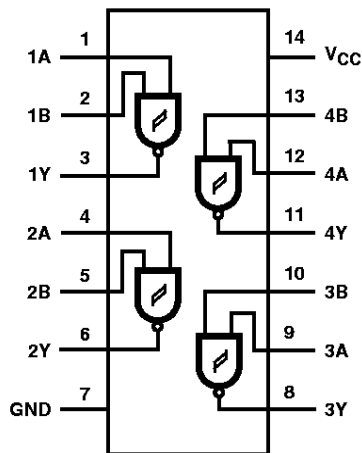
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinout



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### Functional Diagram

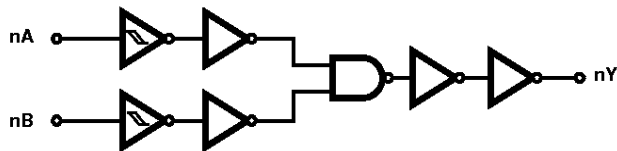


TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

NOTE: H = High Voltage Level, L = Low Voltage Level

### Logic Symbol



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### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	90
SOIC Package .....	175
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range ( $T_A$ ) .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	100ms (Max)
4.5V .....	100ms (Max)
6V .....	100ms (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
Input Switch Points (Note 6)	$V_{T+}$	-	-	2	0.7	-	1.5	0.7	1.5	0.7	1.5	V
				4.5	1.7	-	3.15	1.7	3.15	1.7	3.15	V
				6	2.1	-	4.2	2.1	4.2	2.1	4.2	V
	$V_{T-}$	-	-	2	0.3	-	1	0.3	1	0.3	1	V
				4.5	0.9	-	2.2	0.9	2.2	0.9	2.2	V
				6	1.2	-	3	1.2	3	1.2	3	V
	$V_H$			2	0.2	-	1	0.2	1	0.2	1	V
				4.5	0.4	-	1.4	0.4	1.4	0.4	1.4	V
				6	0.6	-	1.6	0.6	1.6	0.6	1.6	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{T+}$ or $V_{T-}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{T+}$ or $V_{T-}$	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V

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### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{T+}$ or $V_{T-}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Low Level Output Voltage TTL Loads												
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	2	-	20	-	40	μA
<b>HCT TYPES</b>												
Input Switch Points (Note 6)	$V_{T+}$	-	-	4.5	1.2	-	1.9	1.2	1.9	1.2	1.9	V
				5.5	1.4	-	2.1	1.4	2.1	1.4	2.1	V
	$V_{T-}$	-	-	4.5	0.5	-	1.2	0.5	1.2	0.5	1.2	V
				5.5	0.6	-	1.4	0.6	1.4	0.6	1.4	V
	$V_H$	-	-	4.5	0.4	-	1.4	0.4	1.4	0.4	1.4	V
				5.5	0.4	-	1.5	0.4	1.5	0.4	1.5	V
High Level Output Voltage CMOS Loads	-	$V_{T+}$ or $V_{T-}$	-	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{T+}$ or $V_{T-}$	-4	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			0.02	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ and GND	4	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	5.5	-	-	2	-	20	-	40	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	$\Delta I_{CC}$	$V_{CC} - 2.1$	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

**NOTE:**

4. For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.
5. Die for this part number is available which meets all electrical specifications.
6. Hysteresis definition, characteristic and test setup see Test Circuits and Waveforms:

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## HCT Input Loading Table

INPUT	UNIT LOADS
nA, nB	0.6

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g. 360 $\mu$ A max at 25°C.

## Switching Specifications Input $t_r, t_f = 6ns$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay A, B to Y (Figure 1)	$t_{PLH}, t_{PHL}$	$C_L = 50pF$	2	-	-	125	-	156	-	188	ns
			4.5	-	-	25	-	31	-	38	ns
			6	-	-	21	-	27	-	32	ns
Propagation Delay A, B to Y	$t_{TLH}, t_{THL}$	$C_L = 15pF$	5	-	10	-	-	-	-	pF	
Transition Times (Figure 1)	$t_{TLH}, t_{THL}$	$C_L = 50pF$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	$C_I$	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 7, 8)	$C_{PD}$	-	5	-	30	-	-	-	-	pF	
<b>HCT TYPES</b>											
Propagation Delay A, B to Y (Figure 2)	$t_{PHL}, t_{PHL}$	$C_L = 50pF$	4.5	-	-	33	-	41	-	50	ns
Propagation Delay A, B to Y	$t_{PLH}, t_{PHL}$	$C_L = 15pF$	5	-	13	-	-	-	-	-	pF
Transition Times (Figure 2)	$t_{TLH}, t_{THL}$	$C_L = 50pF$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	$C_I$	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 7, 8)	$C_{PD}$	-	5	-	30	-	-	-	-	-	pF

### NOTES:

- $C_{PD}$  is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## Test Circuits and Waveforms

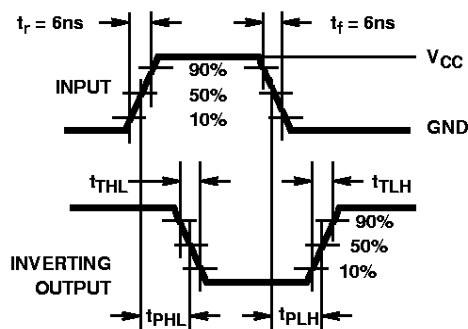


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

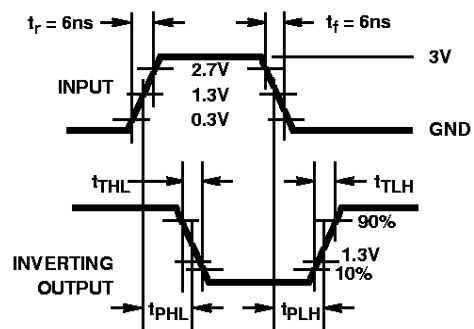


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

**Test Circuits and Waveforms**

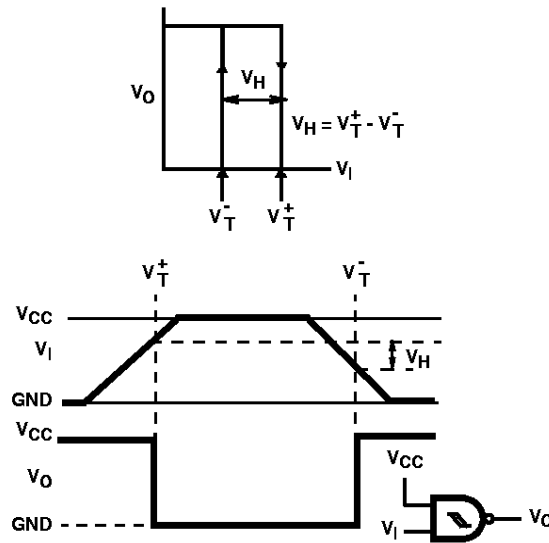


FIGURE 3. HYSTERESIS DEFINITION, CHARACTERISTIC, AND TEST SET-UP

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