application INFO available

Programmable Maximum Duty Cycle PWM Controller

FEATURES

- User Programmable Maximum PWM Duty Cycle
- 100μA Startup Current
- Operation to 1MHz
- Internal Full Cycle Soft Start
- Internal Leading Edge Blanking of Current Sense Signal
- 1A Totem Pole Output

DESCRIPTION

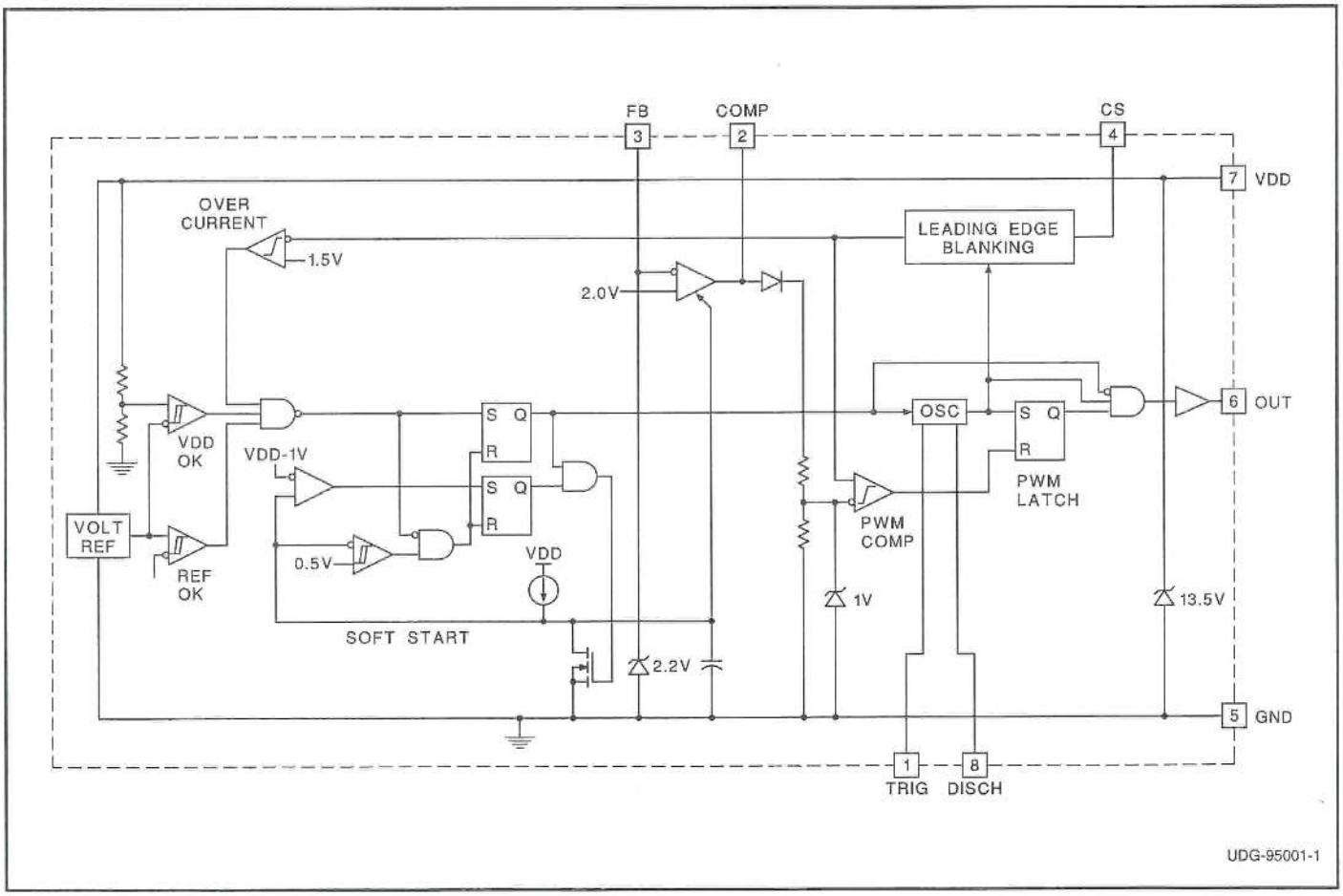
The UCC3807 family of high speed, low power integrated circuits contains all of the control and drive circuitry required for off-line and DC-to-DC fixed frequency current mode switching power supplies with minimal external parts count.

These devices are similar to the UCC3800 family, but with the added feature of a user programmable maximum duty cycle. Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor. The UCC3807 family also features internal full cycle soft start and internal leading edge blanking of the current sense input.

The UCC3807 family offers a variety of package options, temperature range options, and choice of critical voltage levels. The family has UVLO thresholds and hysteresis levels for off-line and battery powered systems. Thresholds are shown in the table below.

Part Number	Turn-on Threshold	Turn-off Threshold	Packages
UCCx807-1	7.2V	6.9V	J
UCCx807-2	12.5V	8.3V	N, D
UCCx807-3	4.3V	4.1V	N, D, PW

BLOCK DIAGRAM



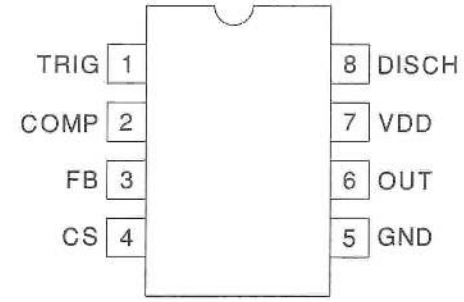
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (I_{DD} ≤10mA) 13.5V
Supply Current 30mA
OUT Current . . . . . ±1A
Analog Inputs (FB, CS) . . . . . –0.3V to (VDD + 0.3V)
Power Dissipation at T_A +25°C (N or J packages) 1W
Power Dissipation at T_A +25°C (D package) 0.65W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

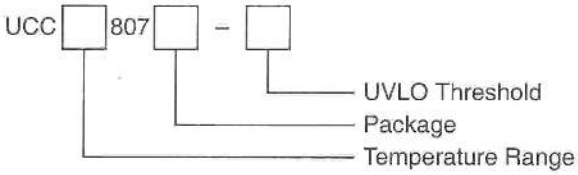
All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8, TSSOP-8 (Top View)
J, N, D or PW Packages



ORDERING INFORMATION



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1807-1/-2/-3; –40°C to +85°C for UCC2807-1/-2/-3; and 0°C to +70°C for UCC3807-1/-2/-3; VDD = 10V (Note 6), R_A = 12kΩ, R_B = 4.7kΩ, CT = 330pF, 1.0µF capacitor from VDD to GND, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section Section					
Frequency		175	202	228	kHz
Temperature Stability	(Note 5)		2.5		%
Amplitude	(Note 1)		1/3VDD		V
Error Amplifier Section					
Input Voltage	COMP = 2.0V	1.95	2.00	2.05	V
Input Bias Current		–1		1	µA
Open Loop Voltage Gain		60	80		dB
COMP Sink Current	FB = 2.2V, COMP = 1.0V	0.3	2.5		mA
COMP Source Current	FB = 1.3V, COMP = 4.0V	–0.2	–0.5		mA
PWM Section					
Maximum Duty Cycle		75	78	81	%
Minimum Duty Cycle	COMP = 0V			0	%
Current Sense Section					
Gain	(Note 2)	1.1	1.65	1.8	V/V
Maximum Input Signal	COMP = 5.0V (Note 3)	0.9	1.0	1.1	V
Input Bias Current		–200		200	nA
CS Blank Time		50	100	150	ns
Overcurrent Threshold		1.4	1.5	1.6	V
COMP to CS Offset	CS = 0V	0.55	1.1	1.65	V
Output Section					
OUT Low Level	I = 100mA		0.4	1	V
OUT High Level	I = –100mA, VDD - OUT		0.4	1	V
Rise/Fall Time	CL = 1nF (Note 5)		20	100	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1807-1/-2/-3; –40°C to +85°C for UCC2807-1/-2/-3; and 0°C to +70°C for UCC3807-1/-2/-3; VDD = 10V (Note 6), R_A = 12kΩ, R_B = 4.7kΩ, CT = 330pF, 1.0μF capacitor from VDD to GND, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout Section					
Start Threshold	UCCx807-1 (Note 4)	6.6	7.2	7.8	V
	UCCx807-2	11.5	12.5	13.5	V
	UCCx807-3	4.1	4.3	4.5	V
Minimum Operating Voltage After Start	UCCx807-1 (Note 4)	6.3	6.9	7.5	V
	UCCx807-2	7.6	8.3	9.0	V
	UCCx807-3	3.9	4.1	4.3	V
Hysteresis	UCCx807-1	0.1	0.3	0.5	V
	UCCx807-2	3.5	4.2	5.1	V
	UCCx807-3	0.1	0.2	0.3	V
Soft Start Section					
COMP Rise Time	FB = 1.8V, From 0.5V to 4.0V		4		ms
Overall Section					
Startup Current	VDD < Start Threshold (UCCx807-1,-3)		0.1	0.2	mA
	VDD < Start Threshold (UCCx807-2)		0.15	0.25	mA
Operating Supply Current	FB = 0V, CS = 0V, No Load (Note 7)		1.3	2.1	mA
VDD Zener Shunt Voltage	I_{DD} = 10mA	12.0	13.5	15.0	V
Shunt to Start Difference		0.5	1.0		V

Note 1: Measured at TRIG; signal minimum = 1/3 VDD, maximum = 2/3 VDD.

Note 2: Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$, $0 \le V_{CS} \le 0.8V$

Note 3: Parameter measured at trip point of latch with FB at 0V.
Note 4: Start Threshold and Zener Shunt thresholds track one another.
Note 5: Ensured by design. Not 100% tested in production.
Note 6: Adjust VDD above the start threshold before setting at 10V for UCC3807-2.
Note 7: Does not include current in external timing RC network.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3807 is a low output impedance, 2MHz operational amplifier. COMP can both source and sink current. The error amplifier is internally current limited, which allows zero duty cycle by externally forcing COMP to GND.

The UCC3807 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: Current sense input. There are two current sense comparators on the chip, the PWM comparator and an overcurrent comparator.

The UCC3807 also contains a leading edge blanking circuit, which disconnects the external CS signal from the current sense comparator during the 100ns interval immediately following the rising edge of the signal at the OUT pin. In most applications, no analog filtering is required on CS. Compared to an external RC filtering technique, leading edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero on-time of the OUT signal is directly affected by the leading edge blanking and the CS to OUT propagation delay.

The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft start cycle.

FB: The inverting input to the error amplifier. For best stability, keep connections to FB as short as possible and stray capacitance as small as possible.

GND: Reference ground and power ground for all functions of the part.

OUT: The output of a high current power driver capable of driving the gate of a power MOSFET with peak currents exceeding 1A. OUT is actively held low when VDD is below the UVLO threshold.

The high current power driver consists of MOSFET output devices in a totem pole configuration. This allows the output to switch from VDD to GND. The output stage also provides a very low impedance which minimizes overshoot and undershoot. In most cases, external Schottky clamp diodes are not required.

PIN DESCRIPTIONS (cont.)

TRIG/DISCH: Oscillator control pins. Trig is the oscillator timing input, which has an RC-type charge/discharge signal controlling the chip's internal oscillator. DISCH is the pin which provides the low impedance discharge path for the external RC network during normal operation. Oscillator frequency and maximum duty cycle are computed as follows:

$$frequency \approx \frac{1.4}{(R_A + 2R_B)C_T}$$

$$duty\ cycle \approx \frac{R_A + R_B}{R_A + 2R_B}$$

as shown in Figure 1.

For best performance, keep the lead from C_T to GND as short as possible. A separate ground connection for C_T is desirable. The minimum value of R_A is 10kΩ, the minimum value of R_B is 2.2kΩ, and the minimum value of C_T is 47pF.

VDD: The power input connection for this device. Total VDD current is the sum of quiescent current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from

$I_{OUT} = Qg \bullet F$, where F is frequency.

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible in parallel with an electrolytic capacitor.

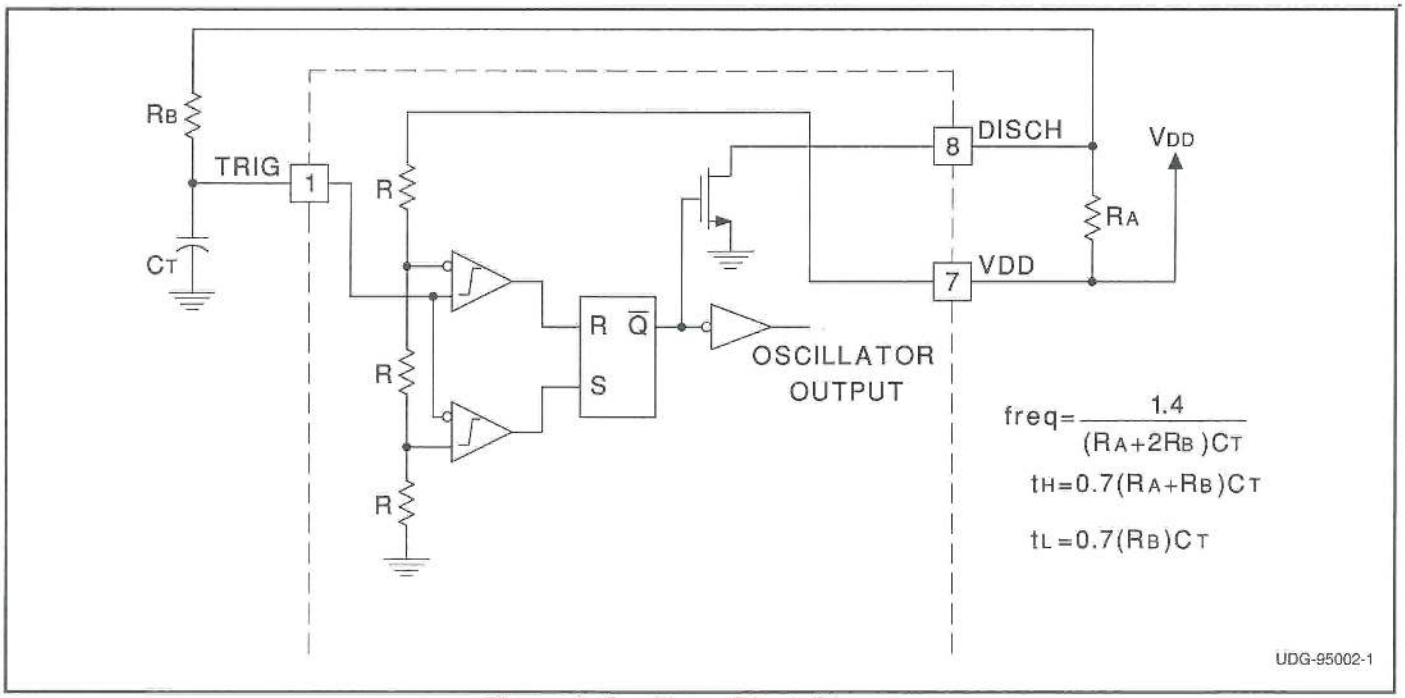


Figure 1. Oscillator Block Diagram

APPLICATIONS INFORMATION

The circuit shown in Fig. 2 illustrates the use of the UCC3807 in a typical off-line application. The 100W, 200kHz, universal input forward converter produces a regulated 12VDC at 8 Amps. The programmable maximum duty cycle of the UCC3807 allows operation down to 80VRMS and up to 265VRMS with a simple RCD clamp to limit the MOSFET voltage and provide core reset. In this application the maximum duty cycle is set to about 65%. Another feature of the design is the use of a flyback winding on the output filter choke for both bootstrapping and voltage regulation. This method of loop closure eliminates the optocoupler and secondary side regulator, common to most off-line designs, while providing good line and load regulation.

T1:	
Core	Magnetics Inc. #P-42625-UG (ungapped)
Primary:	28 turns of 2x #26AWG
Secondary:	6 turns of 50x0.2mm Litz wire
L1:	
Core:	Magnetics Inc. #P-42625-SG-37 (0.020" gap)
Main Winding:	13 turns of 2x #18AWG
Second Winding:	11 turns of #26AWG
Magnetics Inc.	
900 E. Butler Road P.O. Box 391 Butler, PA 16003 Tel: (412) 282-8282 Fax: (412) 282-6955	

APPLICATIONS INFORMATION (cont.)

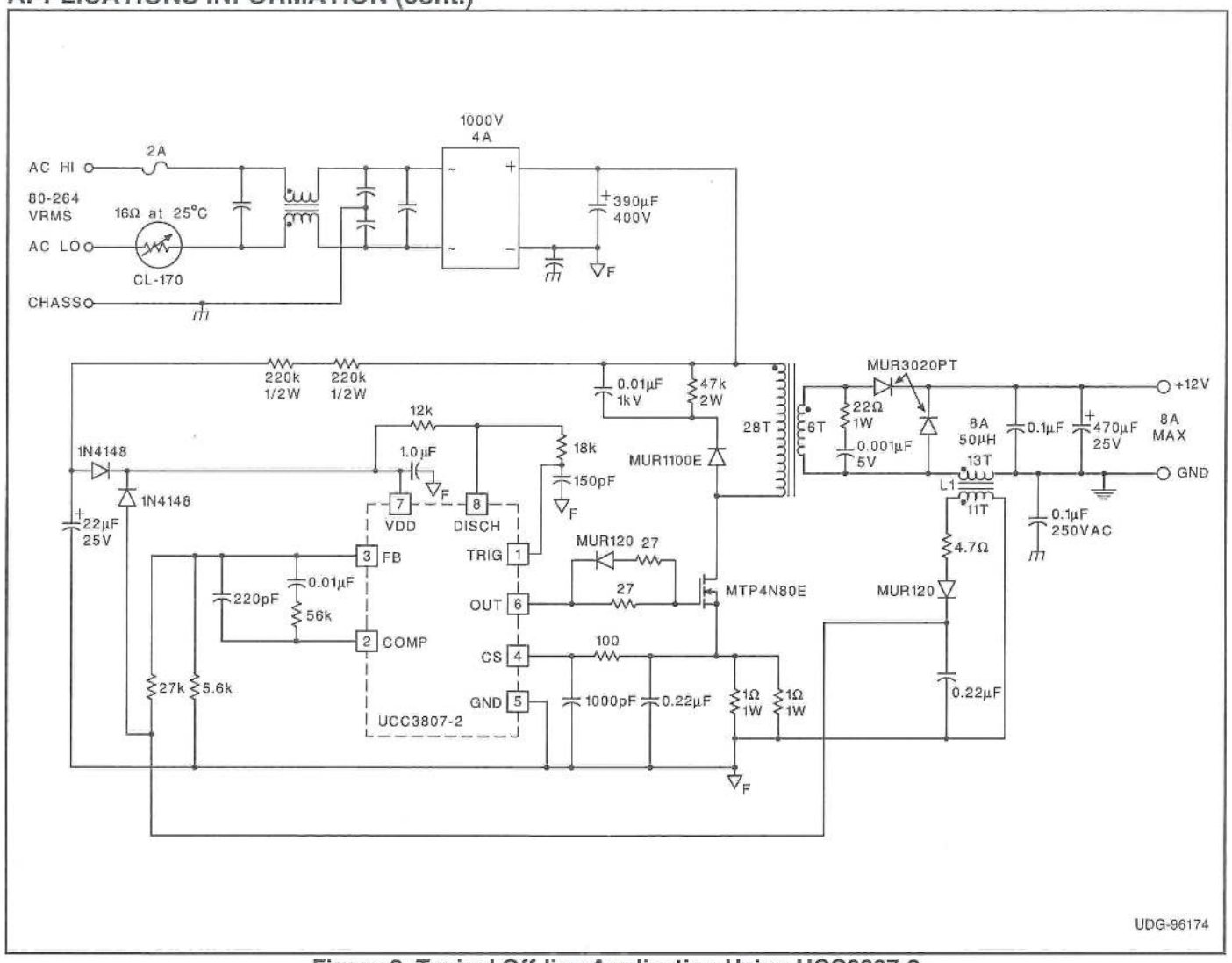


Figure 2. Typical Off-line Application Using UCC3807-2

APPLICATIONS INFORMATION (cont.)

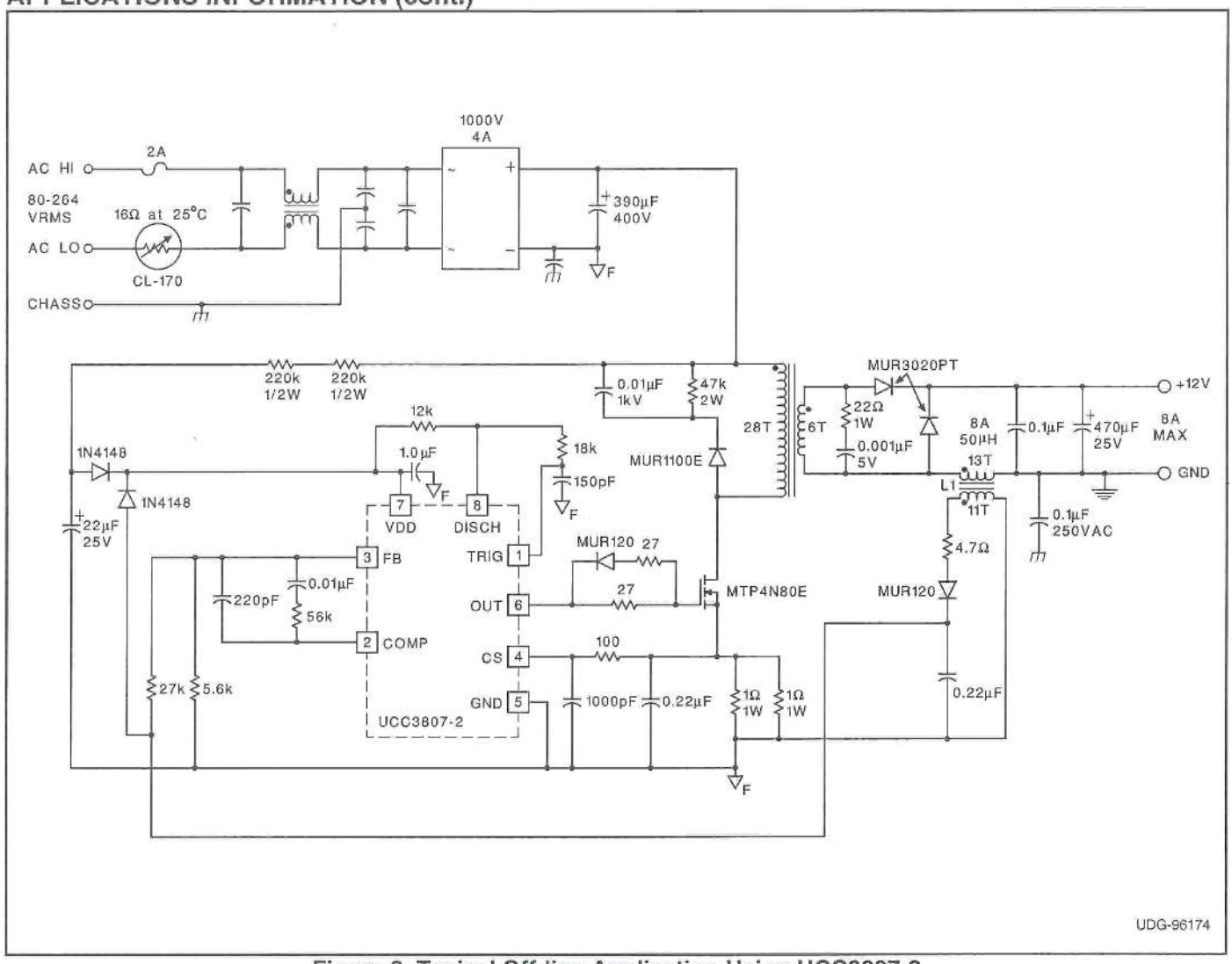


Figure 2. Typical Off-line Application Using UCC3807-2

REVISION HISTORY

SLUS163B, October 2010:

Updated missing symbols, no technical changes made.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2807D-1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2807-1	Samples
UCC2807D-2	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2807-2	Samples
UCC2807D-3	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2807-3	Samples
UCC2807D-3G4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2807-3	Samples
UCC2807DTR-1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2807-1	Samples
UCC2807DTR-2	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2807-2	Samples
UCC2807DTR-3	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2807-3	Samples
UCC3807D-1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	(3807-1, UCC3807) D-1	Samples
UCC3807D-2	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	(3807-2, UCC3807) D-2	Samples
UCC3807D-3	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	(3807-3, UCC3807) D-3	Samples
UCC3807DTR-3	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	(3807-3, UCC3807) D-3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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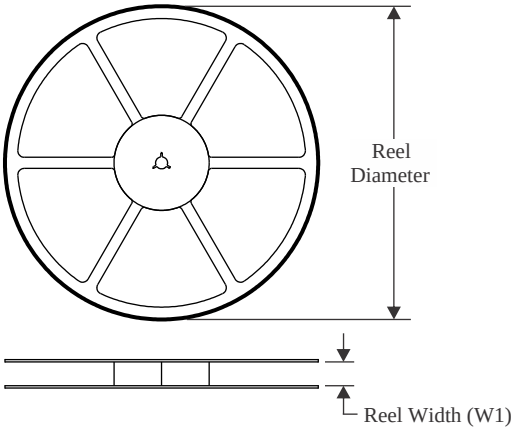
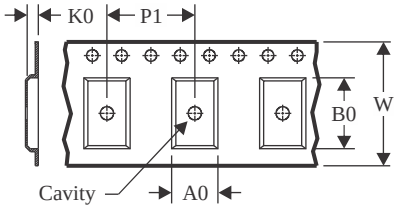
TAPE AND REEL INFORMATION

REEL DIMENSIONS

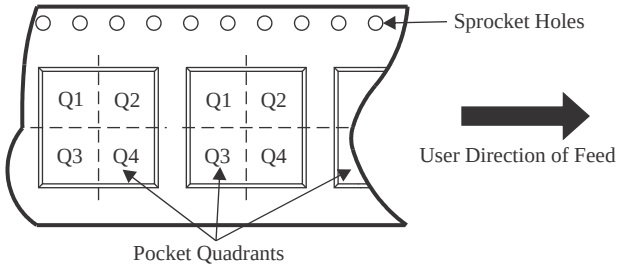


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

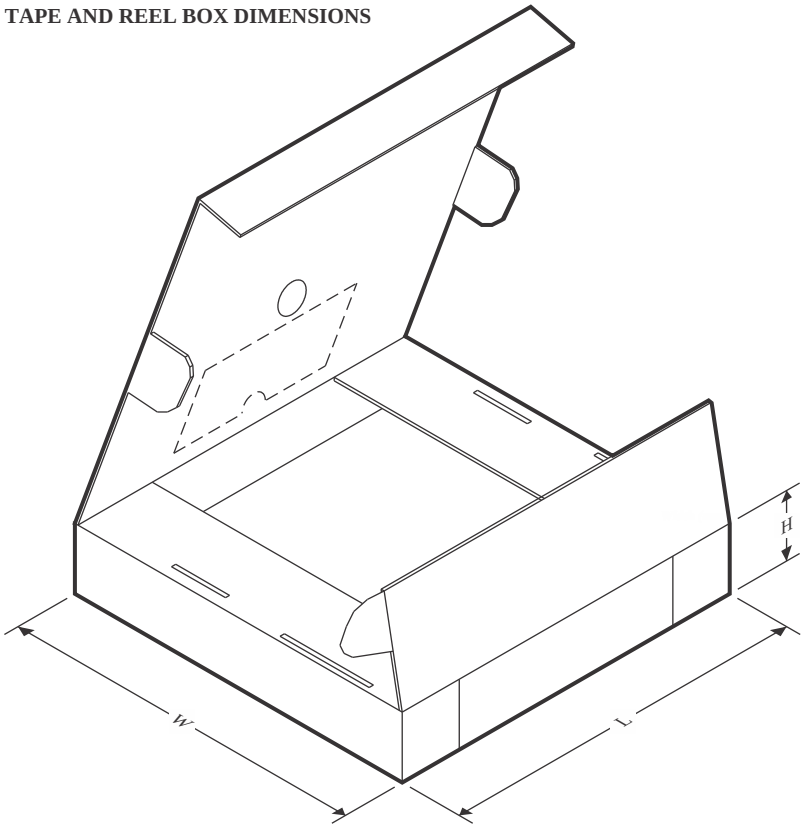
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2807DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2807DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2807DTR-3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3807DTR-3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

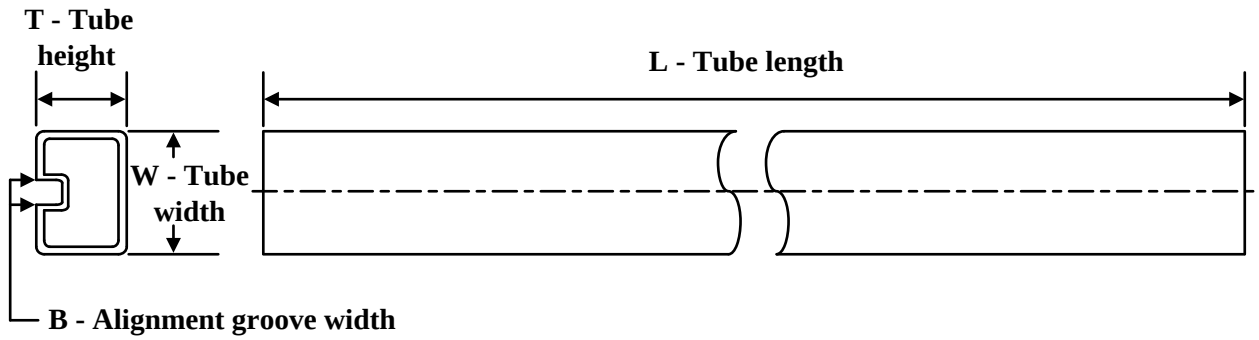
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

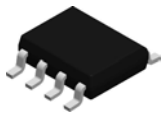
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2807DTR-1	SOIC	D	8	2500	356.0	356.0	35.0
UCC2807DTR-2	SOIC	D	8	2500	356.0	356.0	35.0
UCC2807DTR-3	SOIC	D	8	2500	356.0	356.0	35.0
UCC3807DTR-3	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC2807D-1	D	SOIC	8	75	506.6	8	3940	4.32
UCC2807D-2	D	SOIC	8	75	506.6	8	3940	4.32
UCC2807D-3	D	SOIC	8	75	506.6	8	3940	4.32
UCC2807D-3G4	D	SOIC	8	75	506.6	8	3940	4.32
UCC3807D-1	D	SOIC	8	75	506.6	8	3940	4.32
UCC3807D-2	D	SOIC	8	75	506.6	8	3940	4.32
UCC3807D-3	D	SOIC	8	75	506.6	8	3940	4.32

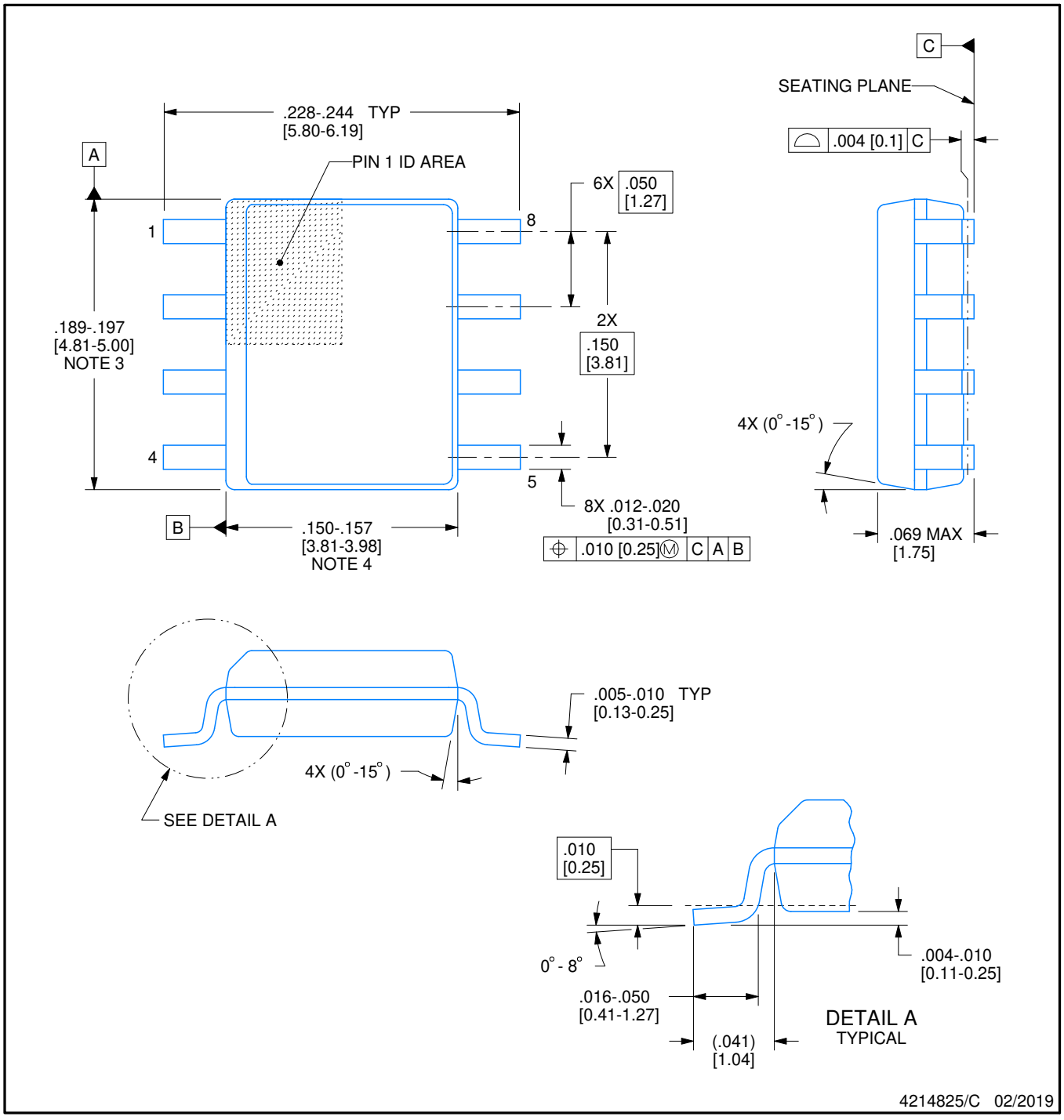


PACKAGE OUTLINE

D0008A

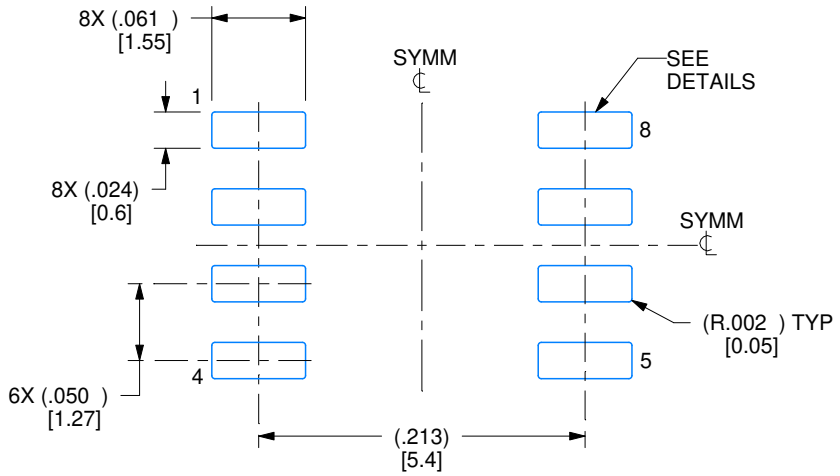
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

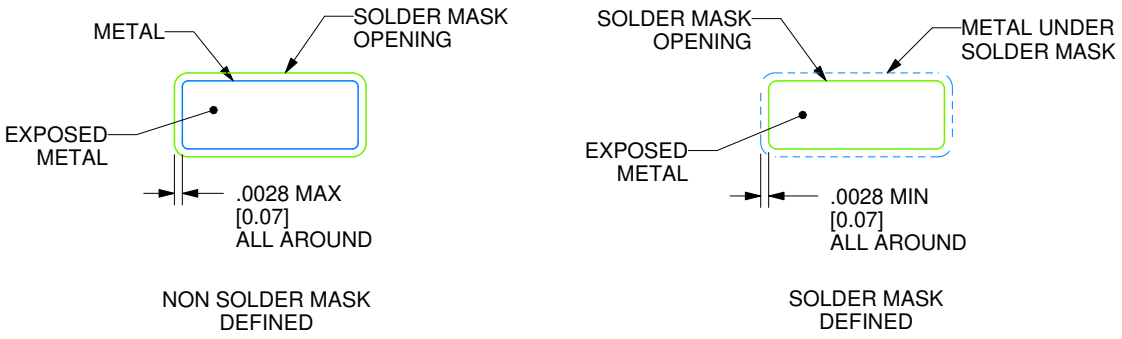


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

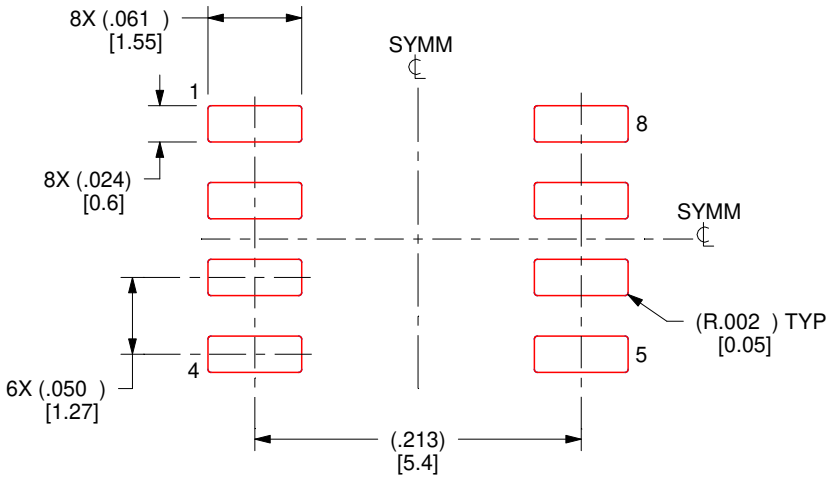
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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