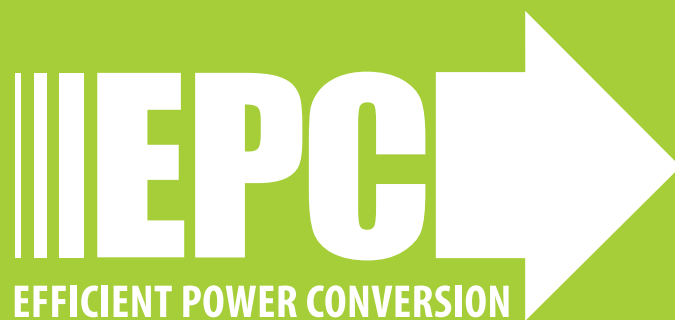


# Development Board EPC9084 Quick Start Guide

*350 V Half-Bridge with Gate Drive, Using EPC2050*

Revision 1.0



## DESCRIPTION

The EPC9084 development board, figure 1, is a 350 V maximum device voltage, 4 A maximum output current, half bridge with onboard gate drives, featuring two EPC2050 enhancement mode (eGaN®) field effect transistors (FETs). The purpose of this development board is to simplify the evaluation process of the EPC2050 eGaN FETs by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9084 development board is 1.5" x 2" and contains two EPC2050 eGaN FETs in a half bridge configuration. As supplied, the high side gate drive uses a digital isolator and both FETs use the Silicon Labs SI8274GB1-IM gate driver. The board also contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation, as well as the option to add trimmer resistors for adjustable deadtime to provide separate high and low side inputs, and an isolator for the low side gate drive. A block diagram of the circuit is given in figure 2.

For more information on the EPC2050 please refer to the datasheet available from EPC at [www.epc-co.com](http://www.epc-co.com). The datasheet should be read in conjunction with this quick start guide.

## QUICK START PROCEDURE

Development board EPC9084 is easy to set up to evaluate the performance of EPC2050 eGaN FETs. Refer to figure 3 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to +V<sub>IN</sub> (J5, J6) and ground / return to -V<sub>IN</sub> (J7, J8).
2. With power off, connect the switch node (SW) of the half bridge OUT (J3, J4) to your circuit as required (half bridge configuration).
3. With power off, connect the gate drive power supply to +V<sub>DD</sub> (J1, Pin-1) and ground return to -V<sub>DD</sub> (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7.5 V and 12 V range.
6. Turn on the controller / PWM input source.
7. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage) and probe switching node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

**Table 1: Performance Summary (T<sub>A</sub> = 25°C) EPC9084**

Symbol	Parameter	Conditions	Min	Max	Units
V <sub>DD</sub>	Gate Drive Input Supply Range		7.5	12	V
V <sub>IN</sub>	Bus Input Voltage Range <sup>(1)</sup>			280	V
I <sub>OUT</sub>	Switch Node Output Current <sup>(2)</sup>			4	A
V <sub>PWM</sub>	PWM Logic Input Voltage Threshold	Input 'High' Input 'Low'	3.5 0	6 1.5	V V
	Minimum 'High' State Input Pulse Width	V <sub>PWM</sub> rise and fall time < 10ns	200		ns
	Minimum 'Low' State Input Pulse Width <sup>(3)</sup>	V <sub>PWM</sub> rise and fall time < 10ns	500		ns

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 350 V for EPC2050.

(2) Maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermal cooling.

(3) Limited by time needed to 'refresh' high side bootstrap supply voltage.

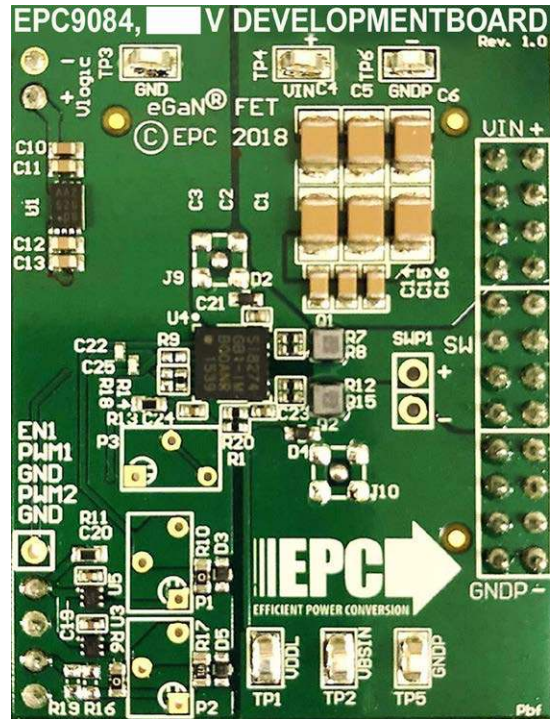


Figure 1: EPC9084 development board

**NOTE.** When measuring the high frequency content switch node, care must be taken to provide an accurate high speed measurement. An optional two pin header (SWP1) is included for switch node measurement. It is recommended to install measurement point on backside of board to prevent contamination of the top side components.

For information about measurement techniques, please review the how to GaN series: HTG09- Measurement

<http://epc-co.com/epc/DesignSupport/TrainingVideos/HowtoGaN/>

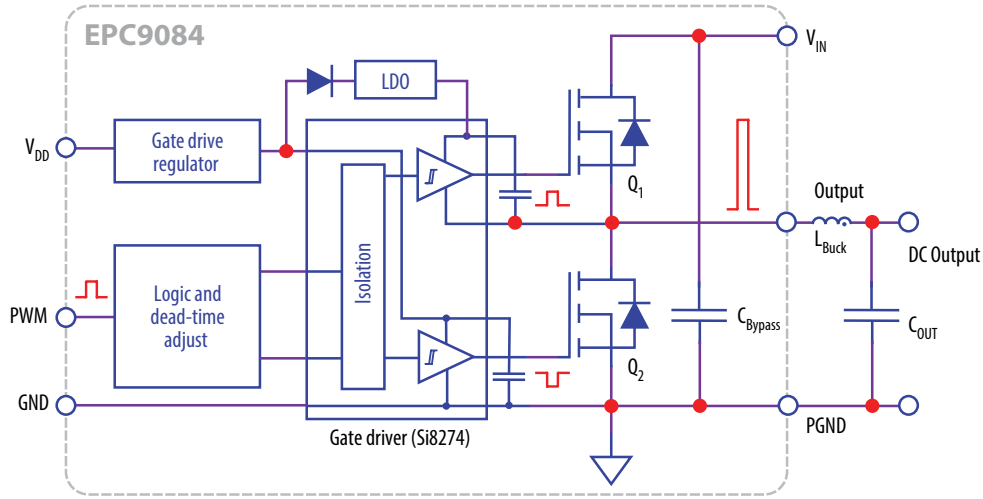


Figure 2: Block diagram of EPC9084 development board

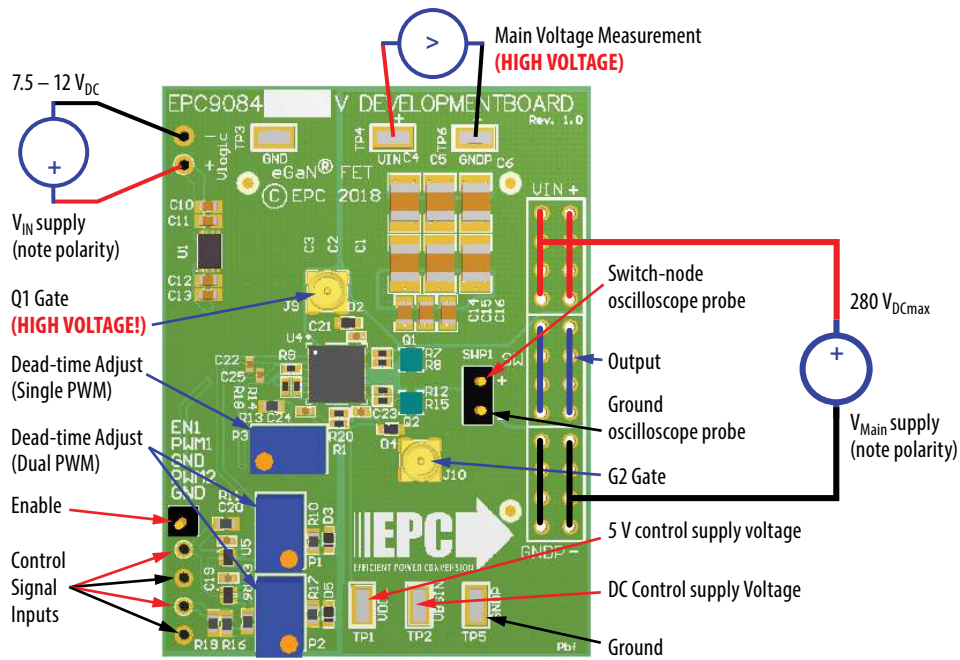
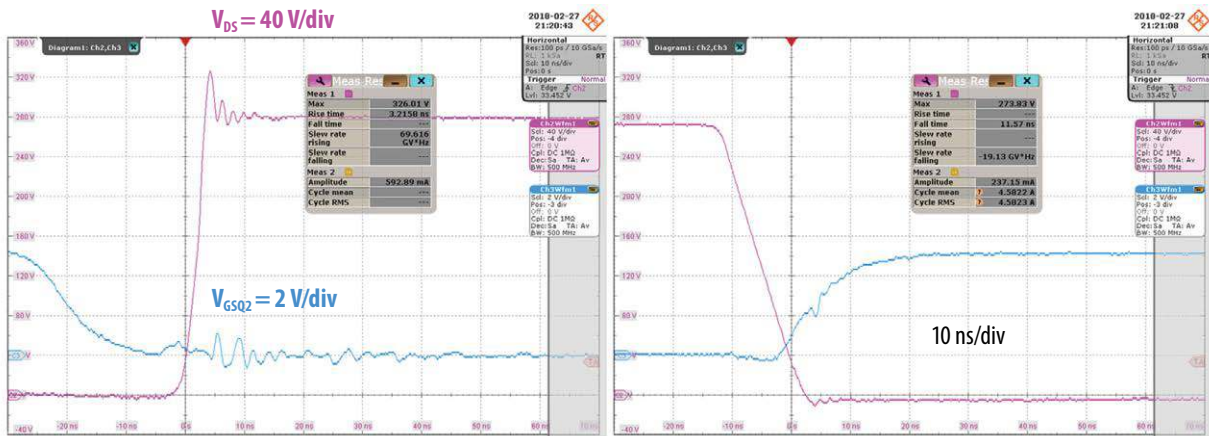


Figure 3: Proper connection and measurement setup



$V_{IN} = 280, V_{OUT} = 28 V, I_{OUT} = 4 A, f_{sw} = 50 kHz, L_{Buck} = 440 \mu H$

Figure 4: Typical Waveform for the EPC9084 operating as a buck converter

### MEASUREMENT CONSIDERATIONS

The EPC9084 development board has been provided with specially designed high frequency (up to 1 GHz minimum) capable measurement connections using MMCX connectors located at J9 & J10 with direct access to the gate signals of both the upper and lower FETs. These nodes can be measured directly using the Tektronix IsoVu probe shown in figure 4. Figure 5 shows typical gate waveforms measured using the IsoVu probe.



Figure 4: Tektronix IsoVu measurement setup

This native connection between the high and low side gate-source nodes to an IsoVu probe tip cable has less than 2 pF common mode loading and completely eliminates ground loops due to its galvanic isolation. These MMCX connectors (option not installed) offer a shielded coaxial environment to the test point which minimizes noise pickup.

Please contact EPC for special instructions on using these connections. To prevent an unterminated transmission line hanging on the gate it is recommended to remove resistors R21 & R22 when not using this feature. The maximum impedance loading of these nodes is 2.5 kΩ.

Tektronix is a leading manufacturer of power test solutions for design validation, characterization, and performance testing. EPC partnered with Tektronix to define the requirements for accurate measurements on GaN devices which led to the development of the Tektronix IsoVu measurement system. IsoVu is a galvanically isolated differential measurement system with 1 GHz bandwidth, 1 Million to 1 (120 dB) common mode rejection ratio, 50 V differential, and 2000 V common mode voltage range. Previously impossible differential measurements such as the high-side  $V_{GS}$  are now possible because of IsoVu's high common mode rejection across bandwidth.

IsoVu allows you to:

- Characterize the time alignment of high side and low side events
- Optimize and tune switching characteristics such as edge rates, overshoot, ringing and dead time
- See the interactions due to parasitic coupling between the high and low side transistors
- Make isolated high frequency current measurements using low impedance sense resistors
- Improve reliability through accurate characterization across all operating conditions

EPC would like to acknowledge Tektronix (<http://www.tek.com/isolated-measurement-systems>) for their support of this project.

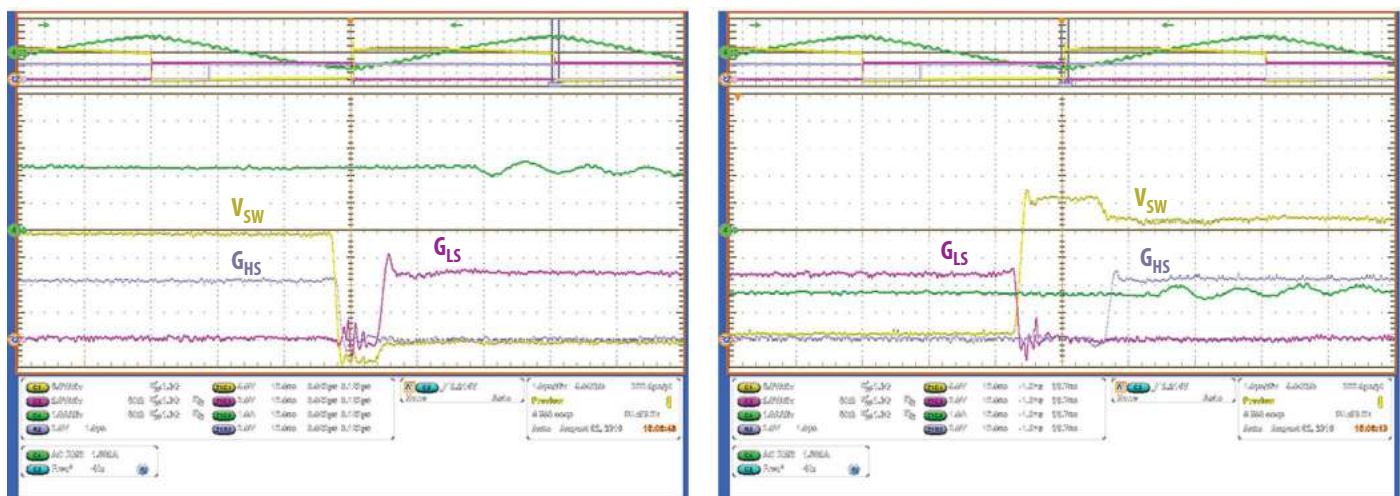


Figure 5: Upper gate and lower gate measurements using the Tektronix IsoVu and switch-node voltage measurement using the TPP1000 probe

## THERMAL CONSIDERATIONS

The EPC9084 development board showcases the EPC2050 eGaN FET. The EPC9084 is intended for bench evaluation with typical room ambient temperature. The addition of heat-sinking and forced air cooling can significantly increase the current capability of these devices, but care must be taken to not exceed the absolute maximum die temperature of 150° C.

**NOTE.** The EPC9084 development board does not have any current or thermal protection on board.

For more information regarding the thermal performance of EPC eGaN FETs, please consult:

D. Reusch and J. Glaser, *DC-DC Converter Handbook*, a supplement to *GaN Transistors for Efficient Power Conversion*, First Edition, Power Conversion Publications, 2015.

**Table 2: Bill of Materials**

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	4	C11, C12, C13, C17	Capacitor, 1 µF, 50 V	Taiyo Yuden UMK107AB7105KA-T
2	1	C10	Capacitor, 4.7 µF, 25 V	TDK C1608X5R1E475K080AC
3	2	C22, C25	Capacitor, 100 pF, 50 V	TDK CGA2B2C0G1H101J050BA
4	3	C14, C15, C16	Capacitor, 10 nF, 630 V	TDK C0805W103KBRAC7800
5	3	C18, C21, C23	Capacitor, 0.47 µF, 25 V	TDK C1005X5R1E474K050BB
6	3	C19, C20, C24	Capacitor, 0.22 µF, 16 V	TDK C1005X7R1C224K050BC
7	9	C1, C2, C3, C4, C5, C6, C7, C8, C9	Capacitor, 0.1 µF, 630 V	TDK CGA6L1X7T2J104K160AE
8	1	J1	Connector, .1" Male Vert.	Würth 61300211121
9	1	J7	Connector, .1" Male Vert.	Tyco 4-103185-0-04
10	2	TP1, TP2	SMD probe loop	Keystone 5015
11	4	TP3, TP4, TP5, TP6	SMD probe loop	Keystone 5015
12	2	D2, D4	Zener Diode, 5.61 V	On Semiconductor MM5Z5V6ST1G
13	2	D3, D5	Schottky Diode, 30 V, 30 mA	Diodes Inc. SDM03U40-7
14	2	Q1, Q2	eGaN FET, 350 V 4 A 150 mΩ	EPC EPC2050
15	5	R1, R3, R4, R14, R20	Resistor, 0 Ω	Panasonic ERJ-2GE0R00X
16	4	R7, R8, R12, R15	Resistor, 10 Ω	Panasonic ERJ-2RKF10R0X
17	1	U1	IC, 5.0 V 250mA DFN	Microchip MCP1703T-5002E/MC
18	1	U2	IC, 5 V 80 mA	Microchip MIC5213-5.0YC5
19	1	U3	IC, 2 In NAND	Fairchild NC7SZ00L6X
20	1	U5	IC, 2 In AND	Fairchild NC7SZ08L6X
21	1	R10	Resistor, 0 Ω	Stackpole ERJ-2GE0R00X
22	1	R11	Resistor, 10 k, 1%	Stackpole RMCF0603FT10K0
23	1	R13	Resistor, 8.2 k, 1%	Panasonic ERJ-3EKF8201V
24	1	R17	Resistor, 470 Ω, 1%	Stackpole RMCF0603FT470R
25	1	R6	Resistor, 0 Ω	Panasonic ERJ-3GEY0R00V
26	1	D1	Diode, 600 V 200 mA	ROHM RFU02VSM6STR
27	1	U4	DGTL ISO 2.5KV GATE DRIVE	Silicon Labs Si8274GB1-IM

**Table 3: Optional Components**

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	1	EN1	Connector, .1" Male Vert.	Würth, 61300111121
2	3	FD1, FD2, FD3	Sml Fiducial	N/A
3	6	J2, J3, J4, J5, J6, J8	Connector	N/A
4	2	J9, J10	MMCX SMD	Molex, 0734152063
5	4	R2, R5, R9, R18	Resistor, 0 Ω	Panasonic, ERJ-2GE0R00X
6	2	R16, R19	Optional 0603 Resistor	N/A
7	2	R21, R22	Resistor, 0 Ω	Stackpole, RMCF0402ZT0R00
8	3	P1, P2, P3	Optional Potentiometer	N/A
9	1	SWP1	Connector, .1" Male Vert.	Würth, 61300111121

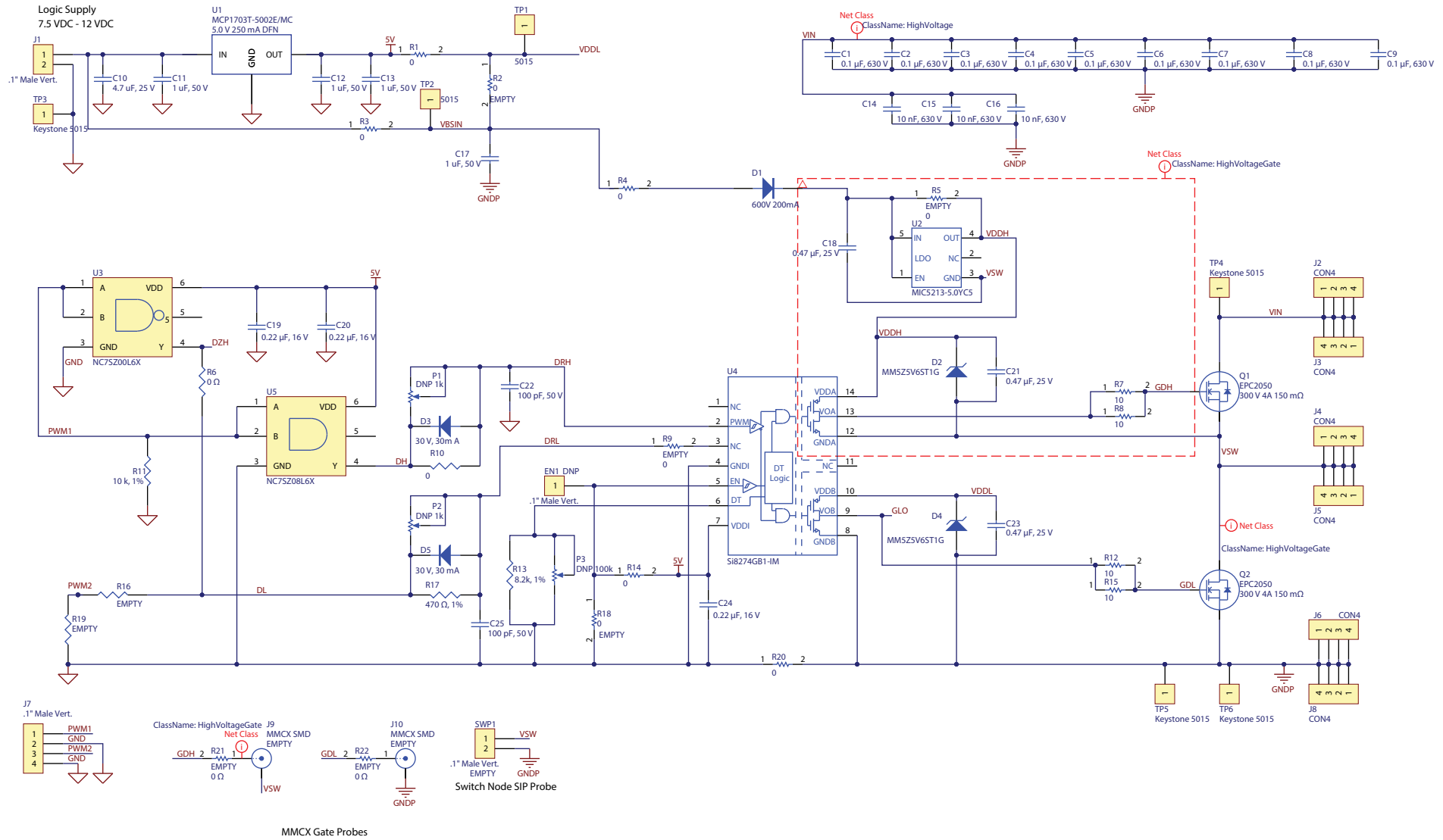


Figure 5: EPC9084 - Schematic

## For More Information:

Please contact [info@epc-co.com](mailto:info@epc-co.com)  
or your local sales representative

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