Low Power Multiclock Generator with VCFO
AK8135C

Features

- 24.576MHz Crystal Input
- One 24.576MHz-Reference Output
- Selectable Clock out Frequencies:
  - 24.576 MHz at CLK1
  - 24.99972 MHz at CLK2
  - 33.332965 MHz at CLK3
  - 74.1758, 74.250 MHz at CLK4
  - 36.864 MHz at CLK5
  - 27.000 MHz at REF1-3
- Built-in VCFO
  - Pull Range: ±96ppm (typ.)
- Low Jitter Performance
  - Period Jitter:
    150 psec (Typ.) at CLK2-3, REF1-3
    200 psec (Typ.) at CLK4-5
    300 psec (Typ.) at CLK1
  - Long term jitter:
    400 psec (Typ.) at CLK1-5, REF1-3
- Low Current Consumption:
  26 mA (Typ.) at 3.3V
- Low C/N output:
  72 dB (Typ.) at REF1-3
- Supply Voltage:
  3.0 – 3.6V
- Operating Temperature Range:
  -20 to +85°C
- Package:
  30-pin VSOP (Lead free)

Description

AK8135C is a member of AKM's low power multi clock generator family designed for Recorders, DTVs or STBs, requiring a range of system clocks with high performance. AK8135C generates different frequency clocks from a 24.576MHz crystal oscillator and provides them to seven outputs. The on-chip VCFO (Voltage Controlled Frequency Oscillator) accepts a voltage control input to allow the output clocks to vary by ±96 ppm for synchronizing to the external clock system. Both circuitries of VCFO and PLL in AK8135C are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption.
AK8135C is available in a 30-pin VSOP package.

Applications

- HDD, DVD, BD Recorder
- DTV
- Set-Top-Boxes

Block Diagram

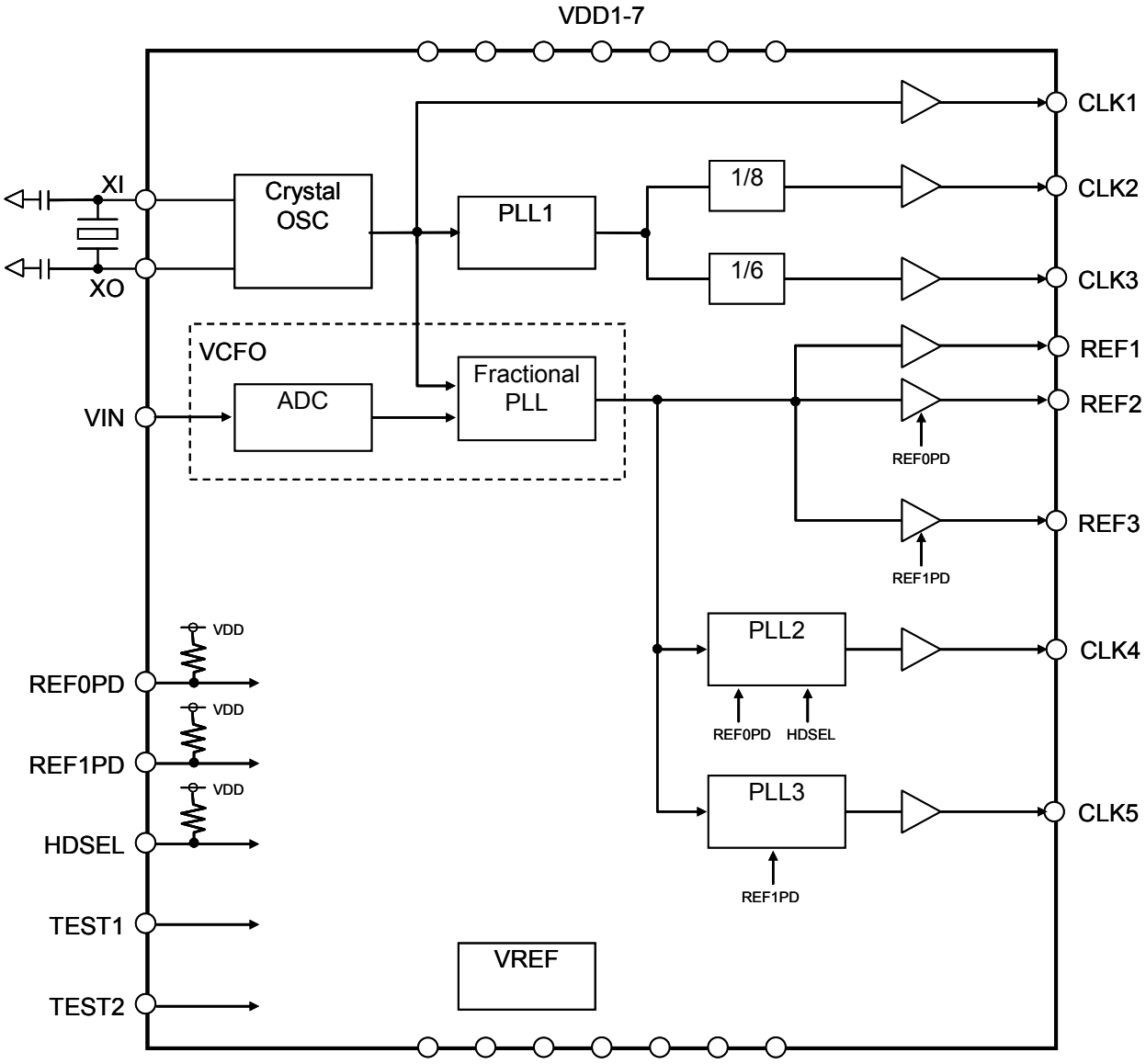


Figure 1: AK8135C Multi Clock Generator

Pin Descriptions

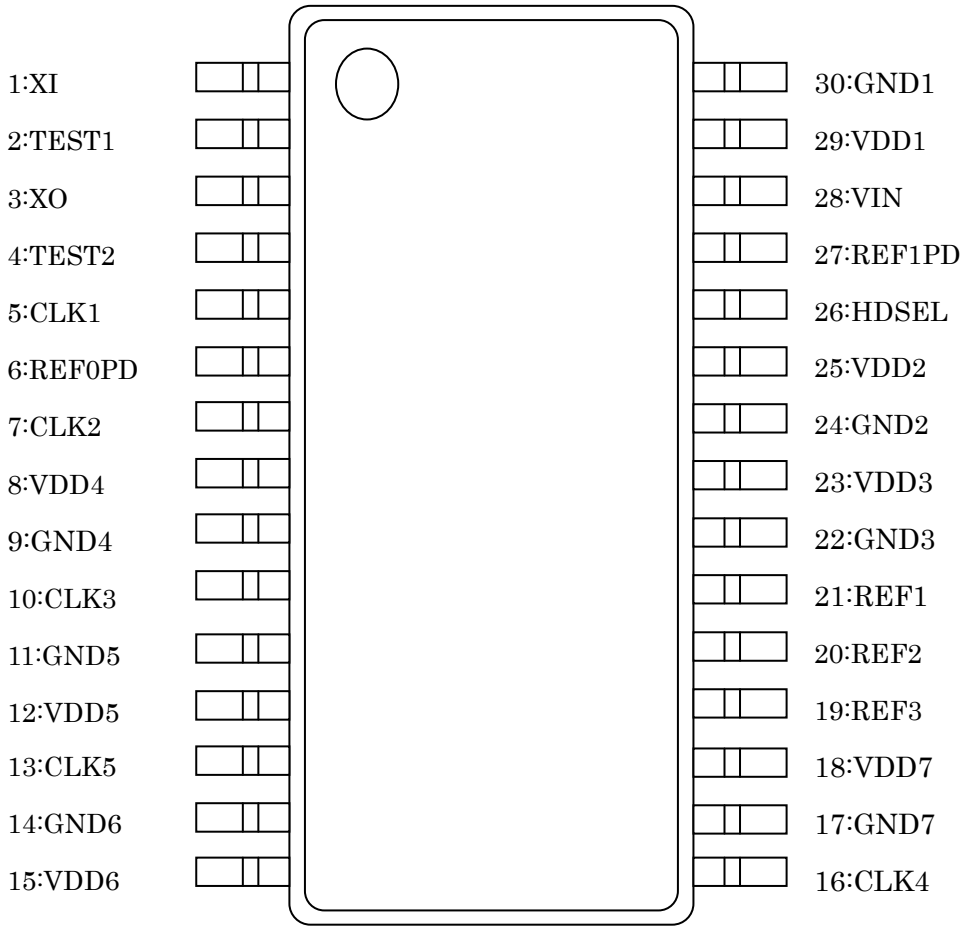


Figure 2: Package: 30-Pin VSOP(Top View)

Pin No.	Pin Name	Pin Type	Description
1	XI	AI	Crystal connection, Connect to 24.576MHz crystal
2	TEST1	DI	TEST input pin, Connect to GND.
3	XO	AO	Crystal connection, Connect to 24.576MHz crystal
4	TEST2	DI	TEST input pin, Connect to GND.
5	CLK1	DO	Reference Clock Output of XO based on 24.576MHz Crystal
6	REF0PD	DI	CLK4 and REF2 pins Mode Select pin, PLL2 Power Down pin "H": Enable, CLK4 and REF2 pins output Clock and PLL2 is Normal Operation. (1) "L": Disable, CLK4 and REF2 pins are "L" and PLL2 is powered down.
7	CLK2	DO	Clock output 2, Output frequency is 25.000MHz.
8	VDD4	PWR	Power Supply 4
9	GND4	PWR	Ground 4
10	CLK3	DO	Clock output 3, Output frequency is 33.333MHz.
11	GND5	PWR	Ground 5
12	VDD5	PWR	Power Supply 5
13	CLK5	DO	When REF1PD pin = "H", Clock output 5, Output frequency is 36.864MHz. When REF1PD pin = "L", CLK5 pin outputs "L".
14	GND6	PWR	Ground 6
15	VDD6	PWR	Power Supply 6
16	CLK4	DO	When REF0PD pin = "H" and HDSEL pin = "L", CLK4 pin outputs 74.1758MHz. When REF0PD pin = "H" and HDSEL pin = "H", CLK4 pin outputs 74.250MHz. When REF0PD pin = "L", CLK4 pin outputs "L".
17	GND7	PWR	Ground 7
18	VDD7	PWR	Power Supply 7
19	REF3	DO	When REF1PD pin = "H", Reference Clock Output 3 from VCFO, Output frequency is 27.000MHz. When REF1PD pin = "L", REF3 pin outputs "L".
20	REF2	DO	When REF0PD pin = "H", Reference Clock Output 2 from VCFO, Output frequency is 27.000MHz. When REF0PD pin = "L", REF2 pin outputs "L".
21	REF1	DO	Reference Clock Output 1 from VCFO, Output frequency is 27.000MHz.
22	GND3	PWR	Ground 3
23	VDD3	PWR	Power Supply 3
24	GND2	PWR	Ground 2
25	VDD2	PWR	Power Supply 2
26	HDSEL	DI	Mode Select pin for Output Frequency of CLK4 pin (1)
27	REF1PD	DI	CLK5 and REF3 pins Mode Select pin, PLL3 Power Down pin "H": Enable, CLK5 and REF3 pins output Clock and PLL3 is Normal Operation. (1) "L": Disable, CLK5 and REF3 pins are "L" and PLL3 is powered down.
28	VIN	AI	VCFO Control Voltage Input
29	VDD1	PWR	Power Supply 1
30	GND1	PWR	Ground 1

(1) Internal pull up 57kΩ

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8135C	AK8135C	Tape and Reel	30-pin VSOP	-20 to 85℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items Sy	mbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	VIN	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	IIN	± 10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter Sy	mbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-20		85	°C
Supply voltage(1)	VDD	Pin: VDD1-7	3.0	3.3	3.6	V
Output Load Capacitance	Cpl1	Pin: CLK1,2,4, REF2,3			15	pF
	Cpl2	Pin: CLK3,5, REF1			25	pF

Note:

(1) Power to VDD1-7 requires to be supplied from a single source. A decoupling capacitor for power supply line should be installed close to each VDD pin.

DC Characteristics

VDD: over 3.0 to 3.6V, Ta: -20 to +85℃, 24.576MHz Crystal, unless otherwise noted

Parameter Sy	mbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	Pin: REF0PD, REF1PD, HDSEL, TEST1,2	0.7VDD			V
Low Level Input Voltage	V_{IL}	Pin: REF0PD, REF1PD, HDSEL, TEST1,2			0.3VDD	V
Input Leak Current 1	I_L1	Pin: TEST1,2	-1		+1	μA
Input Leak Current 2	I_L2	Pin: REF0PD, REF1PD, HDSEL V_{IH}=VDD	-1		+1	μA
Input Leak Current 3	I_L3	Pin: REF0PD, REF1PD, HDSEL V_{IL}=GND	-97 -58		-25	μA
Input Leak Current 4	I_L4	Pin: VIN	-3		+3	μA
High Level Output Voltage	V_{OH}	Pin: CLK1-5, REF1-3 I_{OH}=-4mA	0.8VDD			V
Low level Output Voltage	V_{OL}	Pin: CLK1-5, REF1-3 I_{OL}=+4mA			0.2VDD	V
Current Consumption 1	$I_{DD}1$	No load REF0PD='H', REF1PD='H'	26		35	mA
Current Consumption 2	$I_{DD}2$	No load REF0PD='L', REF1PD='H'	19		26	mA
Current Consumption 3	$I_{DD}3$	No load REF0PD='H', REF1PD='L'	21		28	mA
Current Consumption 4	$I_{DD}4$	No load REF0PD='L', REF1PD='L'	14		19	mA

AC Characteristics

VDD: over 3.0 to 3.6V, Ta: -20 to +85℃, 24.576MHz Crystal, unless otherwise noted

Parameter Sy	mbol	Conditions	MIN	TYP	MAX	Unit
Crystal Clock Frequency (1)	F_{osc} Pin:XI,	XO		24.576		MHz
Output Clock Accuracy (1)	$F_{accuracy}$	Pin:CLK1 24.576MHz Crystal CL=8[pF]	-30	0 +	30	ppm
		Pin:CLK2 24.99972MHz Relative to 25.000MHz Crystal CL=8[pF]	-41	-11 +	19	ppm
		Pin:CLK3 33.332965MHz Relative to 33.333MHz Crystal CL=8[pF]	-41	-11	+19	ppm
		Pin:REF1-3 27.000MHz VIN=0.5VDD Crystal CL=8[pF]	-30	0 +	30	ppm
VCFO Pullable Range	PR_{VCFO}	Pin:REF1-3 VIN=0.5VDD±1.0	±75	±96 ±11	1	ppm
VCXO Response Time	RT_{VCXO}	Pin:REF1-3 VIN=0.5VDD±1.0	5	40		ppm/10 0ms
C/N CN		Pin:REF1 with Load Cpl2=25pF	72			dB
		Pin:REF2,3 with Load Cpl2=15pF	72			dB
Output Clock Rise Time 1	$T_{\_rise1}$	Pin:CLK1,2,4 REF2,3 with Load Cpl1=15pF 0.2VDD → 0.8VDD	1.5		4.0	ns
Output Clock Fall Time 1	$T_{\_fall1}$	Pin:CLK1,2,4 REF2,3 with Load Cpl1=15pF 0.8VDD → 0.2VDD	1.5		4.0	ns
Output Clock Rise Time 2	$T_{\_rise2}$	Pin:CLK3,5, REF1 with Load Cpl2=25pF 0.2VDD → 0.8VDD	2.5		4.0	ns
Output Clock Fall Time 2	$T_{\_fall2}$	Pin:CLK3,5, REF1 with Load Cpl2=25pF 0.8VDD → 0.2VDD	2.5		4.0	ns
Period Jitter (2) Jit	_period	Pin:CLK1 with Load Cpl1=15pF		300 (6 σ)	500 (6 σ)	ps
		Pin:CLK2, REF2,3 with Load Cpl1=15pF		150 (6 σ)	300 (6 σ)	ps
		Pin:CLK3, REF1 with Load Cpl1=25pF		150 (6 σ)	300 (6 σ)	ps
		Pin:CLK4 with Load Cpl1=15pF		200 (6 σ)	400 (6 σ)	ps
		Pin:CLK5 with Load Cpl2=25pF		200 (6 σ)	400 (6 σ)	ps
Long Term Jitter (2) Jit	_long	Pin:CLK1,2,4, REF2,3 with Load Cpl1=15pF 1000 cycle delay		400 (6 σ)	600 (6 σ)	ps
		Pin:CLK3,5, REF1 with Load Cpl2=25pF 1000 cycle delay		400 (6 σ)	600 (6 σ)	ps
Output Clock Duty Cycle	DtyCyc	Pin:CLK1 with Load Cpl1=15pF	40	50 60		%
		Pin:CLK2,4, REF2,3 with Load Cpl2=15pF	45	50 55		%
		Pin: CLK3,5, REF1 with Load Cpl1=25pF	45	50 55		%

Parameter Sy	mbol	Conditions	MIN	TYP	MAX	Unit
Power-up Time (3)	$T_{\_put}$	Pin:CLK1,2,4, REF2,3 with Load Cpl1=15pF		1	2	ms
		Pin:CLK3,5, REF1 with Load Cpl2=25pF	1		2	ms
Output Lock Time (4)	$T_{\_lock}$	Pin:CLK 4		60		µs

(1) Output Clock Accuracy depends on crystal characteristics, on-chip load capacitance, and stray capacity of PCB. MIN., Max.=±30ppm is applied to AKM's authorized test condition.
Please contact us when you plan the use of other crystal unit.

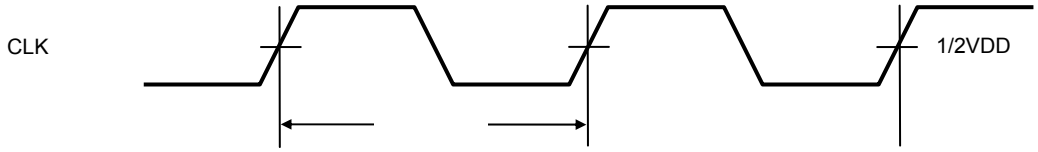
(2) $\pm 3\sigma$ in 10000 sampling or more

(3) Time to settle output into ±0.1% of specified frequency from the point that the power supply reaches VDD.

(4) Time to settle output into ±20ppm of specified frequency from the point that the HDSEL is switched.

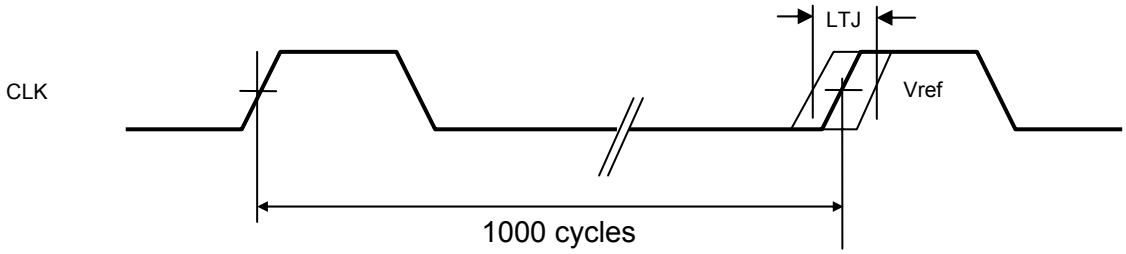
Definition of Jitter

1. Period Jitter (AC Characteristics)



PJ = t_{cyclen} - 1 / f0 : where f0 is the nominal output frequency and *t*cycle n is any cycle within the sample measured on controlled edges

2. Long Term Jitter (AC Characteristics)



1000Cycles after oscilloscope trigger.

Function Description

Voltage Controlled Frequency Oscillator (VCFO)

AK8135C has a voltage controlled frequency oscillator (VCFO), featuring fine frequency tuning for 27MHz of primary clock frequency by external DC voltage control. This tuning enables output clock frequency to synchronize the external clock system.
VCFO is composed of analog-to-digital converter and high resolution PLL as shown in Figure 3. VIN (Pin28) accepts DC voltage control from a processor or a system controller, and pulls the primary frequency of crystal to higher or lower. This pulling range is determined by supply Voltage to AK8135C. AK8135C is designed to range ± 96ppm of primary frequency, and the typical pulling profile is shown in **Figure 4**.

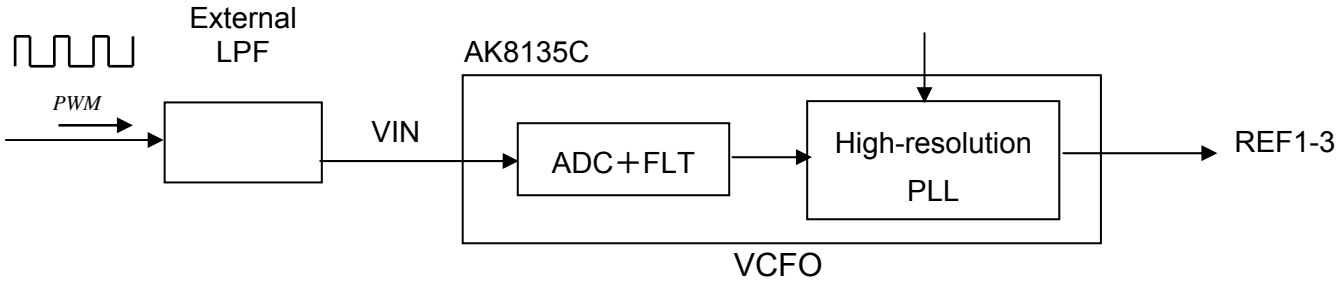


Figure 3: VCFO Diagram

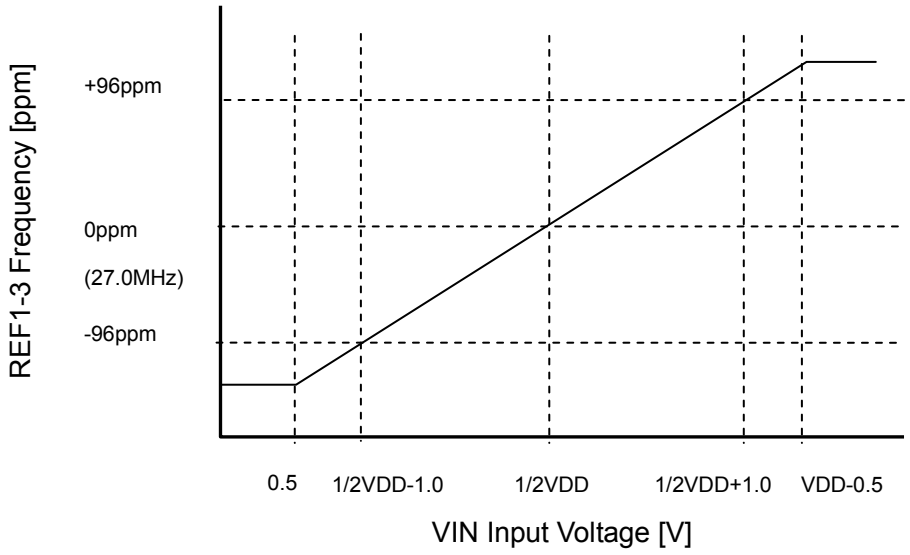


Figure 4: Typical VCFO Pulling Profile

Typical Connection Diagram

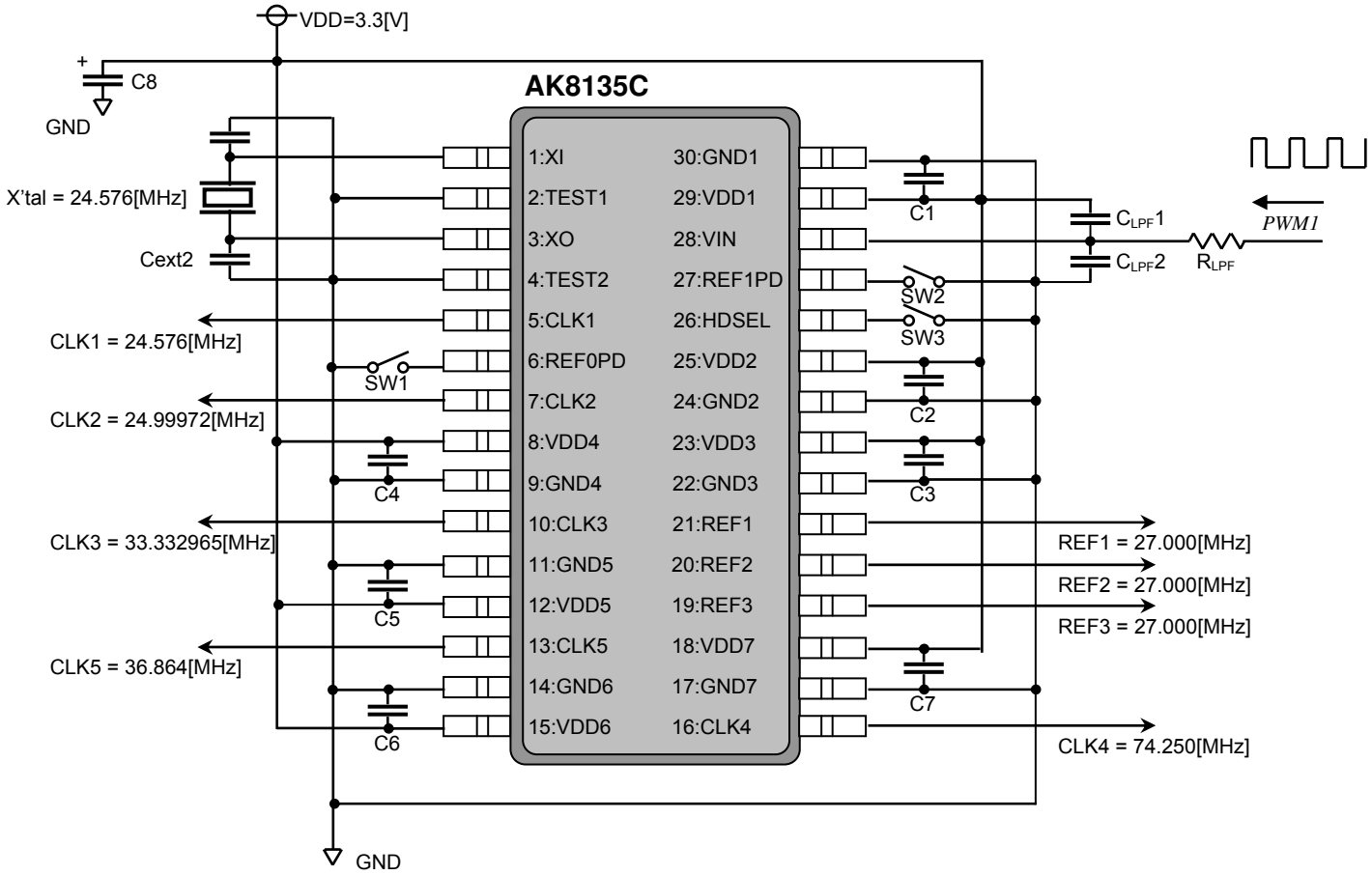


Figure 5: Typical Connection Diagram

C1, C2, C3, C4, C5, C6, C7: 0.1μF
C8 : Electrolytic capacitor
Cext1, Cext2: Depends on crystal characteristics. Refer the specification of the crystal.
SW1, SW2, SW3: These are switche s that c ontrol outputs of CLK4, CLK5, REF2 and REF3 and power up/down of PLL2 and PLL3.
R_{LPF}, $C_{LPF}1$, $C_{LPF}2$: In case of interface by PWM. For right configuration, refer the specification of the applied processor.

PCB Layout Consideration

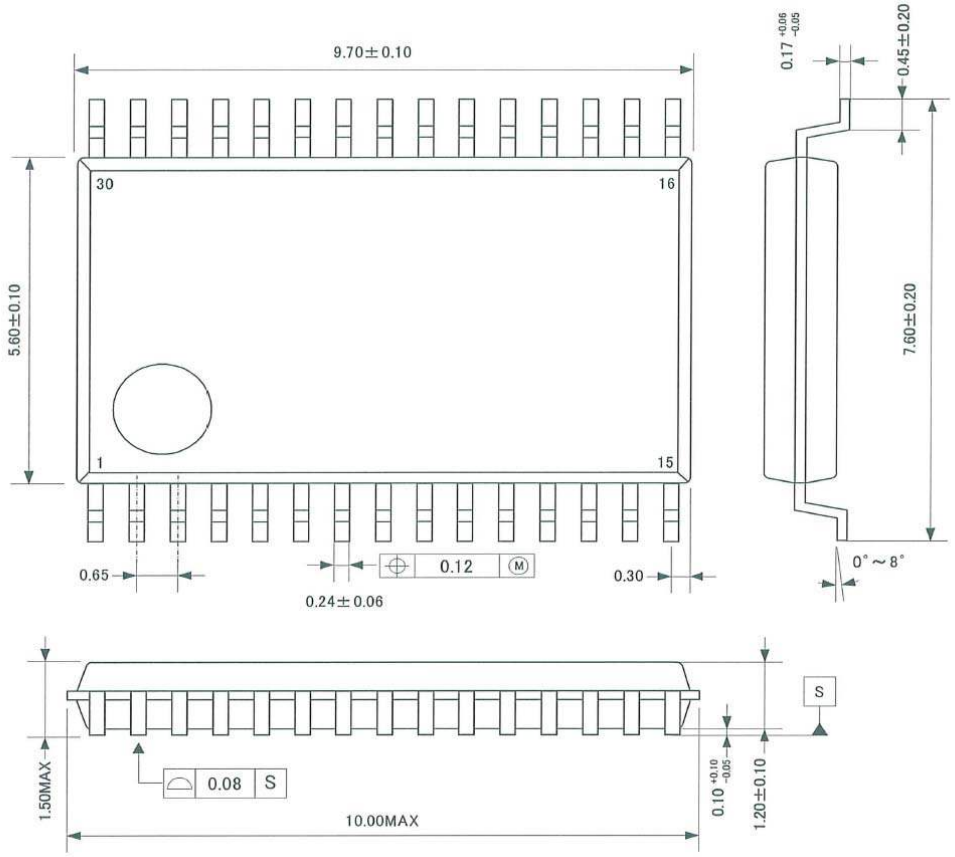
AK8135C is a high-accuracy and low-jitter multi clock generator. For proper performances specified in this datasheet, careful PCB layout should be taken. The followings are layout guidelines based on the typical connection diagram shown in Figure 5

Power supply line – AK8135C has seven power supply pins (VDD1-7) which deliver power to internal circuitry segments. A 0.1μF decoupling capacitor should be placed as close to each VDD pin as possible.

Ground pin connection – AK8135C has seven ground pins (GND1-7). These pin require connecting to plane ground which will eliminate any common impedance with other critical switching signal return. 0.1μF decoupling capacitors placed at VDD1, VDD2, VDD3, VDD4, VDD5, VDD6, and VDD7 should be grounded at close to the GND1pin, the GND2 pin, the GND3 pin, the GND4 pin, the GND5 pin, the GND6 pin, and the GND7 respectively.

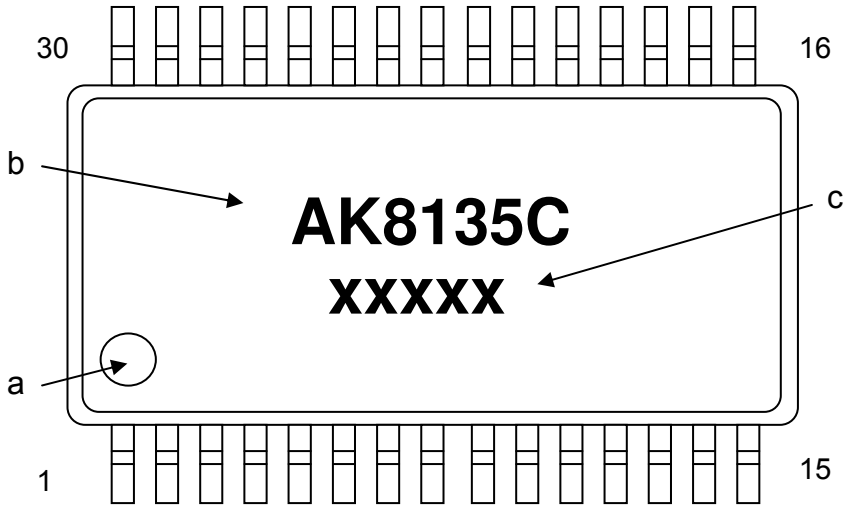
Crystal connection – Proper oscillation performance is susceptible to stray or parasitic capacitors around crystal. The wiring traces to a crystal form XI (Pin 1) and XO (Pin 3) have equal lengths with no via and as short in length as possible. These traces should be also located away from any traces with switching signal.

Package Information

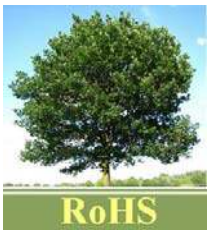


- **Marking**

a: #1 Pin Index
b: Part number
c: Date code (5 digits)



- **RoHS Compliance**



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