

N-channel 600 V, 0.092 Ω typ., 31.5 A MDmesh™ II Power MOSFET in a TO-220FP package

Datasheet - production data

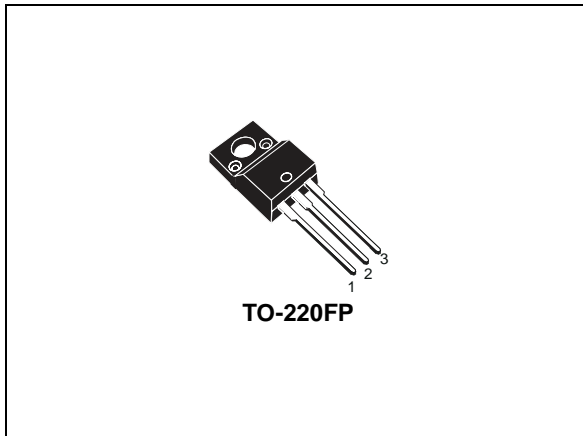
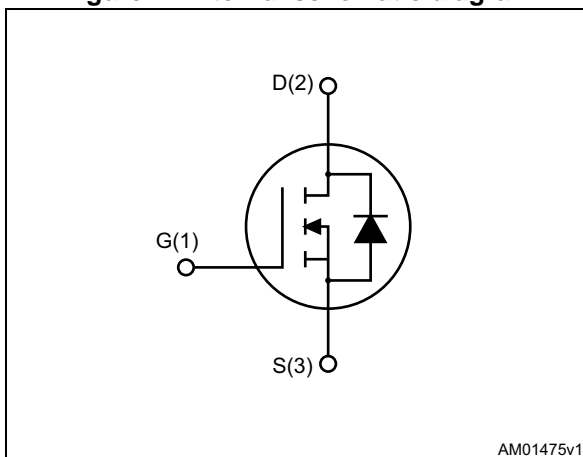


Figure 1. Internal schematic diagram



Features

| Order code | V _{DSS} | R _{DS(on)} | I _D | P _{TOT} |
|------------|------------------|---------------------|----------------|------------------|
| STF34NM60N | 600 V | 0.105 Ω | 31.5 A | 40 W |

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

| Order code | Marking | Packages | Packaging |
|------------|---------|----------|-----------|
| STF34NM60N | 34NM60N | TO-220FP | Tube |

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------------|
| V_{DS} | Drain-source voltage | 600 | V |
| V_{GS} | Gate-source voltage | ± 25 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 31.5 ⁽¹⁾ | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 20 ⁽¹⁾ | A |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 126 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 250 | W |
| I_{AR} | Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax}) | 7 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$) | 345 | mJ |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}$; $T_C=25\text{ }^\circ\text{C}$) | 2500 | V |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| $dv/dt^{(4)}$ | MOSFET dv/dt ruggedness | 50 | V/ns |
| T_{stg} | Storage temperature | -55 to 150 | $^\circ\text{C}$ |
| T_j | Operating junction temperature | 150 | |

- Limited by package
- Pulse width limited by safe operating area.
- $I_{SD} \leq 31.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$
- $V_{DS} \leq 480\text{ V}$

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|--------------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case max | 3.1 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-amb max | 62.5 | |

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--------------------------------------------------|-------------------------------------------------------------------------|------|-------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS} = 0$) | $I_D = 1\text{ mA}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}, T_c = 125\text{ °C}$ | | | 1 100 | μA μA |
| I_{GSS} | Gate body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 25\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}, I_D = 14.5\text{ A}$ | | 0.092 | 0.105 | Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$ | - | 2722 | - | pF |
| C_{oss} | Output capacitance | | - | 173 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 1.75 | - | pF |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent capacitance time related | $V_{GS} = 0, V_{DS} = 0\text{ to }480\text{ V}$ | - | 458 | - | pF |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 300\text{ V}, I_D = 15.75\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 18 and 14) | - | 18 | - | ns |
| t_r | Rise time | | - | 36 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 104 | - | ns |
| t_f | Fall time | | - | 73 | - | ns |
| Q_g | Total gate charge | $V_{DD} = 480\text{ V}, I_D = 31.5\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 15) | - | 84 | - | nC |
| Q_{gs} | Gate-source charge | | - | 14 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 45 | - | nC |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz},$ gate DC Bias=0 test signal level=20 mV open drain | - | 2.9 | - | Ω |

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 31.5 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 126 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD}= 31.5 \text{ A}, V_{GS}=0$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD}= 31.5 \text{ A}, V_{DD}= 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, (see Figure 16) | - | 412 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 8 | | μC |
| I_{RRM} | Reverse recovery current | | - | 39 | | A |
| t_{rr} | Reverse recovery time | $I_{SD}= 12 \text{ A}, V_{DD}= 60 \text{ V}$ $di/dt=100 \text{ A}/\mu\text{s}$, $T_j=150 \text{ }^\circ\text{C}$ (see Figure 16) | - | 490 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 10 | | μC |
| I_{RRM} | Reverse recovery current | | - | 43 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

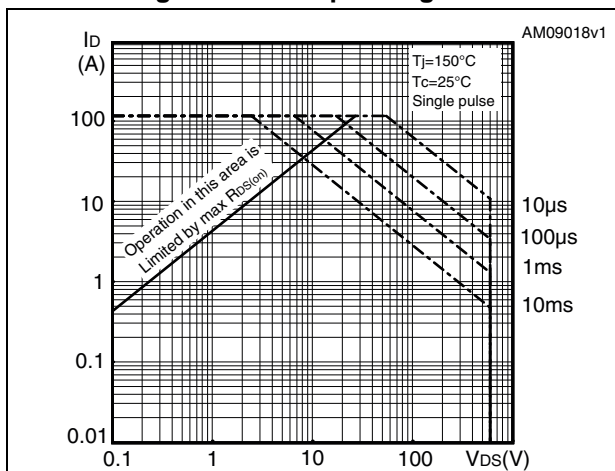


Figure 3. Thermal impedance

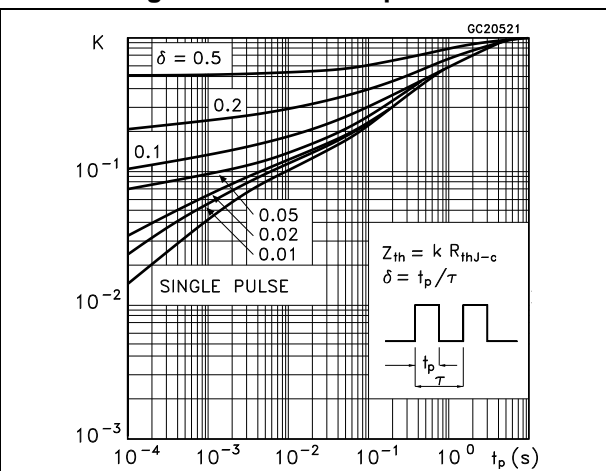


Figure 4. Output characteristics

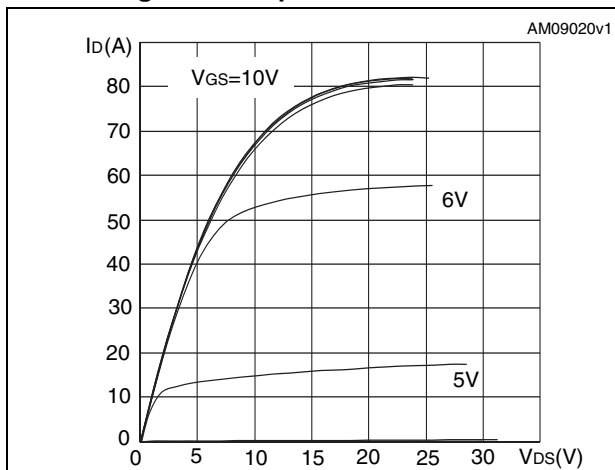


Figure 5. Transfer characteristics

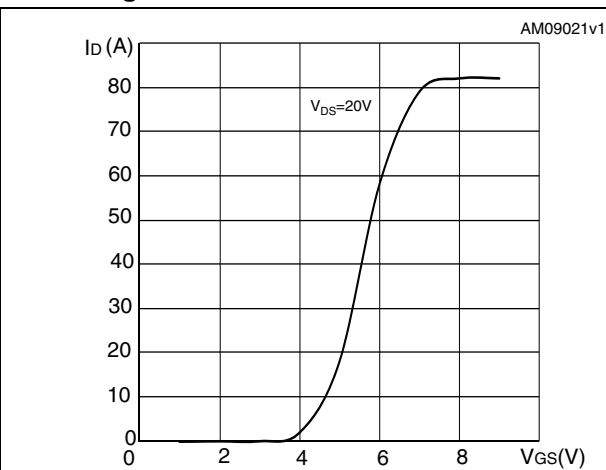


Figure 6. Gate charge vs gate-source voltage

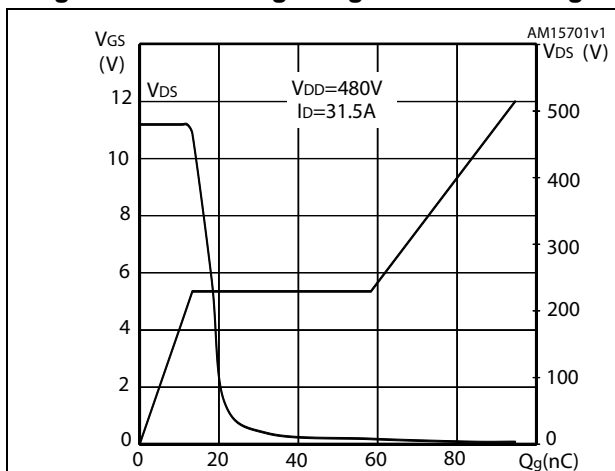


Figure 7. Static drain-source on-resistance

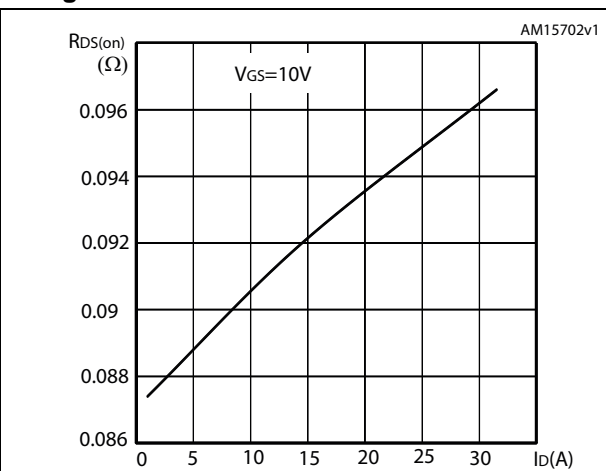


Figure 8. Capacitance variations

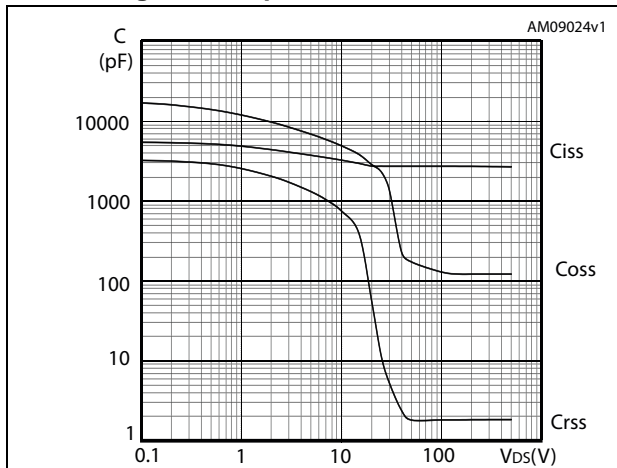


Figure 9. Output capacitance stored energy

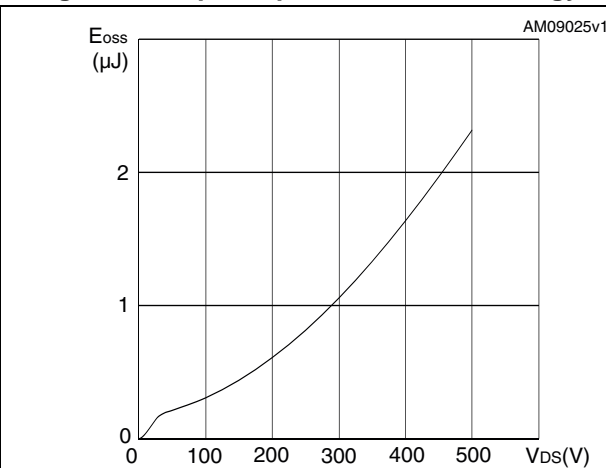


Figure 10. Normalized gate threshold voltage vs temperature

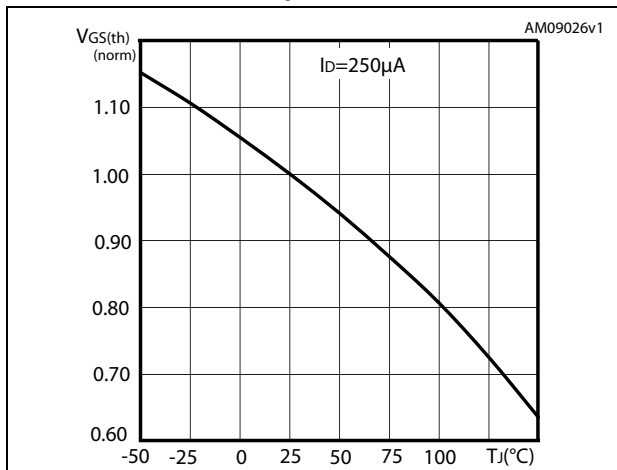


Figure 11. Normalized on-resistance vs temperature

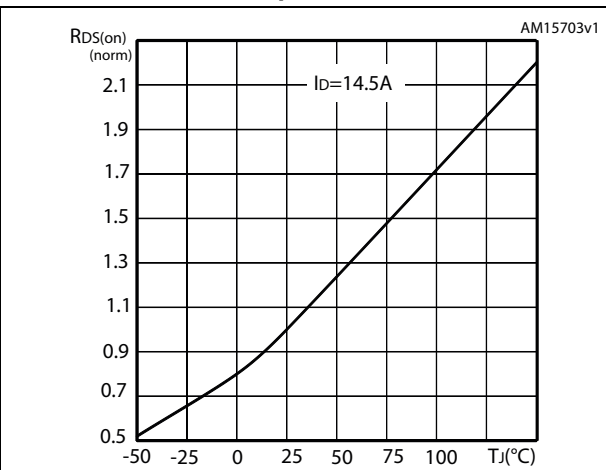


Figure 12. Normalized B_{VDS} vs temperature

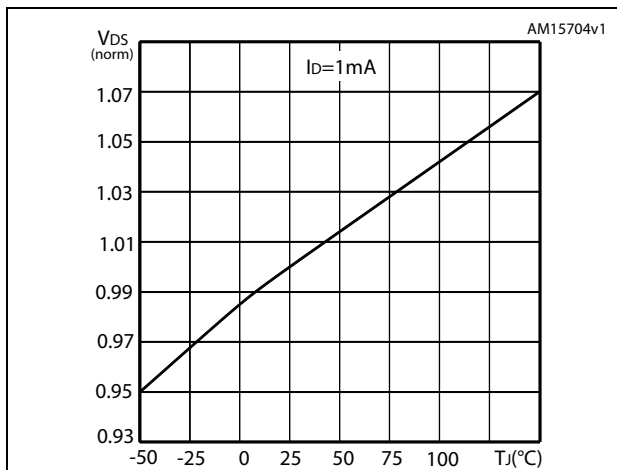
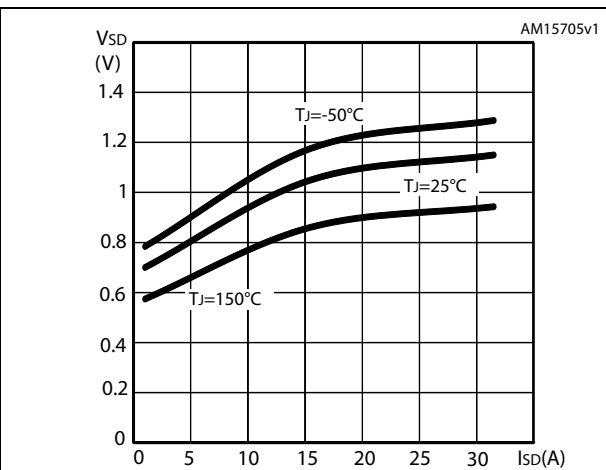
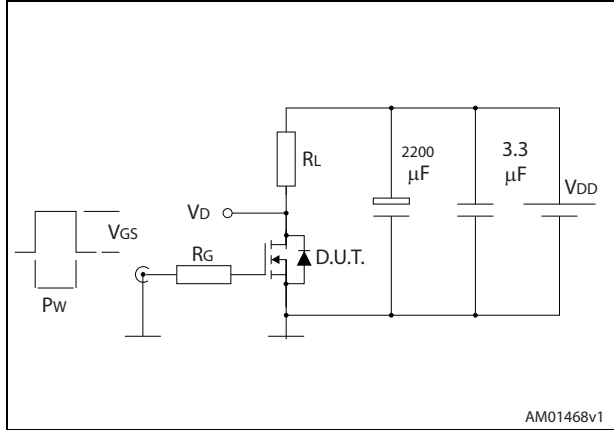


Figure 13. Source-drain diode forward characteristics



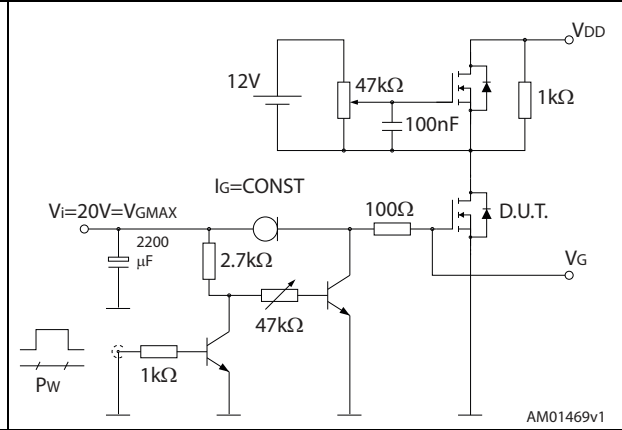
3 Test circuits

Figure 14. Switching times test circuit for resistive load



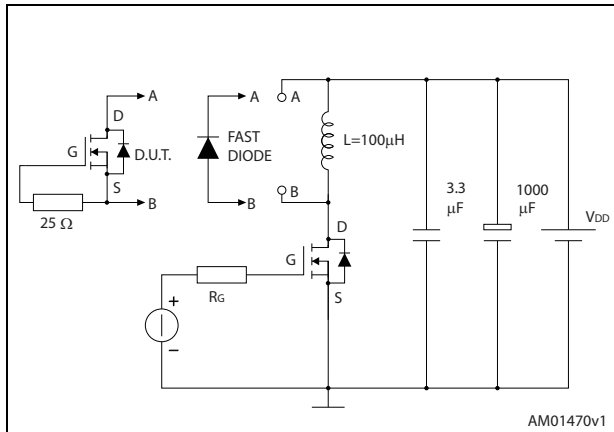
AM01468v1

Figure 15. Gate charge test circuit



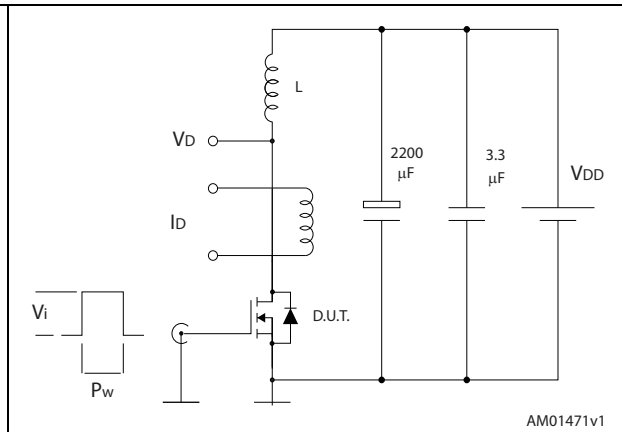
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Figure 16. Test circuit for inductive load switching and diode recovery times



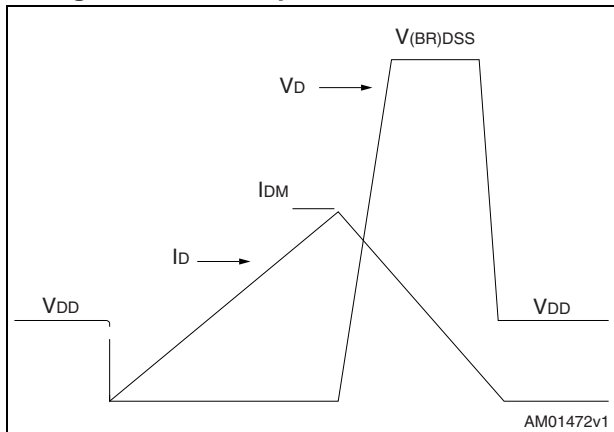
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Figure 17. Unclamped inductive load test circuit



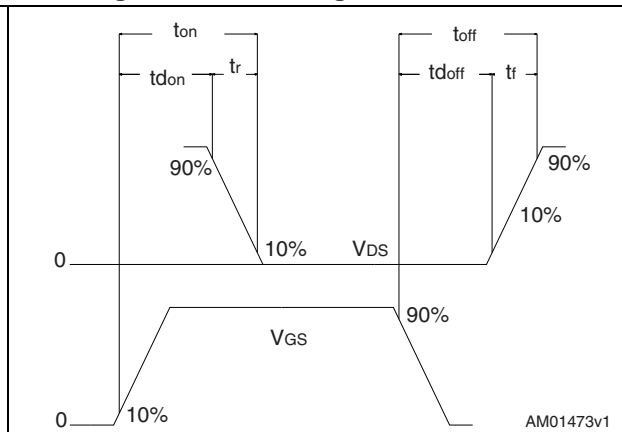
AM01471v1

Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



AM01473v1

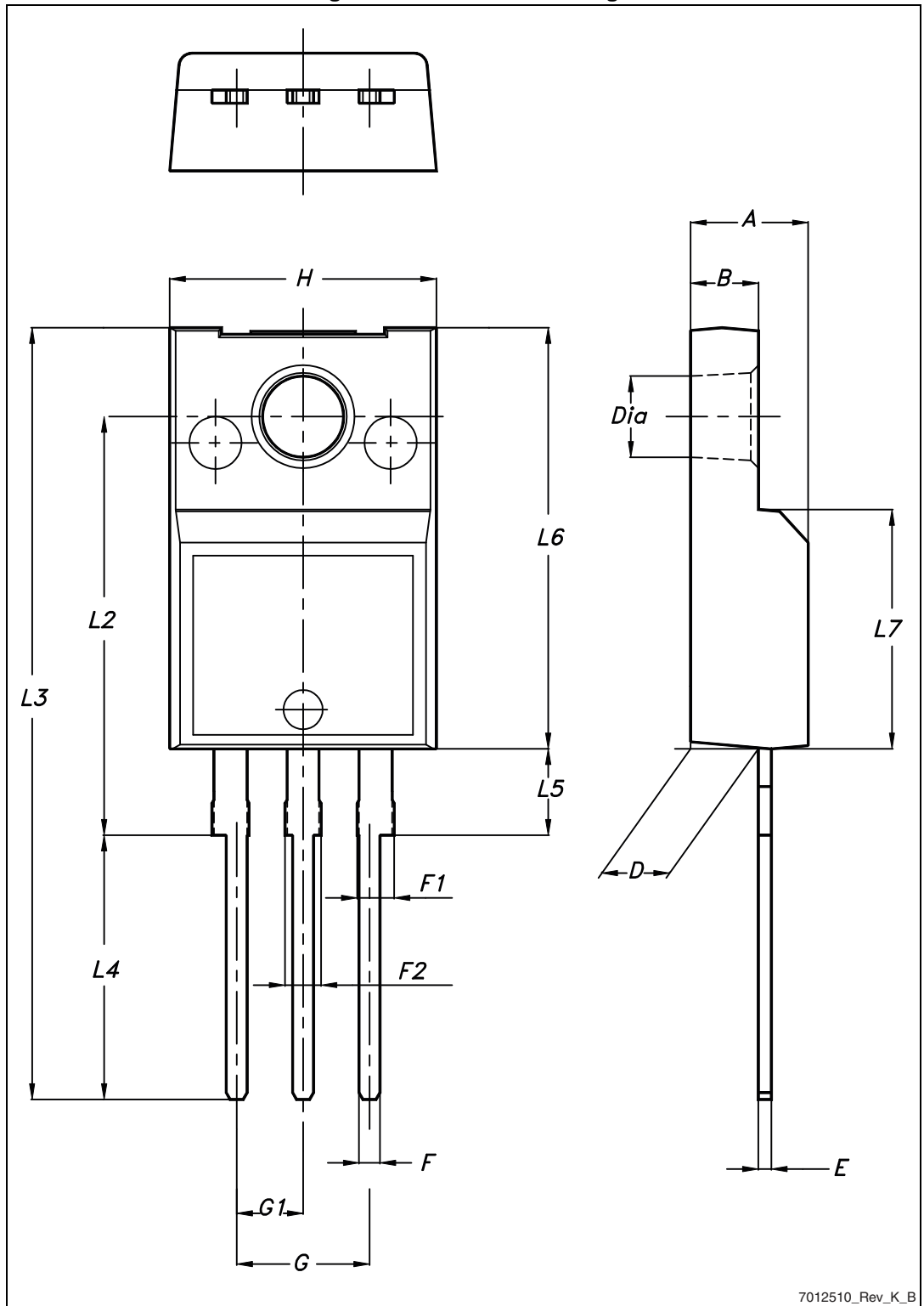
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 7. TO-220FP mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | 4.4 | | 4.6 |
| B | 2.5 | | 2.7 |
| D | 2.5 | | 2.75 |
| E | 0.45 | | 0.7 |
| F | 0.75 | | 1 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.2 |
| G1 | 2.4 | | 2.7 |
| H | 10 | | 10.4 |
| L2 | | 16 | |
| L3 | 28.6 | | 30.6 |
| L4 | 9.8 | | 10.6 |
| L5 | 2.9 | | 3.6 |
| L6 | 15.9 | | 16.4 |
| L7 | 9 | | 9.3 |
| Dia | 3 | | 3.2 |

Figure 20. TO-220FP drawing



7012510_Rev_K_B

5 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|-------------|----------|----------------|
| 16-Jul-2013 | 1 | First release. |

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