IS31AP2031

CLASS-K AUDIO POWER AMPLIFIER WITH INTEGRATED CHARGE PUMP CONVERTER

October 2016

GENERAL DESCRIPTION

The IS31AP2031 is a Class-K audio power amplifier with automatic gain control. It drives up to 2.0W (10%

THD+N) into an 8Ω speaker from a 4.2V V_{DD} supply.

The IS31AP2031 provides low cost, space saving solution for portable equipments which need audio output with higher power by boosting up supply voltage.

Its external components just include a few capacitors and resistors (no inductor).

The IS31AP2031 use fully differential design to reduce RF noise. The IS31AP2031 integrates de-pop circuitry to reduce pop and click noise during power on/off or shutdown enable operation. The IS31AP2031 also integrates thermal and short circuit protection function.

IS31AP2031 is available in QFN-20 (3mm × 3mm) package. It operates from 2.7V to 4.5V over the temperature range of -40°C to +85°C.

FEATURES

- Operates from 2.7V to 4.5V
- 2.0W into an 8Ω load from a 4.2V supply(10% THD+N)
- 4 gain levels: 12dB, 16dB, 24dB, 27.5dB
- AGC function
- Pulse Count Control serial interface
- 8kV HBM ESD
- Thermal and short-circuit protection
- Integrated Click-and-Pop suppression circuitry
- Available in QFN-20(3mm × 3mm) package

APPLICATIONS

- Smart phones
- Cellular phones
- PDAs
- GPS
- Portable electronics

TYPICAL APPLICATION CIRCUIT

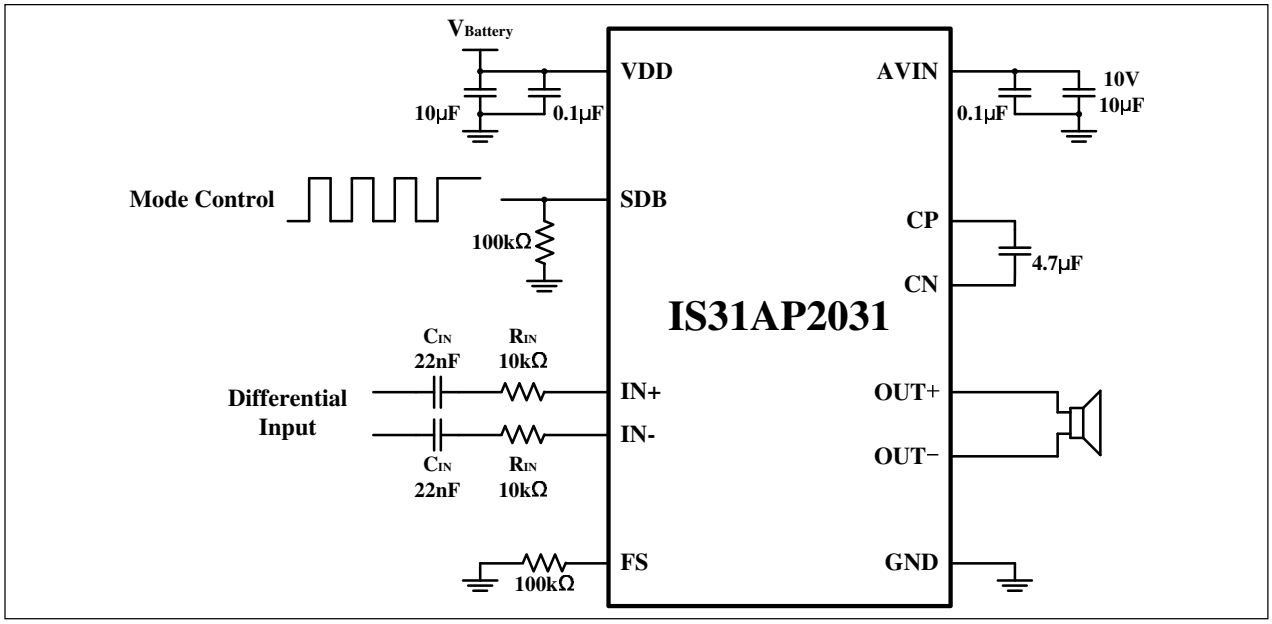


Figure 1 Typical Application Circuit (Differential Input)

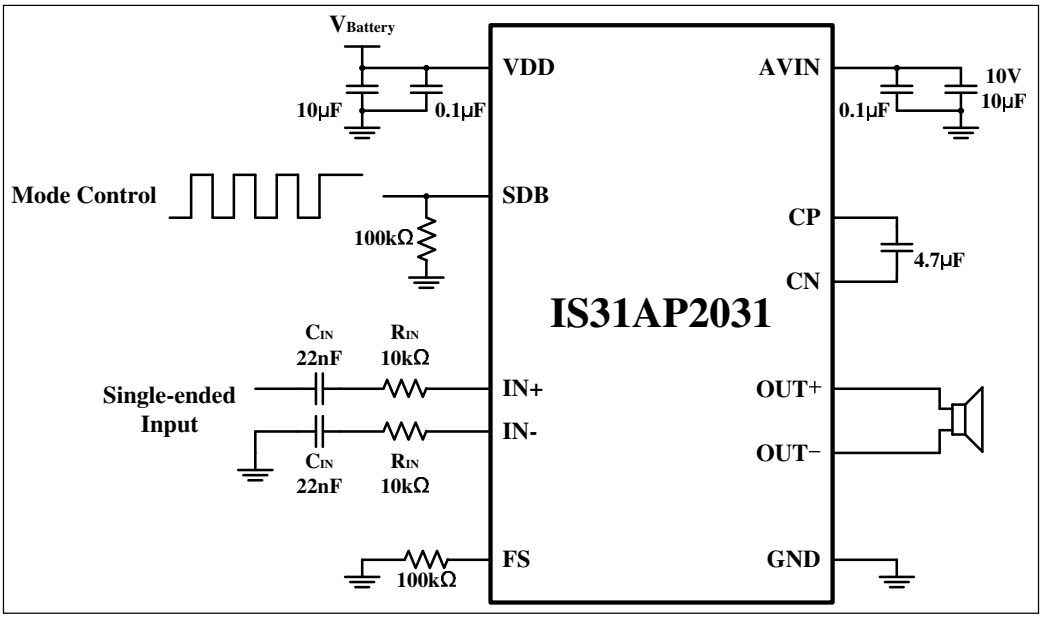
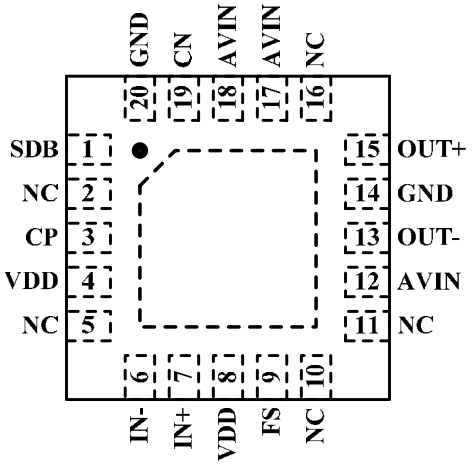


Figure 2 Typical Application Circuit (Single-ended Input)

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-20	

PIN DESCRIPTION

No.	Pin	Description
1	SDB	Shutdown pin. Active low.
2,5,10,11,16	NC	No connection.
3	CP	Positive input for external flying cap.
4,8	VDD	Power supply.
6	IN-	Negative audio input.
7	IN+	Positive audio input.
9	FS	Pull 100kΩ resistor to ground.
12,17,18	AVIN	Amplifier supply voltage.
13	OUT-	Negative audio output.
14,20	GND	GND.
15	OUT+	Positive audio output.
19	CN	Negative input for external flying cap.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
INDUSTRIAL RANGE: -40°C TO +85°C

Order Part No.	Package	QTY/Reel
IS31AP2031-QFLS2-TR	QFN-20, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	−0.3V ~ +6.0V
Voltage at any input pin	−0.3V ~ V_{DD}+0.3V
Thermal resistance, junction to ambient, θ_{JA}	58.9°C/W
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	−65°C ~ +150°C
Operating temperature range, T_A	−40°C ~ +85°C
ESD (HBM) ESD (CDM)	±8kV ±1kV

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.7V ~ 4.5V, unless otherwise noted. Typical value are T_A = +25°C, V_{DD} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.7		4.5	V
I_{DD}	Quiescent current	V_{DD} = V_{AVIN} = 3.6V, no load		5		mA
I_{SD}	Shutdown current	V_{SDB} = 0V			1	μA
F_{OSC}	Clock frequency			350		kHz
V_{AVIN}	Charge pump output	No load		5.7		V
t_{ON}	Charge pump soft start time			600		μs
$\|V_{OS}\|$	Output offset voltage			3		mV
R_{IN}	Input resistor	Mode 1, Mode 2		30		kΩ
		Mode 3, Mode 4		5		
F_{SW}	Switching frequency			250		kHz
V_{IH}	Input logic high voltage		1.4			V
V_{IL}	Input logic low voltage				0.4	V
I_{IH}	Input logic high current			2.1		μA
I_{IL}	Input logic low current			0.8		μA
T_{OTP}	Over temperature protection	*(Note 1)*		150		°C
T_{HYS}	Hysteresis temperature	*(Note 1)*		50		°C

AC CHARACTERISTICS *(Note 1)*

T_A = 25°C, V_{DD} = 3.6V, unless otherwise noted.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Po	Output power	THD+N = 10%, f = 1kHz R_L = 8Ω+33μH	V_{DD} = 3.6V		1.72		W
			V_{DD} = 4.2V		2.0		
		THD+N = 1%, f = 1kHz R_L = 8Ω+33μH	V_{DD} = 3.6V		1.38		
			V_{DD} = 4.2V		1.70		
THD+N	Total harmonic distortion plus noise	V_{DD} = 3.6V, P_O = 0.5W, R_L = 8Ω+33μH f = 1kHz			0.33		%
		V_{DD} = 4.2V, P_O = 1.0W, R_L = 8Ω+33μH f = 1kHz			0.53		
t_{WU}	Wake-up time from shutdown				35		ms
PSRR	Power supply rejection ratio	V_{P-P} = 200mV， R_L = 8Ω， f = 217Hz			-74		dB
		V_{P-P} = 200mV， R_L = 8Ω， f = 1kHz			-68		
t_{AT}	Attack time				10		ms
t_{RL}	Release time				1.2		s
A_{max}	Max attenuation gain				-8		dB
t_{LO}	Mode control low time			0.75		10	μs
t_{HI}	Mode control high time			0.75		10	μs
t_{OFF}	CTRL off time for shutdown			150			μs

Note 1: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

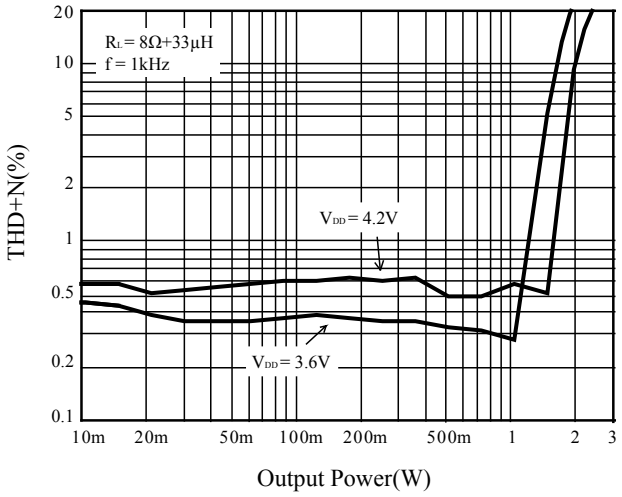


Figure 3 THD+N vs. Output Power

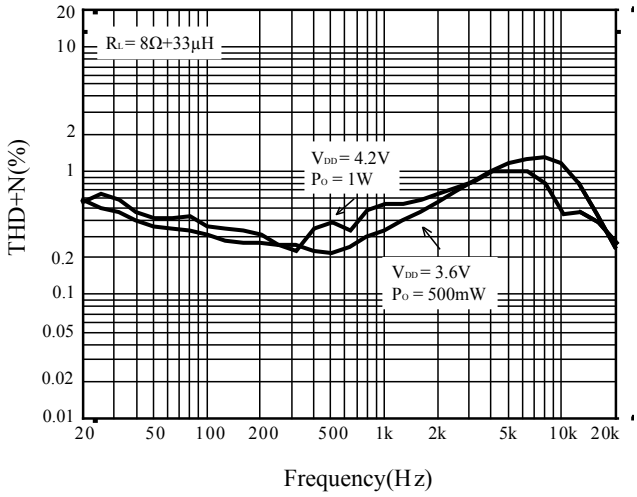


Figure 4 THD+N vs. Frequency

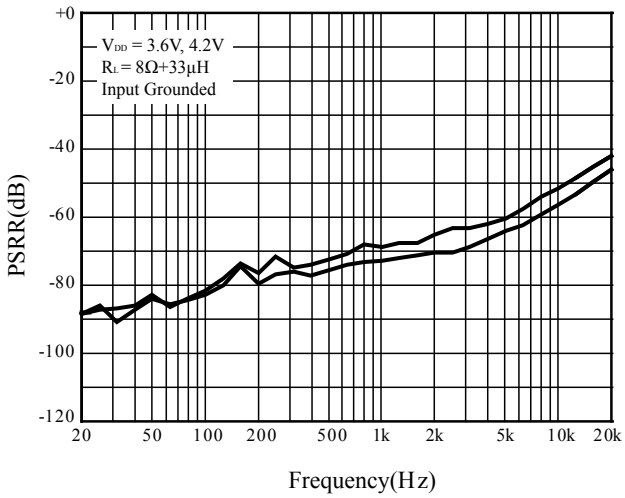


Figure 5 PSRR vs. Frequency

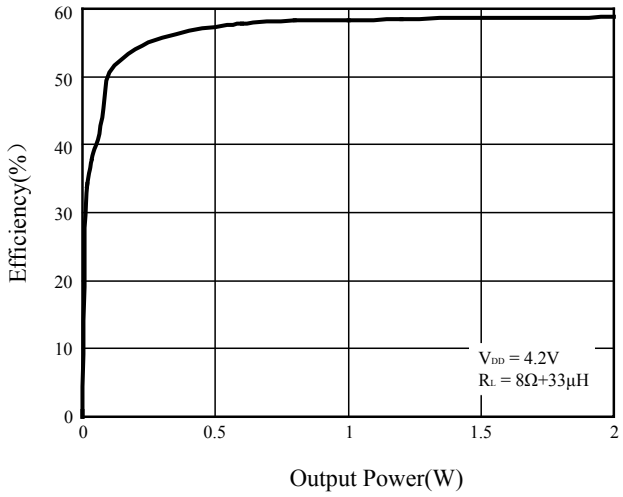


Figure 6 Efficiency vs. Output Power

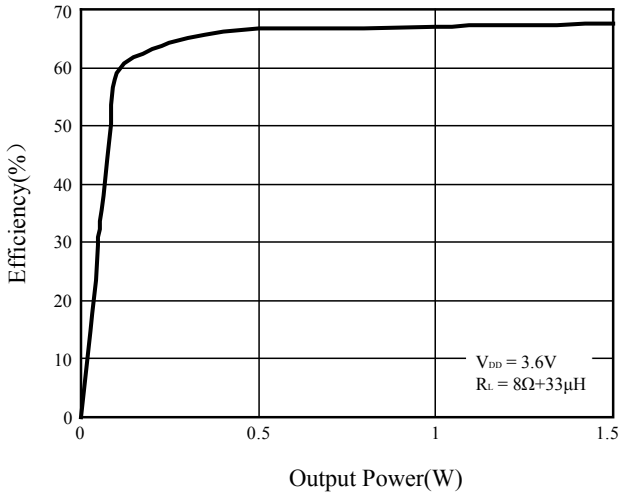


Figure 7 Efficiency vs. Output Power

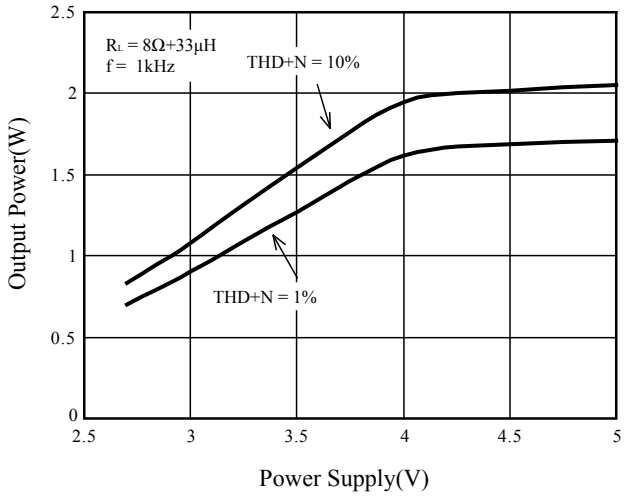


Figure 8 Output Power vs. Power Supply

APPLICATION INFORMATION

GENERAL DESCRIPTION

The IS31AP2031 is a Class-K audio power amplifier with an integrated charge pump converter. It consists of a charge pump and a fully differential audio amplifier. The operating mode and gain are controlled by Pulse Count Control (PCC wire) serial interface.

AGC FUNCTION

This is the function to control the output in order to obtain a maximum output level without distortion when an excessive input is applied which would otherwise cause clipping at the differential signal output. That is, with the AGC function, IS31AP2031 lowers the gain of the digital amplifier to an appropriate value so as not to cause clipping at the differential signal output.

The attack time is a time interval that gains falls down with a big signal input enough. And the release time is a time from target attenuation to no AGC attenuation.

Assuming no limitation by the power supply, the audio output signal would be as in Figure 9.

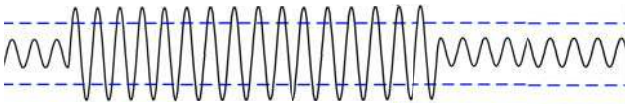


Figure 9 Assuming no Restriction from Power Supply, the Audio Output Signal

In normal operation without the AGC, the output is distorted because of the restriction from power supply, as shown in Figure 10.

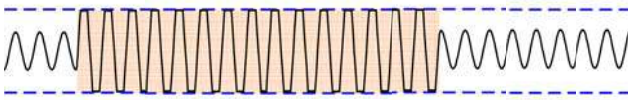


Figure 10 AGC Function Off

With the AGC function of IS31AP2031, the optimum output power can be obtained along with the minimal distortion. The Figure 11 shows the outcome of AGC function.

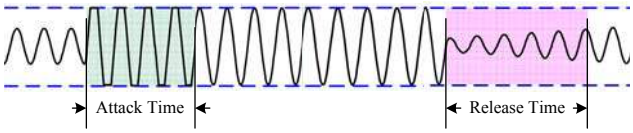


Figure 11 AGC Function On

OPERATING MODE

The operating mode and gain are controlled by Pulse Count Control (PCC wire) serial interface. The interface records rising edges of the SDB pin and decodes them into 4 operating mode (Figure 12).

If the SDB pin is pulled to high, receiving one rising edge, the IC starts up and operates in Mode 1. If the SDB pin receives two rising edges, the IC operates in Mode 2. If the SDB pin receives three rising edges, the IC operates in Mode 3. If the SDB pin receives four rising edges, the IC operates in Mode 4.

Mode 1—12dB, AGC off.

Mode 2—16dB, AGC on.

Mode 3—24dB, AGC off.

Mode 4—27.5, AGC on.

If the SDB pin is pulled to low last at least 150μs, the IC will be into shutdown mode.

The gain also can be controlled by the input resistors R_{IN}.

Mode 1: A_V = 160kΩ / (30kΩ+R_{IN})

Mode 2: A_V = 240kΩ/ (30kΩ+R_{IN})

Mode 3: A_V = 240kΩ/ (5kΩ+R_{IN})

Mode 4: A_V = 360kΩ/ (5kΩ+R_{IN})

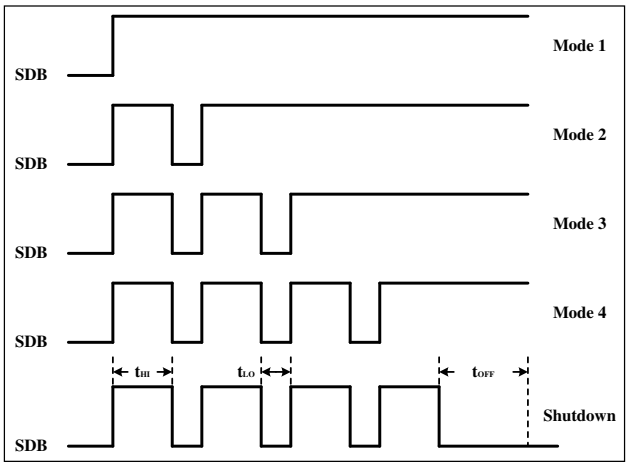


Figure 12 Operating Mode Control

CHARGE PUMP

The charge pump converter boosts input supply voltage (V_{DD}) up to a 5.7V output voltage (V_{OUT}). V_{OUT} is the supply for the Class-K amplifier.

The charge pump converter only needs three external components: supply decoupling capacitor, output bypass capacitor and flying capacitor.

Choose low ESR capacitors to ensure the best operating performance and place the capacitors as close as possible to the IS31AP2031.

FULLY DIFFERENTIAL AUDIO AMPLIFIER

The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around V_{DD}/2 regardless of the common-mode voltage at the input.

The fully differential IS31AP2031 can still be used with a single-ended input; however, the IS31AP2031 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

ADVANTAGES OF FULLY DIFFERENTIAL AMPLIFIERS

The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid-supply affects both positive and negative channels equally and cancels at the differential output.

GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the noise signal much better than the typical audio amplifier.

INPUT CAPACITORS (C_{IN})

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_C, determined in Equation (1) when IS31AP2031 operates in Mode 1 and Mode 2.

$$f_c = \frac{1}{2\pi(R_{IN} + 30\text{k}\Omega)C_{IN}} \quad (1)$$

Follow the Equation (2) when IS31AP2031 operates in Mode 3 and Mode 4.

$$f_c = \frac{1}{2\pi(R_{IN} + 5\text{k}\Omega)C_{IN}} \quad (2)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

DESIGN NOTE

COMPONENT SELECTION

The value and ESR of the output capacitor for charge pump will affect output ripple and transient performance. A X7R or X5R ceramic capacitor in 10μF should be recommended. The flying capacitor should use a 4.7μF X7R or X5R ceramic capacitor.

All the capacitors should support at least 10V.

PCB LAYOUT

The decoupling capacitors should be placed close to the VDD pin and the output capacitors should be placed close to the AVIN pin. The flying capacitor should be placed close to the CN and CP pins. The input capacitors and input resistors should be placed close to the IN+ and IN- pins and the traces must be parallel to prevent noise. The traces of OUT+ and OUT- pins connected to the speaker should be as possible as short and wide. The recommended width is 0.5mm.

Trace width should be at least 0.75mm when the current reaches 1A. Trace width should be at least 1.0mm for the power supply and the ground plane. The thermal pad and the GND pin should connect directly to a strong common ground plane for heat sinking.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

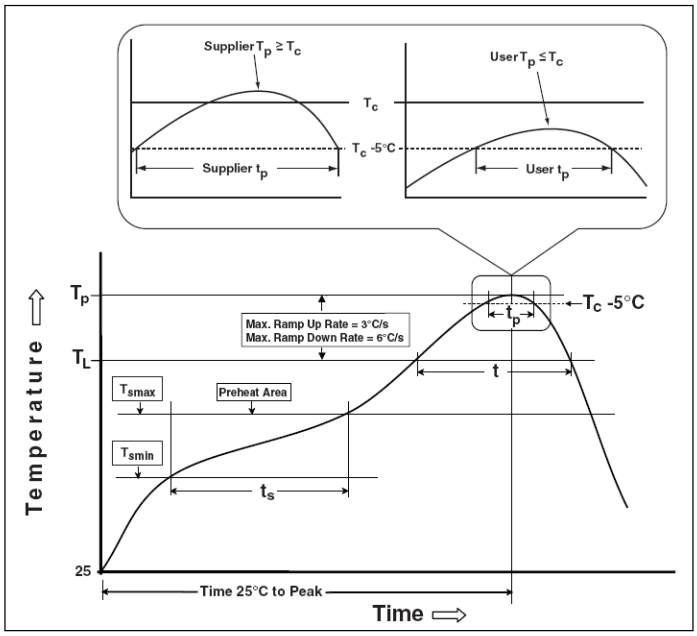
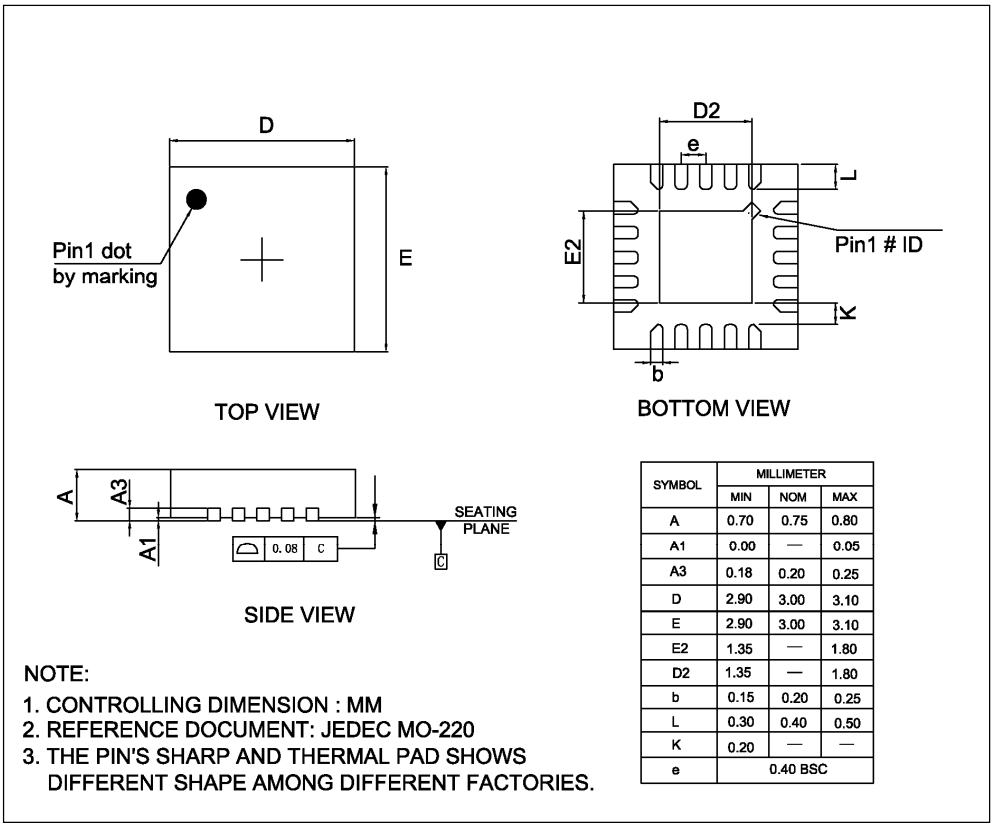


Figure 13 Classification Profile

PACKAGE INFORMATION

QFN-20

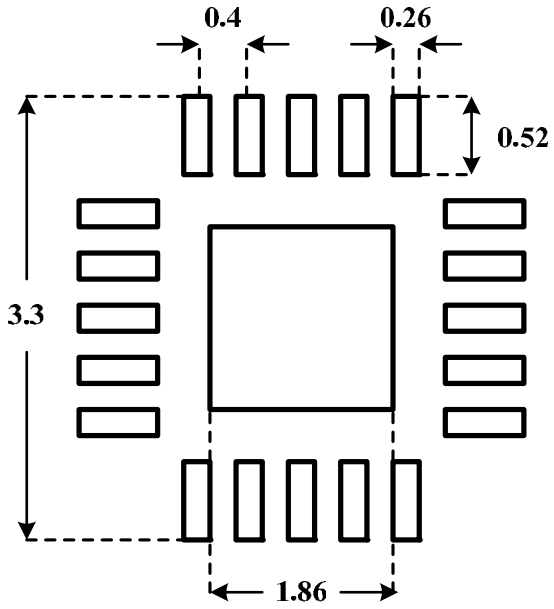


NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.18	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E2	1.35	—	1.80
D2	1.35	—	1.80
b	0.15	0.20	0.25
L	0.30	0.40	0.50
K	0.20	—	—
e	0.40 BSC		

Note: All dimensions in millimeters unless otherwise stated.

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2011.12.28
B	1.Change Class-G to Class-K 2.add θ_{JA} in ABSOLUTE MAXIMUM RATINGS 3.add RECOMMENDED LAND PATTERN in page 12	2016.10.25