FocalTech

FT5x46

True Multi-Touch Capacitive Touch Panel Controller

INTRODUCTION

The FT5X46 is single-chip capacitive touch panel controllers with built-in enhanced Micro-controller unit (MCU).It provides the benefits of full screen common mode scan technology,fast response time and high level of accuracy.It can drive capacitive type touch panel with up to 20 driving and 28 sensing lines.

FEATURES

- Mutual Capacitive Sensing Techniques
- Full Screen Common Mode Scan Techniques
- 5346DQQ Supports up to 15TX + 24 RX
- 5446DQS Supports up to 16TX + 28 RX
- 5446WWa Supports up to 20TX + 28 RX
- Support up to 10 fingers
- High immunity to inductive power noise
- Automatic mode switching (Active, Monitor,Sleep)
- Support >100Hz sampling rate
- Auto-calibration
- Support IIC (up to 400kbits/sec) interface
- Power
  - 2.7 to 3.6V Operating Voltage
  - IOVCC supports from 1.8V to 3.6V
- Built-in 64KB Flash
- Single Channel(TX or RX)resistance: Up to 100K Ω
- Single Channel (transmit/receive) Capacitance: 40pF
- 12-Bit ADC Accuracy
- Features “short I/O ” testing for sense pins
- Supports various type of panels with no ground shielding layer
- 3 Operating Modes
  - Active
  - Monitor
  - Sleep
- Operating Temperature Range: -40°C to +85°C
- Package:
  - QFN56L 6x6x0.6mm, 0.35mm/pitch
  - BGA62L 5x5x0.6mm, 0.6mm/pitch

TABLE OF CONTENTS

1 OVERVIEW

1.1 Typical Applications

FT5X46 provids a wide range of applications with a set of buttons up to a 2D touch sensing device.It ‘s powerful design for below applications.

- Mobile phones
- Navigation systems, GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras

FT5X46 support Touch Panel, the spec is listed in the following table,

Part Number	Package	TX	RX	Total Channels	Recommended for Smart Phone TP Size (16:9)
FT5346DQQ	QFN 56L 6x6x0.6mm Pitch =0.35mm	15	24	39	≦5.5”, Sensor Pitch:5mm
FT5446DQS	QFN 56L 6x6x0.6mm Pitch =0.35mm	16	28	44	≦6.1”, Sensor Pitch:5mm
FT5446WWa	BGA 62L 5x5x0.6mm Pitch =0.6mm	20	28	48	≦6.4”, Sensor Pitch:5mm

2 FUNCTIONAL BLOCK DESCRIPTIONS

2.1 Architecture Overview

Figure2-1 shows the architecture of FT5X46.

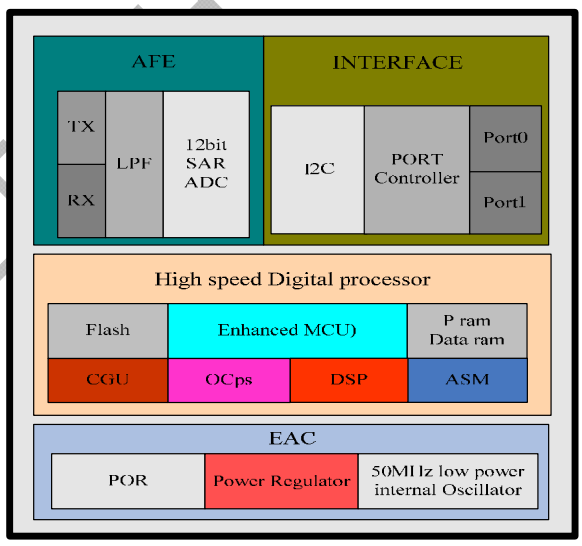


Figure 2-1 System Architecture Diagram

The FT5X46 has five main functional parts below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. It includes both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces.

- Enhanced MCU with DSP accelerator

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash memory is implemented to store programs and some key parameters.
Complex signal processing algorithms are implemented by MCU and DSP accelerator to detect the touches reliably and efficiently. Communication protocol software is also implemented in this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip. The port is also use to wake up the FT5X46 from the Sleep mode.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply
- Power On Reset (POR) is active until VDDD is higher than some level and hold decades of μs.

2.2 MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- A DSP accelerator cooperates with MCU to process the complex algorithms
- Timer: A number of timers are available to generate different clocks
- Clock Manager: To control various clocks under different operation conditions of the system

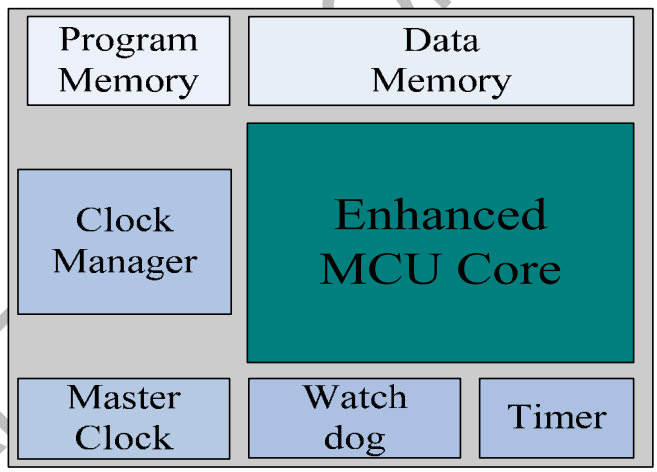


Figure 2-2 MCU Block Diagram

2.3 Operation Modes

FT5X46 offers following three modes:

- **Active Mode**

In active mode,the frame scan rate is 0~120Hz.The host processor can configure it to speed up or to slow down.

- **Monitor Mode**

In monitor mode, the frame scan rate is 25Hz and the host processor can increase or decrease this rate. In this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5X46 shall enter the Active mode immediately. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- **Sleep Mode**

In Sleep mode, it shall only respond to the “RESET” signal from the host processor.

2.4 Host Interface

Figure 2-3 shows the interface between a host processor and FT5X46. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT5X46 to the Host
- Reset Signal from the Host to FT5X46

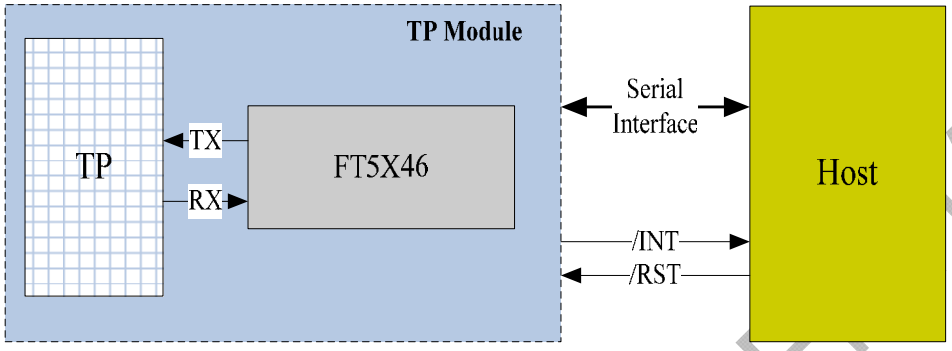


Figure 2-3 Host Interface Diagram

The serial interface of FT5X46 is I2C. The detail of the interface is described in detail in Section 2.5. The interrupt signal (/INT) is used for FT5X46 to inform the host that data are ready for the host to receive. The /RST signal is used for the host to wake up FT5X46 from the Sleep mode. After resetting, FT5X46 shall enter the Active mode.

2.5 Serial Interface

FT5X46 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4**.

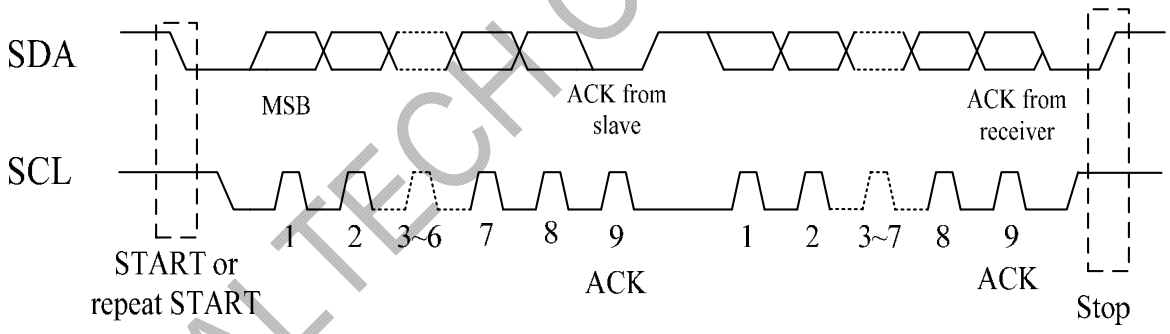


Figure 2-4 I2C Serial Data Transfer Format

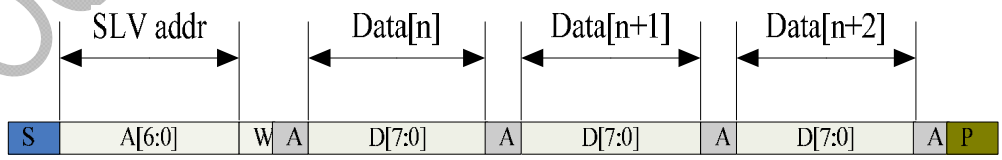


Figure 2-5 I2C master write, slave read

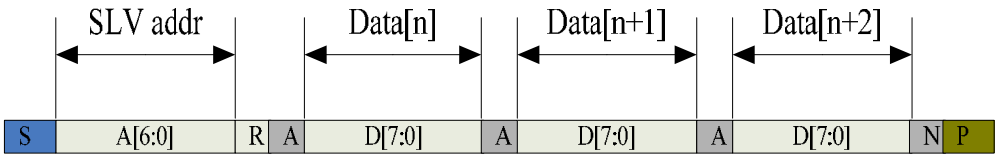


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDD3 – VSS	2.7 ~ 3.6	V	1, 3
I/O Digital Voltage	IOVCC	1.8~3.6	V	1
Operating Temperature	Topr	-40 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1

Notes

1. If used beyond the absolute maximum ratings, FT5X46 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDD3 (high) ≥VSSLF (low)

3.2 DC Characteristics

Table 3-2 DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V	IOH=-0.1mA	0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V	IOH=0.1mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	uA	Vin=0~VDD3	-1	--	1	
Current consumption （Normal operation mode）	Iopr	mA	VDD3 = 3V Ta=25℃ MCLK=24MHz	--	11	--	
Current consumption （Monitor mode）	Imon	mA	VDD3 = 3V Ta=25℃ MCLK=24MHz	--	0.43	--	
Current consumption （Sleep mode）	Islp	uA	VDD3 = 3V Ta=25℃ MCLK=24MHz	--	42	--	
Step-up output voltage	VDD5	V	VDD3= 2.8V		0.25		
Step-up output voltage	VDD10	V	VDD3= 2.8V		0.5		
Power Supply voltage	VDD3	V		2.7	--	3.6	

Notes: This sample data is intended for design guidance only. Values shown are typical for a 15Tx × 24Rx sensor configured at 80 Hz report rate.Actual current will depend on the particular sensor design and firmware options.

3.3 AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V; Ta=25℃	49	50	51	

Table 3-3 AC Characteristics of TX & RX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		50	150	400	KHz	
TX output rise time	Ttxr		--	210	--	nS	
TX output fall time	Ttxf		--	210	--	nS	
RX input voltage	Trxi		1.2	--	1.6	V	

3.4 I/O Ports Circuits

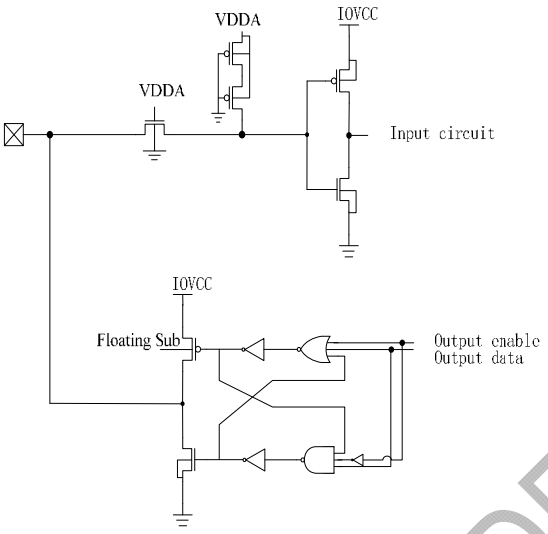


Figure 3-1 General Purpose *In/Out Port Circuit.*

The input/output property can be configured via firmware setting. The firmware can also control its output behavior as push-pull or as open-drain that SDA of I2C interface is required.

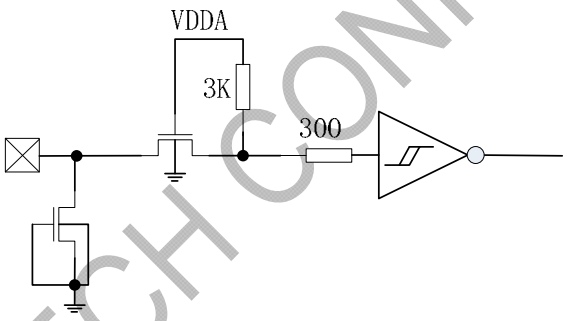


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

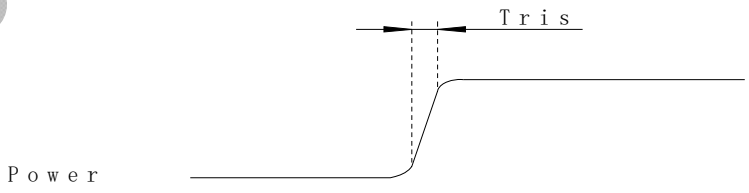


Figure 3-3 Power on time

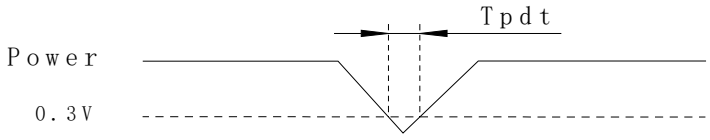


Figure 3-4 Power Cycle requirement

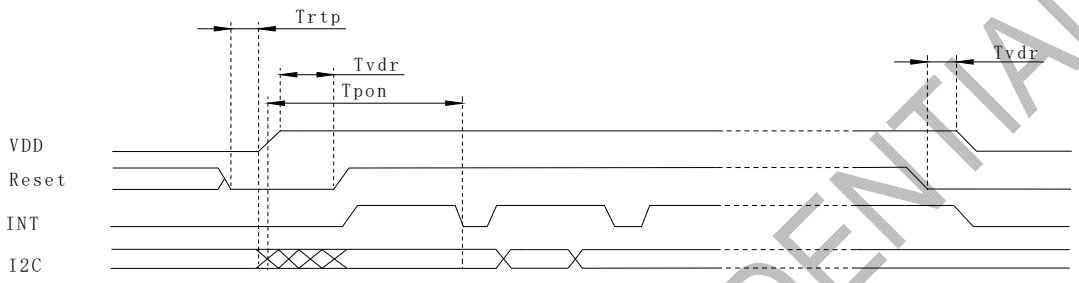


Figure 3-5 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

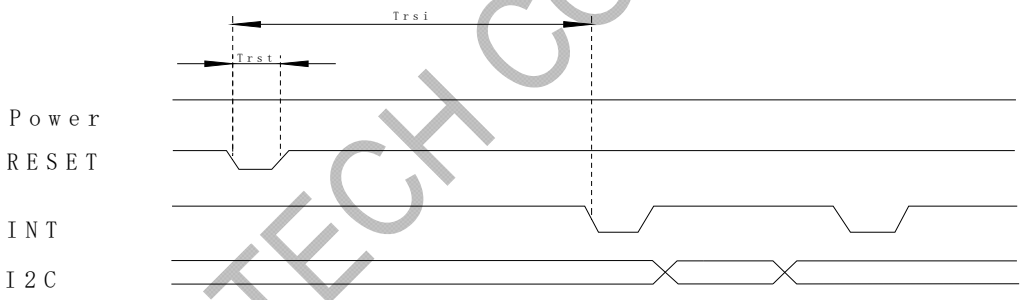


Figure 3-6 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tpon	Time of starting to report point after powering on	--	200	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	1	--	ms

4 PIN CONFIGURATIONS

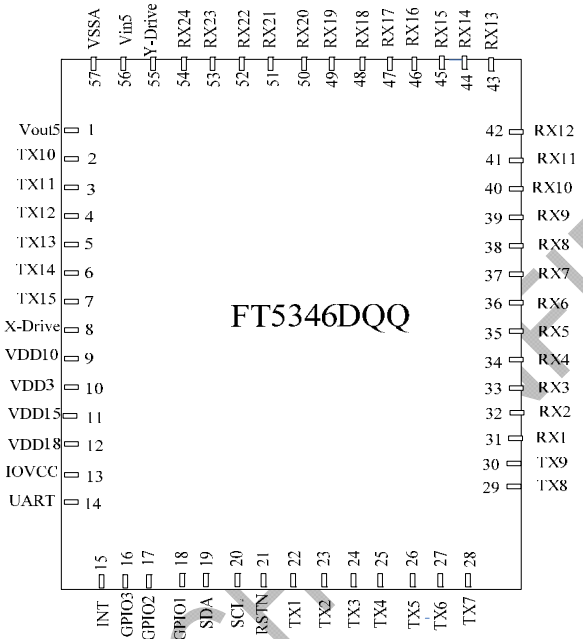
Pin List of FT5X46

Table 4-1 Pin Definition

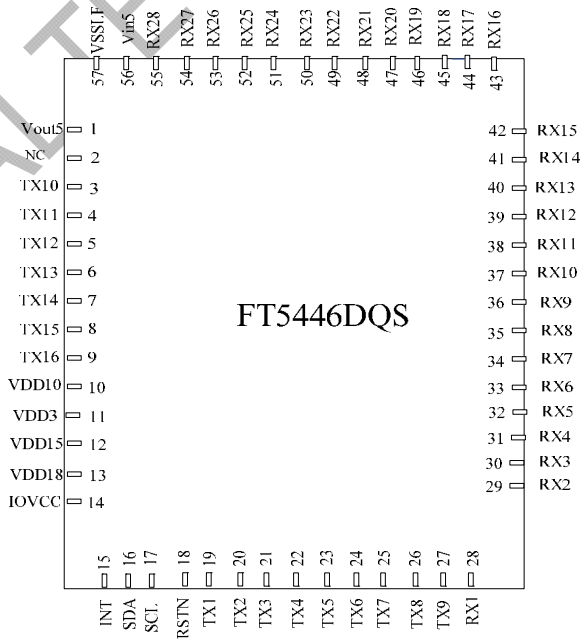
Name	Pin/Ball No.			Type	Description
	5346DQQ	5446DQS	5446WWa		
RX28		55	H1	I	Receiver input pins
RX27		54	H2	I	Receiver input pins
RX26		53	H3	I	Receiver input pins
RX25		52	H4	I	Receiver input pins
RX24	54	51	G1	I	Receiver input pins
RX23	53	50	G2	I	Receiver input pins
RX22	52	49	G3	I	Receiver input pins
RX21	51	48	G4	I	Receiver input pins
RX20	50	47	G5	I	Receiver input pins
RX19	49	46	F1	I	Receiver input pins
RX18	48	45	F2	I	Receiver input pins
RX17	47	44	F3	I	Receiver input pins
RX16	46	43	F4	I	Receiver input pins
RX15	45	42	F5	I	Receiver input pins
RX14	44	41	A1	I	Receiver input pins
RX13	43	40	B1	I	Receiver input pins
RX12	42	39	C1	I	Receiver input pins
RX11	41	38	D1	I	Receiver input pins
RX10	40	37	E1	I	Receiver input pins
RX9	39	36	A2	I	Receiver input pins
RX8	38	35	B2	I	Receiver input pins
RX7	37	34	C2	I	Receiver input pins
RX6	36	33	D2	I	Receiver input pins
RX5	35	32	E2	I	Receiver input pins
RX4	34	31	E3	I	Receiver input pins
RX3	33	30	D3	I	Receiver input pins
RX2	32	29	E4	I	Receiver input pins
RX1	31	28	D4	I	Receiver input pins
VDD5_IN	56	56	H7	PWR	internal generated 5V power supply, A 1μF ceramic capacitor to ground

					is required.
VSSLF	57	57	D6	PWR	Analog ground
VDD5_Out	1	1	H6	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
NC		2		NC	
X-Drive	8			NC	
Y-Drive	55			NC	
TX10	2	3	B7	O	Transmit output pin
TX11	3	4	B6	O	Transmit output pin
TX12	4	5	B5	O	Transmit output pin
TX13	5	6	B4	O	Transmit output pin
TX14	6	7	B3	O	Transmit output pin
TX15	7	8	A8	O	Transmit output pin
TX16		9	A7	O	Transmit output pin
TX17			A6	O	Transmit output pin
TX18			A5	O	Transmit output pin
TX19			A4	O	Transmit output pin
TX20			A3	O	Transmit output pin
VDD10	9	10	G7	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
VDD3	10	11	H5	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
VDD15	11	12	G6	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
VDD18	12	13	H8	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
IOVCC	13	14	G8	PWR	I/O power supply
INT	15	15	E8	I/O	Interrupt request to the host, or Wakeup request from the host.
UART	14		E6	I/O	UART port
GPIO1	18		F7	I/O	General Purpose Input/Output port Support PS2_CLK
GPIO2	17			I/O	General Purpose Input/Output port Support PS2_Data
GPIO3	16			I/O	General Purpose Input/Output port
SDA	19	16	F6	I/O	I2C data input and output
SCL	20	17	E7	I/O	I2C clock input
RSTN	21	18	F8	I	External Reset, Low is active
TX1	22	19	D8	O	Transmit output pin
TX2	23	20	D7	O	Transmit output pin

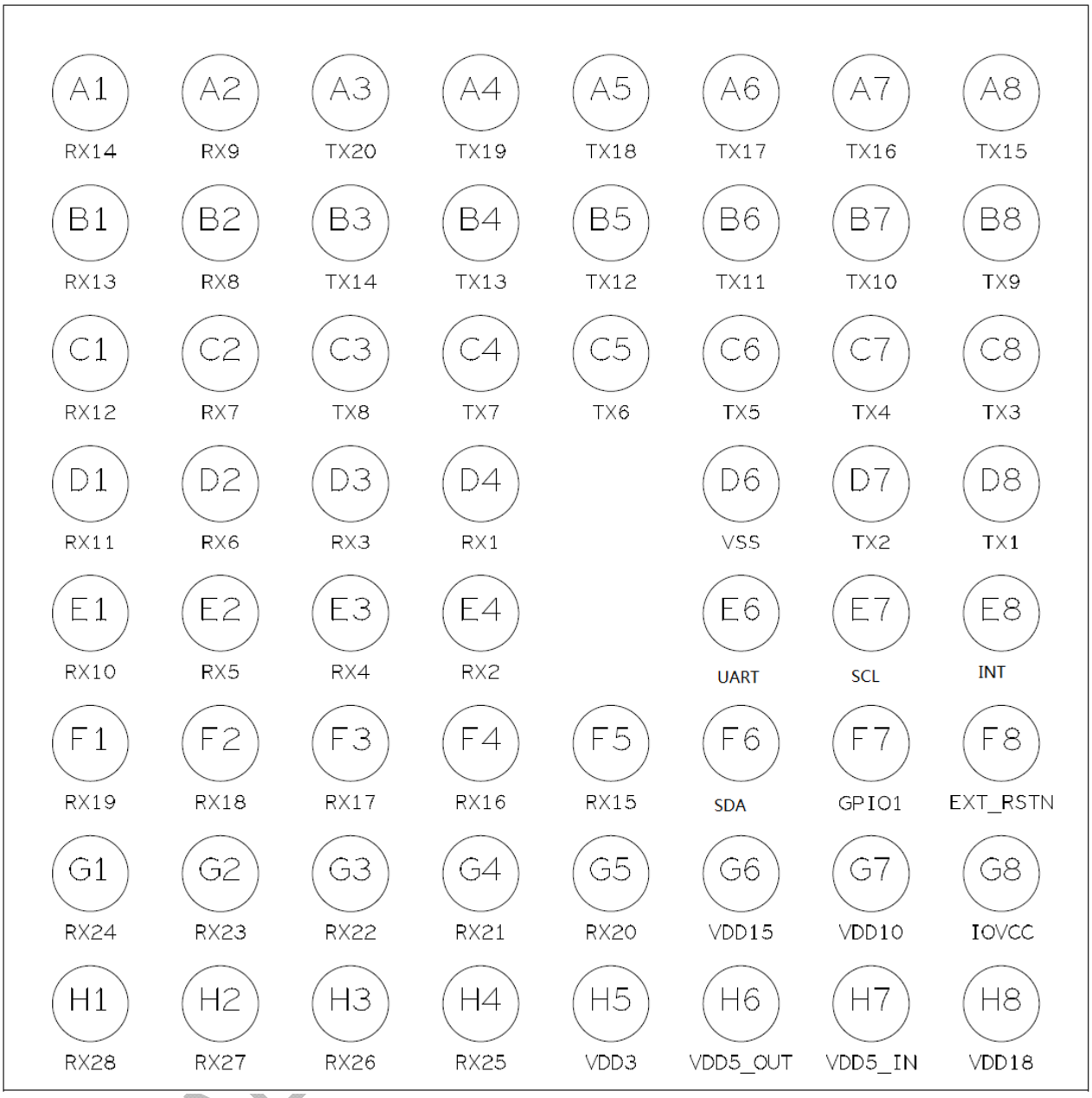
TX3	24	21	C8	O	Transmit output pin
TX4	25	22	C7	O	Transmit output pin
TX5	26	23	C6	O	Transmit output pin
TX6	27	24	C5	O	Transmit output pin
TX7	28	25	C4	O	Transmit output pin
TX8	29	26	C3	O	Transmit output pin
TX9	30	27	B8	O	Transmit output pin



FT5346DQQ Package Diagram



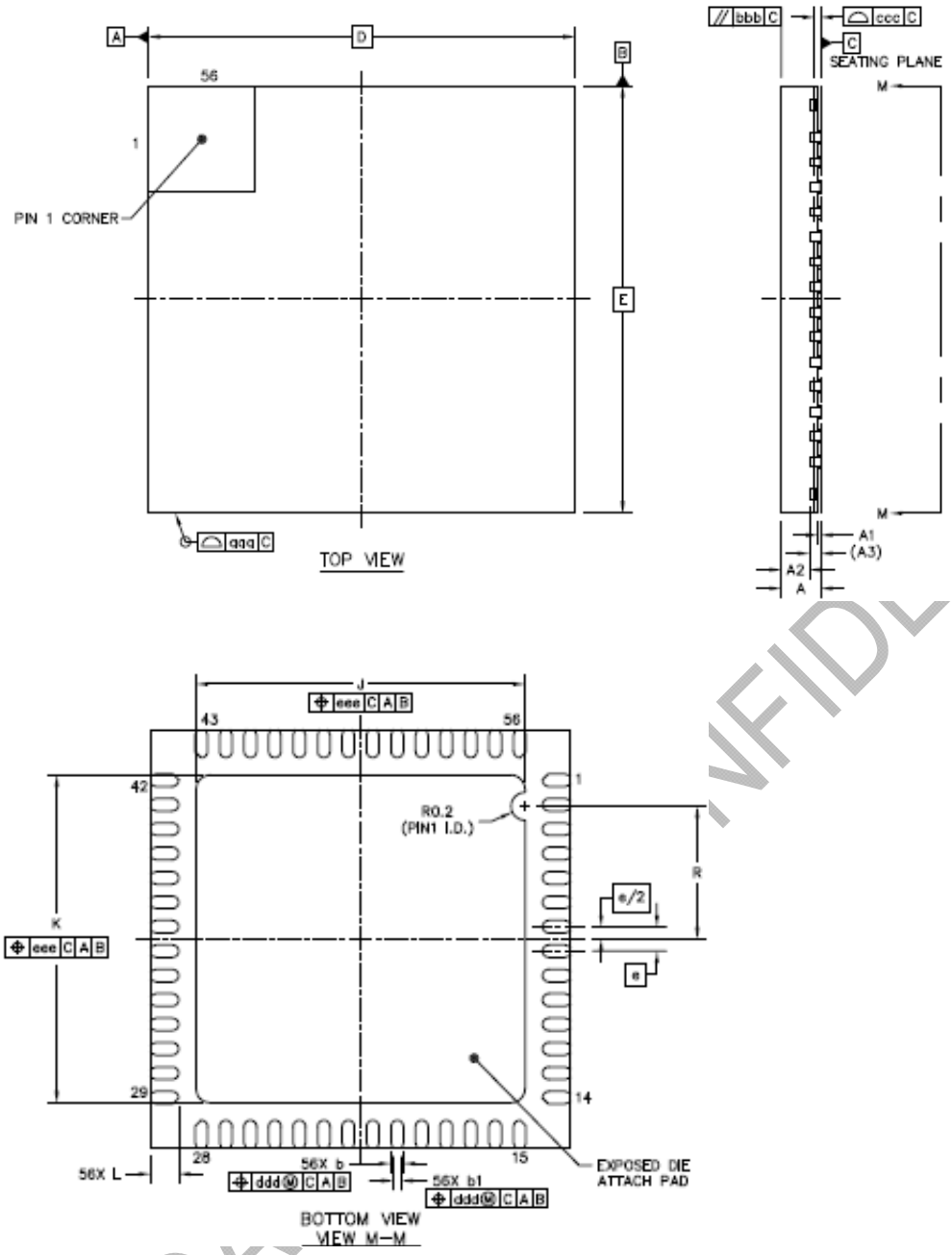
FT5446DQS Package Diagram



FT5446WWa Package Diagram

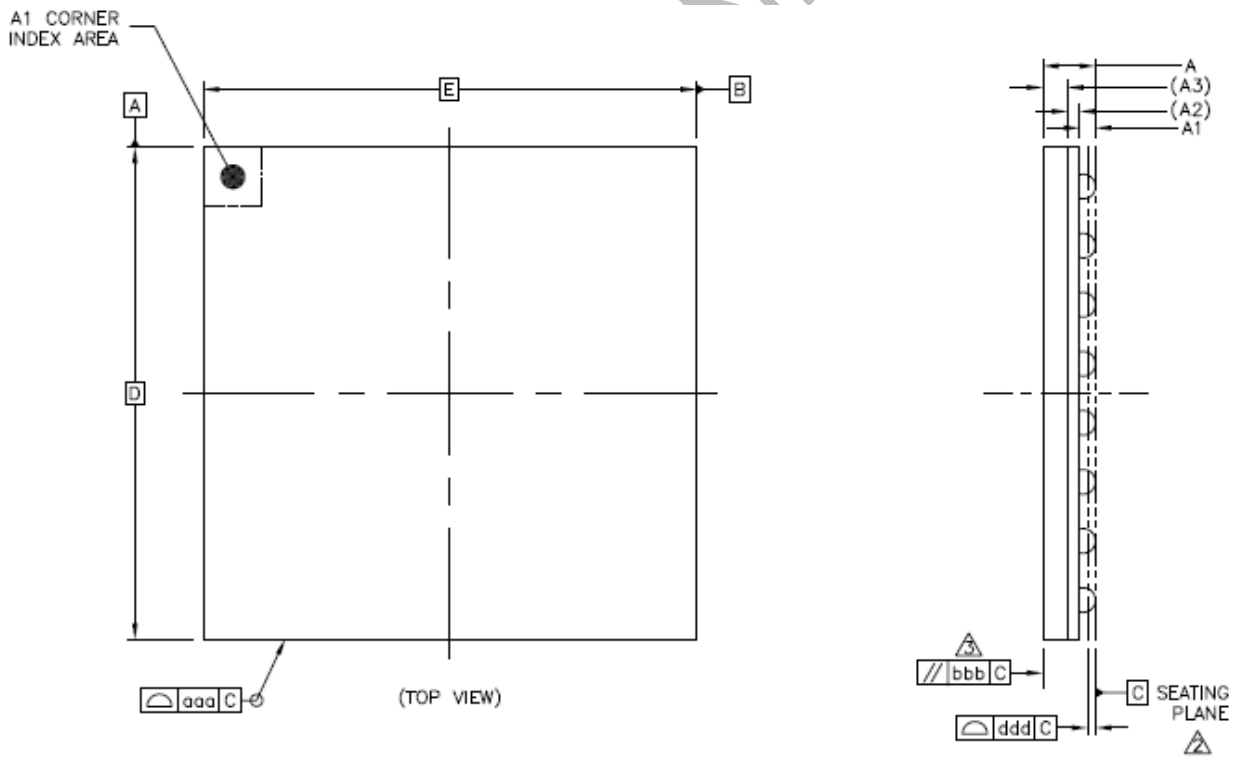
5 PACKAGE INFORMATION

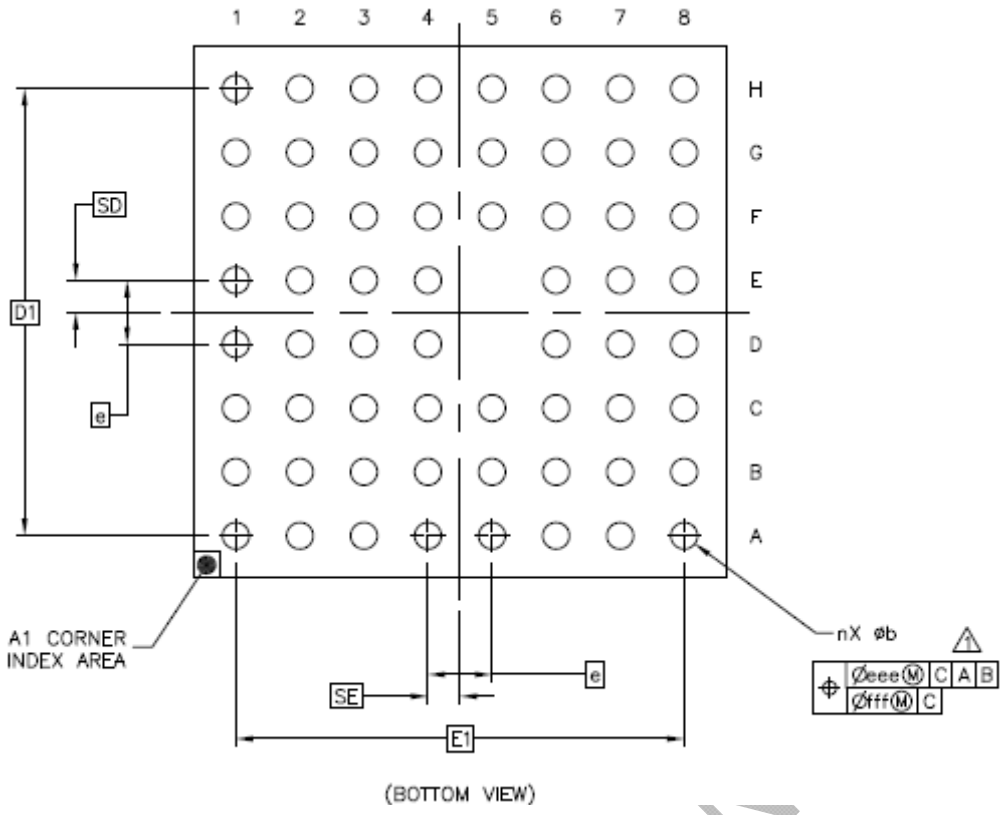
5.1 Package Information of QFN-6x6-56L Package



Item		Symbol	Millimeter		
			Min	Type	Max
Total Thickness		A	0.5	0.55	0.6
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	----	0.4	----
L/F Thickness		A3	0.152 REF		
Lead Width		b	0.13	0.18	0.23
		b1	0.07	0.12	0.17
Body Size	X	D	6 BSC		
	Y	E	6 BSC		
Lead Pitch		e	0.35 BSC		
EP Size	X	J	3.9	4	4.1
	Y	K	3.9	4	4.1
Lead Length		L	0.35	0.4	0.45
		R	1.45	1.55	1.65
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Co Planarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		

5.2 Package Information of BGA-5x5-62L Package





Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	---	---	0.6
Stand Off	A1	0.12	---	0.2
Substrate Thickness	A2	0.125 REF		
Mold Thickness	A3	0.25 REF		
Body Size	D	5 BSC		
	E	5 BSC		
Ball Diameter		0.25		
Ball Opening		0.25		
Ball width	b	0.2		0.3
Ball pitch	e	0.6 BSC		
Ball count	n	62		
Edge Ball Center to Center	D1	4.2 BSC		
	E1	4.2 BSC		
Body Center to Contact Ball	SD	0.3 BSC		
	SE	0.3 BSC		
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.1		
Co Planarity	ddd	0.08		
Ball Offset(Package)	eee	0.15		
Ball Offset(Ball)	fff	0.08		

5.3 Ordering Information

Package Type	QFN/BGA
	56Pin(6 * 6)/62Ball(5 * 5)
	56Pin(0.6 - P0.35)/62Ball(0.6 - P0.6)
Product Name	FT5446

Note:

1). The last three letters in the product name indicate the package type , lead pitch and thickness and numbers of TX and RX.

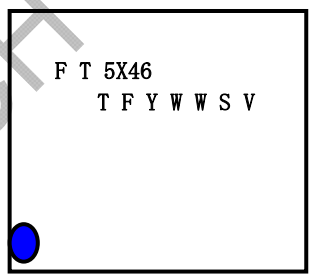
2). The third last letter indicates the package type .
D : QFN-6*6
W: BGA-5*5

3). The second last letter indicates the lead pitch and thickness.
Q : 0.6 - P0.35
W: 0.6 - P0.6

4). The last letter indicates the numbers of TX and RX.
Q: 15TX-24RX
S: 16TX-28RX
a: 20TX-28RX

Date Code :
Code 1~6 : (Serial Code, tracking)

Code 7 : (Version Code, IC version)



Product Name	Package Type	# TX Pins	# RX Pins
FT5346DQQ	QFN-56L	15	24
FT5446DQS	QFN-56L	16	28
FT5446WWa	BGA-62L	20	28

Appendix: IC Revision history of FT5X46 Specification

Version	Change Items	Effective Date
0.01	1st Preliminary	27-Jun-14
0.02	Updated Y Drive	8-Aug-14
1.0	1.Removed Hibernation 2.updated Tpon<=200ms 3.updated Trsi<=200ms 4.updated I2C Timing Characteristics	23-Sept-14

END OF DATASHEET