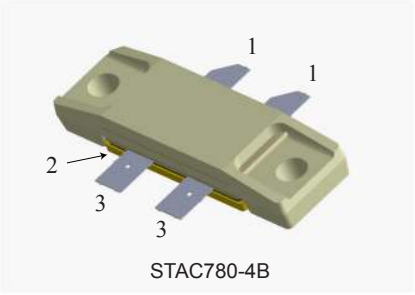
STAC2942B

Datasheet

HF/VHF/UHF RF power N-channel MOSFET



STAC780-4B

Pin connection	
Pin	**Connection**
1	Drain
2	Source (bottom side)
3	Gate

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
STAC2942BW	175 MHz	50 V	350 W	21 dB	60 %

- Gold metallization
- Excellent thermal stability
- Common source push-pull configuration
- P_{OUT} = 350 W min. with 21 dB gain at 175 MHz
- In compliance with the 2002/95/EC European directive
- ST air-cavity STAC packaging technology

Description

The STAC2942B is a gold metallized N-channel MOS field-effect RF power transistor, intended for use in 50 V DC large signal applications up to 250 MHz.

Product status link
STAC2942B

Product summary	
Order code	STAC2942BW
Marking	STAC2942
Package	STAC780-4B
Packing	Box
Base / Bulk qty	20 / 80

1 Electrical data

1.1 Maximum ratings

Table 1. Absolute maximum ratings (T_{CASE} = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$[1]	Drain source voltage	130	V
V_{DRG}[1]	Drain-gate voltage (R_{GS} = 1 MΩ)	130	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current	40	A
P_{DISS}	Power dissipation	625	W
T_J	Maximum operating junction temperature	200	°C
T_{STG}	Storage temperature range	-65 to +150	°C

1. T_J = 150 °C

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction-case thermal resistance	0.28	°C/W

1.3 ESD protection characteristics

Table 3. ESD protection

Symbol	Test Methodology	Class
HBM	Human Body Model (per JESD22-A114)	2

2 Electrical characteristics

(T_{CASE} = +25 °C, unless otherwise specified)

2.1 Static

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain - Source Breakdown voltage	V_{GS} = 0 V, I_{DS} = 100 mA, T_J = 150 °C	130			V
I_{DSS}	Zero gate voltage drain Leakage Current	V_{GS} = 0 V, V_{DS} = 50 V			100	µA
I_{GSS}	Gate - Source leakage current	V_{GS} = 20 V, V_{DS} = 0 V			250	nA
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 10 V, I_D = 250 mA	1.5	2.5	4.0	V
$V_{DS(ON)}$	Drain - Source on voltage	V_{GS} = 10 V, I_D = 10 A			3	V
G_{FS}	Forward transconductance	V_{DS} = 10 V, I_D = 5 A	5			S
C_{ISS}	Input capacitance	V_{DS} = 50 V, f = 1 MHz		425		pF
C_{OSS}	Ouput capacitance			202		pF
C_{RSS}	Reverse transfer capacitance			12		pF

2.2 Dynamic

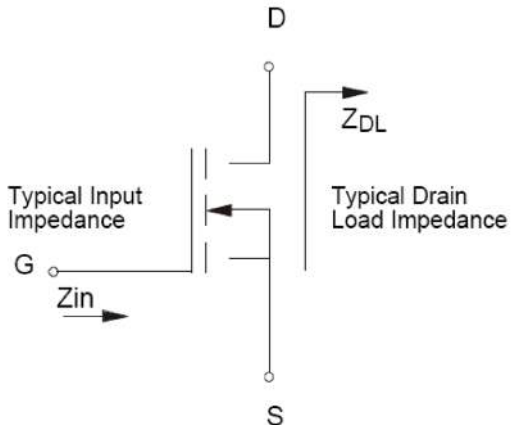
Table 5. Dynamic (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	P_{IN} = 4 W	350	450	-	W
η_D	Drain efficiency	P_{IN} = 4 W	60	75	-	%
VSWR	Load mismatch	P_{OUT} = 350 W, all phases angles			5:1	

1. *F = 175 MHz, V_{DD} = 50 V, I_{DQ} = 2 X 250 mA.*

3 Impedance

Figure 1. Current conventions



GADG170720191138MT

Table 6. Impedance data

Freq. (MHz)	Z_{IN} (Ω)	Z_{DL}(Ω)
175	2.0 - j2.0	3.5 + j 5.2

Note: Measured gate-to-gate and drain-to-drain, respectively, balanced configuration.

4 Typical performance

Figure 2. Capacitances versus drain supply voltage

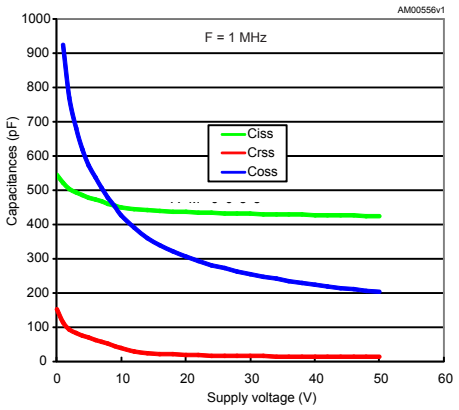


Figure 3. Output power versus drain supply voltage

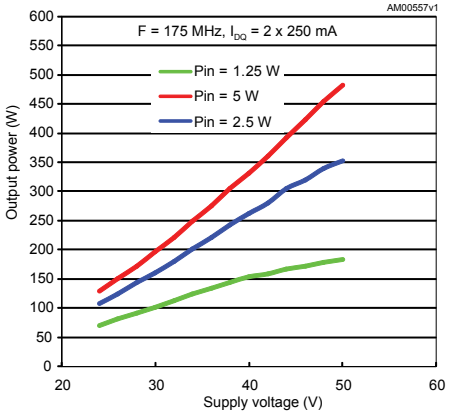


Figure 4. Output power versus gate voltage

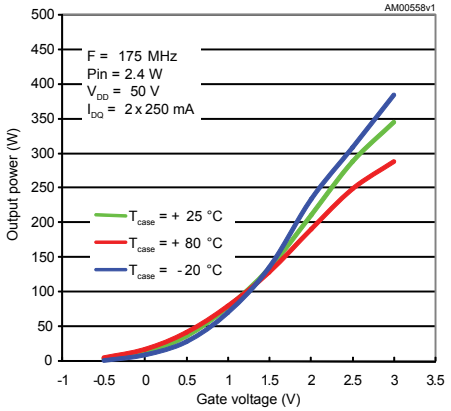


Figure 5. Output power versus input power

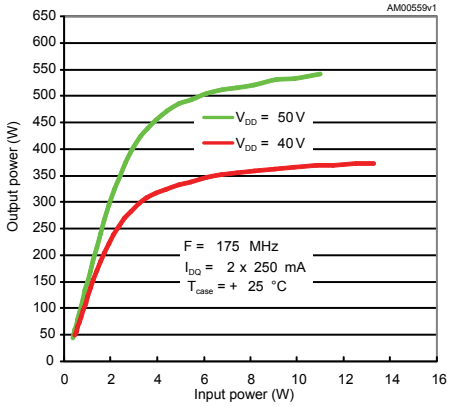


Figure 6. Output power vs input power and case temperature

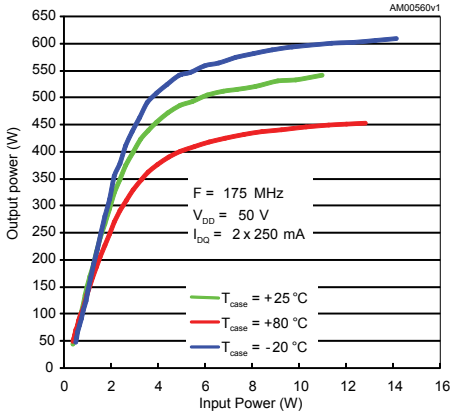


Figure 7. Efficiency vs output power and case temperature

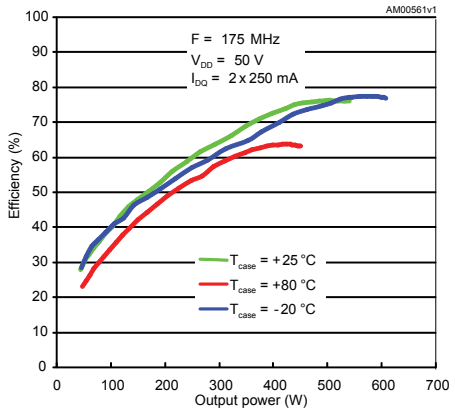


Figure 8. Power gain vs output power and case temperature

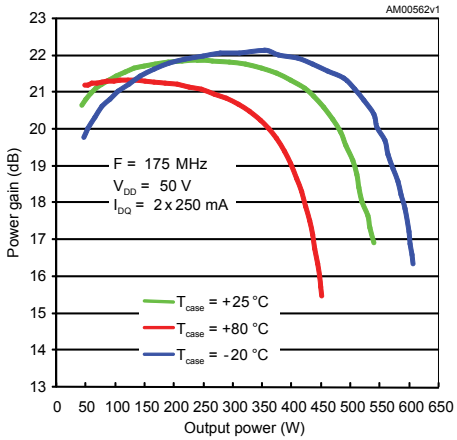


Figure 9. Safe operating area

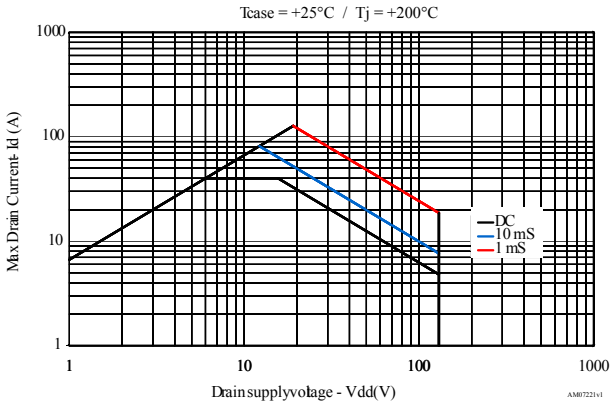


Figure 10. Transient thermal impedance

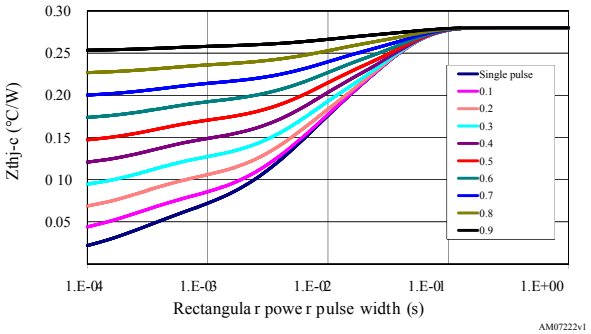
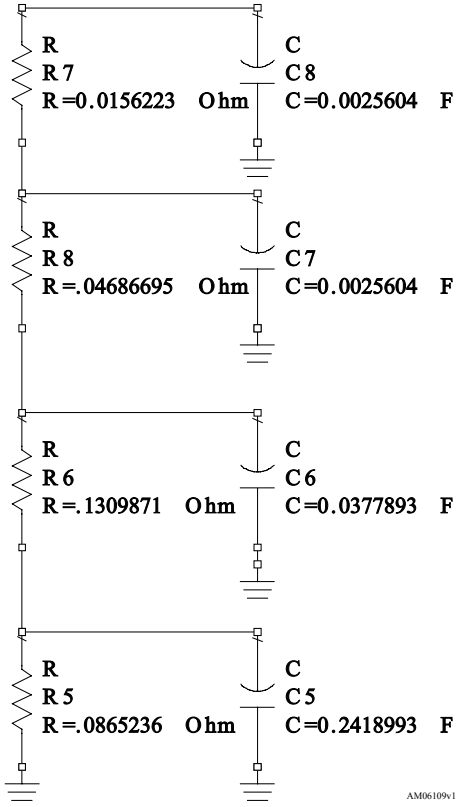


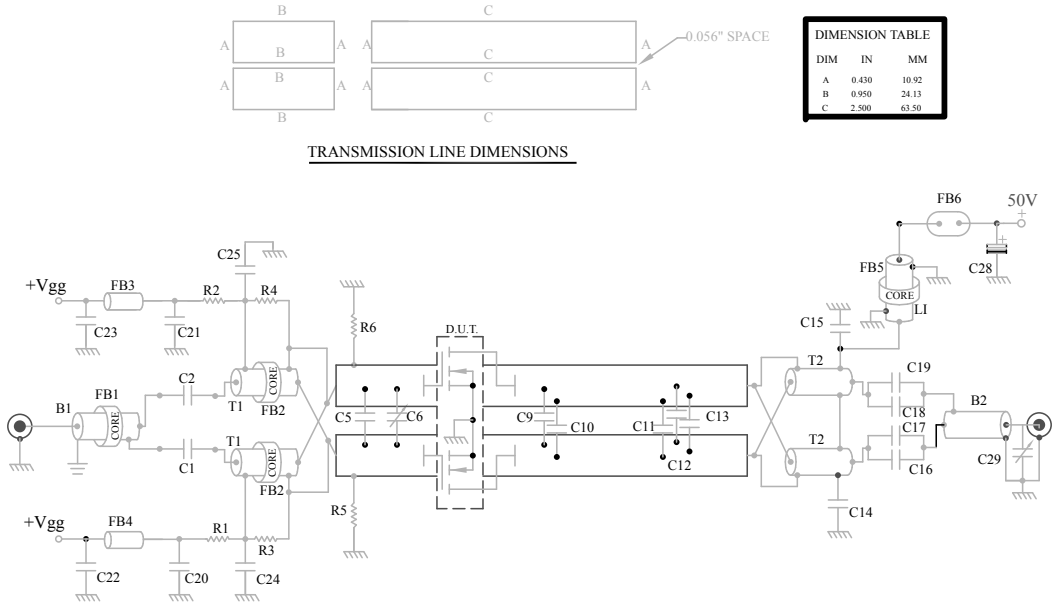
Figure 11. **Transient thermal model**



5 Test circuit

5.1 Electrical schematic and BOM

Figure 12. 175 MHz test circuit schematic (production test circuit)



NOTES:
1. DIMENSIONS AT COMPONENT SYMBOLS ARE REFERENCE FOR COMPONENT PLACEMENT. SEE SHEET 1.
2. GAP BETWEEN GROUND & TRANSMISSION LINES IS 0.056[1.42] TYP

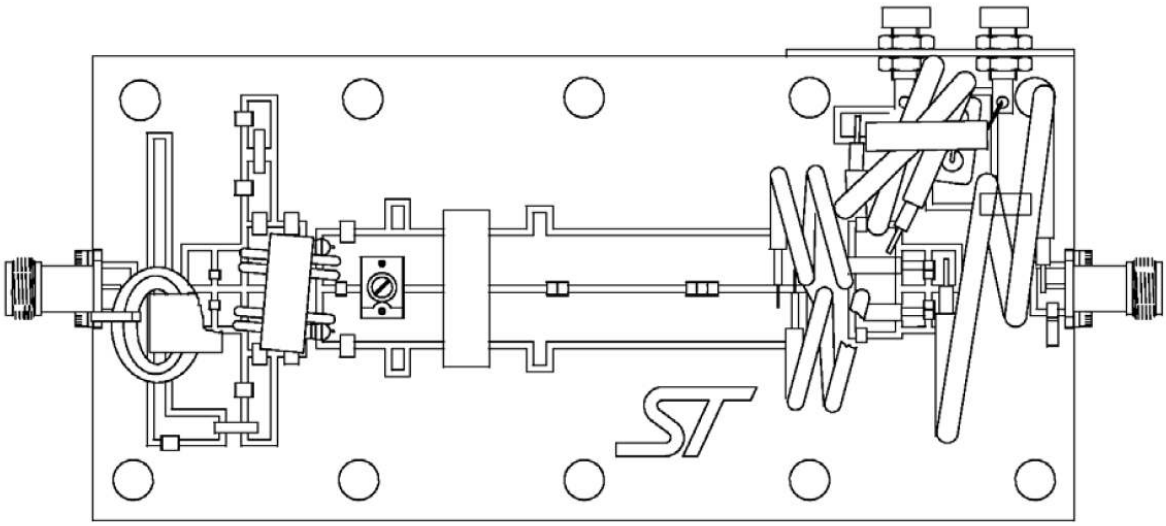
AM00528v1

Table 7. 175 MHz test circuit component list

Component	Description
C1, C2, C14, C15, C24, C25	1200 pF ATC 700B chip capacitor
C5	75 pF ATC 100B chip capacitor
C6	ST406 variable capacitor
C9, C10	47 pF ATC 100B chip capacitor
C11, C12, C13	43 pF ATC 100B chip capacitor
C16, C18	470 pF ATC 100B chip capacitor
C17, C19, C20, C21	10,000 pF ATC 200B chip capacitor
C22, C23	0.1 µF 200 V chip capacitor
C28	10 µF 100 V electrolytic capacitor
C29	0.8 - 8 pF variable capacitor
R1, R2, R5, R6	430 Ω, 1/2 W chip resistor
R3, R4	270 Ω 1/2 W axial lead resistor
B1	RG-316 50 Ω 11.8" through ferrite toroid
B2	RG-142 50 Ω 11.8"
T1	4:1, RG-316 25 Ω, 5.9", 2 turns thru ferrite core
T2	1:4, 25 Ω semi-rigid cable, OD .141", 5.9"
L1	λ/4 inductor, RG-142 50 Ω, 11.8", 3 turns thru ferrite toroid
FB1,FB5	Ferrite toroid
FB2, FB6	Multi-aperture core
FB3, FB4	Surface mount ferrite bead
PCB	Rogers ultralam 2000, Er 2.55, .060"

5.2 Test circuit layout

Figure 13. **Test circuit**

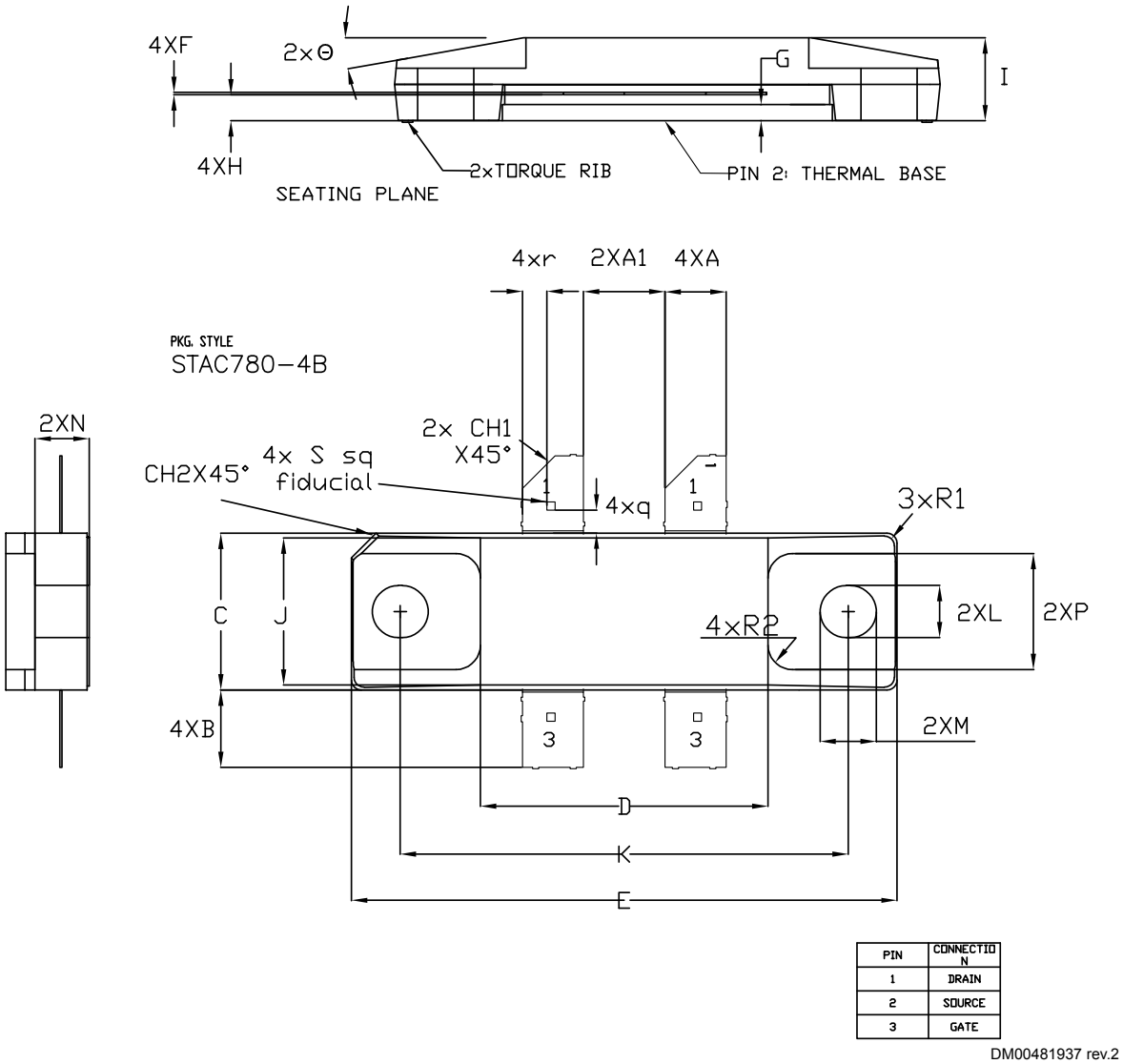


6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 STAC780-4B package information

Figure 14. **STAC780-4B package outline**



DM00481937 rev.2

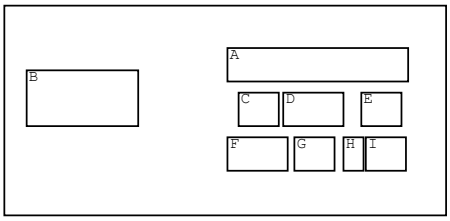
Table 8. **STAC780-4B mechanical data**

Symbol	Milimeters		
	Min	Typ	Max
A	3.76		3.86
A1	5.03		5.13
B	4.57		5.08
C	9.65		9.91
D	17.78		18.08
E	33.88		34.19
F	0.13		0.18
G	0.97		1.14
H	1.52		1.70
I	4.83		5.33
J	9.52		9.78
K	27.69		28.19
L	3.20	3.25	3.30
M	3.43	3.51	3.58
M	3.30	3.38	3.45
p	7.14	7.21	7.29
q		1.45	
R1		0.64	
R2		1.52	
r		1.52	
s		0.51	
Θ		10°	
CH1		2.03	
CH2		1.52	

6.2 Marking information

Figure 15. **Marking information**

PACKAGE FACE : TOP



LEGEND

Marking Composition Field

A - MARKING AREA
B - ST LOGO
C - Assy Plant
(PP)
D - BE Sequence
(LLL)
E - Diffusion Traceability Plant
(WX)
F - COUNTRY OF ORIGIN
(MAX CHAR ALLOWED = 3)
G - Test & Finishing Plant
(TF)
H - Assy Year
(Y)
I - Assy Week
(WW)

Revision history

Table 9. **Document revision history**

Date	Version	Changes
20-Mar-2009	1	First release.
16-Apr-2010	2	Added Figure 10, Figure 11 and Figure 12.
12-Aug-2011	3	Update figures on coverpage and Section 6: Package mechanical data. Inserted Section 7: Marking, packing and shipping specifications.
05-Sep-2011	4	Update L and M dimensions Table 8 on page 13.
11-Oct-2011	5	Updated order code in Table 1: Device summary and Table 9: Packing and shipping specifications. Updated Table 10: Marking specifications and Figure 16: Marking layout. Modified document title.
17-Jan-2012	6	Updated Table 5: Dynamic new “load mismatch” has been inserted.
27-Jan-2014	7	Modified pin labeling in Figure 1: Pin connection.
03-Apr-2020	8	Updated package information. Added Section 1.3 ESD protection characteristics.

Contents